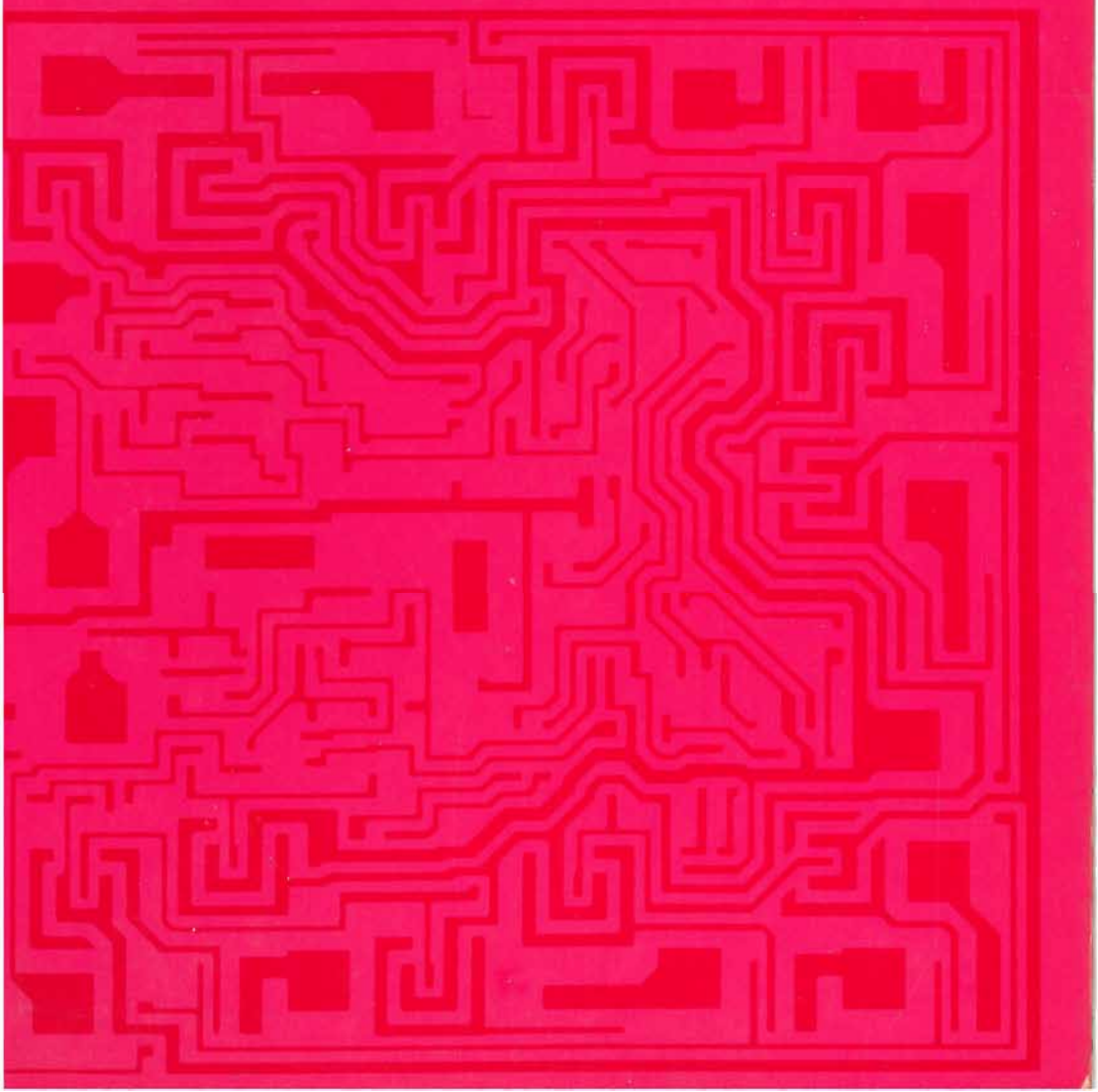
PROFESSIONAL SEMICONDUCTOR

DATABOOK 2

SGS ATES

1975/76



PROFESSIONAL SEMICONDUCTOR DATABOOK 2

SGS ATES 1975/76

INTRODUCTION

This databook contains data sheets on the SGS-ATES range of bipolar digital silicon integrated circuits intended for professional applications. To permit ease of consultation, it has been divided into six main sections: Index, DTL, TTL, HLL, LPDTL and RTL integrated circuits.
Since the LPDTL and RTL families are not recommended for new designs only a brief resumé of the available devices has been included. Full data sheets are still available and will be supplied free on request.
At the beginning of each section, an analytical index of applications refers to the corresponding pages containing fully characterized data on the appropriate types.
The information on each product has been specially presented in order that the performance of the product can be readily evaluated within any required equipment design.
Particular attention has been given to the measurement of the characteristics of all integrated circuits to ensure that they conform to the Company's Semiconductor Users' Reliability Evaluation programme (SURE).
The SURE programme has been carefully devised so as to be compatible with any national or international quality assurance programme. It is continuous (performed on all production batches), repetitive (performed under fixed conditions) and comprehensive (represents as many military and industrial specifications as possible).
It is emphasised that all products are produced from the same high grade silicon material and by the same manufacturing processes, the only difference in their classification being in the number and severity of tests applied and the degree of information supplied on each test.

OTHER SGS-ATES DATABOOKS

The SGS-ATES range of products includes discrete devices, linear and digital integrated circuits for both consumer and professional applications. Data sheets on these devices can be found in the following databooks:

SGS-ATES Professional Databook 1 - Small Signal Discrete Devices

SGS-ATES Professional Databook 3 - Linear, MOS & COS/MOS ICs

SGS-ATES Consumer Databook - Transistors & ICs

SGS-ATES Power Databook - Discrete Devices

SGS-ATES GROUP OF COMPANIES

INTERNATIONAL HEADQUARTERS
SGS-ATES Componenti Elettronici S.p.A.
Via C. Olivetti 2 - 20041 Agrate Brianza - Italy
Tel.: 039-650341÷4 / 650441÷5 / 650841÷5
Telex: 36141-36131

BENELUX
SGS-ATES Componenti Elettronici S.p.A.
Benelux Sales Office
-B- 1180 Bruxelles
Winston Churchill Avenue, 112
Tel.: 02-3432439
Telex: 011-24149

DENMARK
SGS-ATES Scandinavia AB
Sales Office:
2730 Herlev
Marielundvej 46A
Tel.: 02-948533
Telex: 16494

FRANCE
SGS-ATES France S.A.
75643 Paris Cedex 13
Résidence "Le Palatino"
17, Avenue de Choisy
Tel.: 5842730
Telex: 021-25938

GERMANY
SGS-ATES Deutschland Halbleiter-Bauelemente GmbH
809 Wasserburg/Inn
Postfach 1269
Tel.: 08071-721
Telex: 05 25143
Sales Offices:
1000 Berlin 33
Warmbrunner Strasse 39
Tel.: 030-8233038
Telex: 01 85418
3000 Hannover 1
Lange Laube 19
Tel.: 0511-17522/3
Telex: 09 23195
8000 München 40
Gernotstrasse 10
Tel.: 089-304270/304485
Telex: 05 215784
7000 Stuttgart 80
Kalifenweg 45
Tel.: 0711-713091/2
Telex: 07 255545

ITALY
SGS-ATES Componenti Elettronici S.p.A.
Sales Offices:
50127 Firenze
Via Giovanni Del Pian Dei Carpini 96/5
Tel.: 055-4377763
20149 Milano
Via Tempesta 2
Tel.: 02-4695651
00199 Roma
Piazza Gondar 11
Tel.: 06-8392848/8312777
10134 Torino
Via La Loggia 51/7
Tel.: 011-634572

NORWAY
SGS-ATES Scandinavia AB
Sales Office:
Oslo 4
Sandakerveien 104B
Tel.: 213755
Telex: 11796

SINGAPORE
SGS-ATES Singapore (Pte) Ltd.
Singapore 12
Lorong 4 & 6 - Toa Payoh
Tel.: 531411
Telex: ESGIES RS 21412

SWEDEN
SGS-ATES Scandinavia AB
19501 Märsta
Industrigatan 2
Tel.: 0760-40120
Telex: 042-10932

UNITED KINGDOM
SGS-ATES (United Kingdom) Ltd.
Aylesbury, Bucks
Planar House, Walton Street
Tel.: 0296-5977
Telex: 041-83245

U.S.A.
SGS-ATES Semiconductor Corporation
Newtonville, Mass. 02160
435 Newtonville Avenue
Tel.: 617-9691610
Telex: 922482

GENERAL ALPHA-NUMERICAL INDEX

E. = Extended temperature range
I. = Intermediate temperature range
S. = Standard temperature range

DTL INTEGRATED CIRCUITS

DTL INTEGRATED CIRCUITS

DTL 930 SERIES

E. = Extended temperature range
S. = Standard temperature range

diode-transistor logic family

EXTENDED TEMPERATURE RANGE - 55°C+ 125°C

- Compatible with TTL and LPDTL products
- Noise Immunity 1V
- Output drive capability of 10
- Power dissipation 8.5 mW per gate
- Fan-in expansion capability
- Wired-OR capability
- Same pin configuration as the corresponding TTL and LPDTL products

The SGS Diode-Transistor Logic (DTL) Family consists of a set of compatible integrated circuits designed for medium power, medium speed applications.
The circuits are fabricated within a silicon monolithic substrate using the standard Planar epitaxial process.
DTL elements are available in two hermetically sealed ceramic packages : the Dual in-Line Package (6A) designed for low cost insertion, and the 14 leads flat package (3I) for maximum component density.

ORDERING NUMBER

U6A XXXX51X
(for Dual in-Line Package, XXXX is type number)
U3I XXXX51X
(for Flat Package, XXXX is type number)

ABSOLUTE MAXIMUM RATINGS

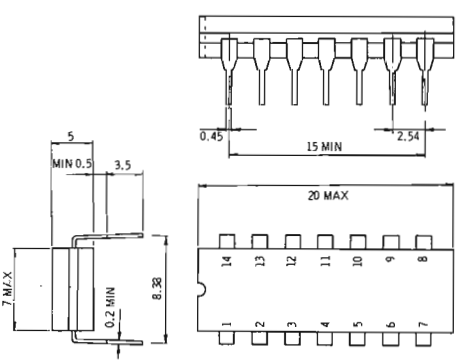
(above which the useful life may be impaired)

Supply voltage (V_{CC}), continuous	8 V
Supply voltage (V_{CC}), pulsed < 1 sec	12 V
Output current, into outputs	
DTL 9932 - 9944	100 mA
Other elements	30 mA
Input forward current	-10 mA
Input reverse current	1 mA
Temperature (ambient) under bias	- 55°C to 125°C
Storage temperature	- 65°C to 150°C

OPERATING CONDITIONS

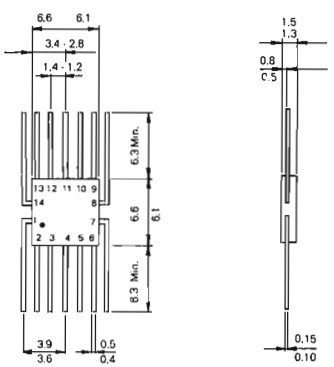
Temperature range	- 55°C to 125°C
Supply voltage	5 V ± 10 %

PHYSICAL DIMENSIONS
Dual-In-Line ceramic package



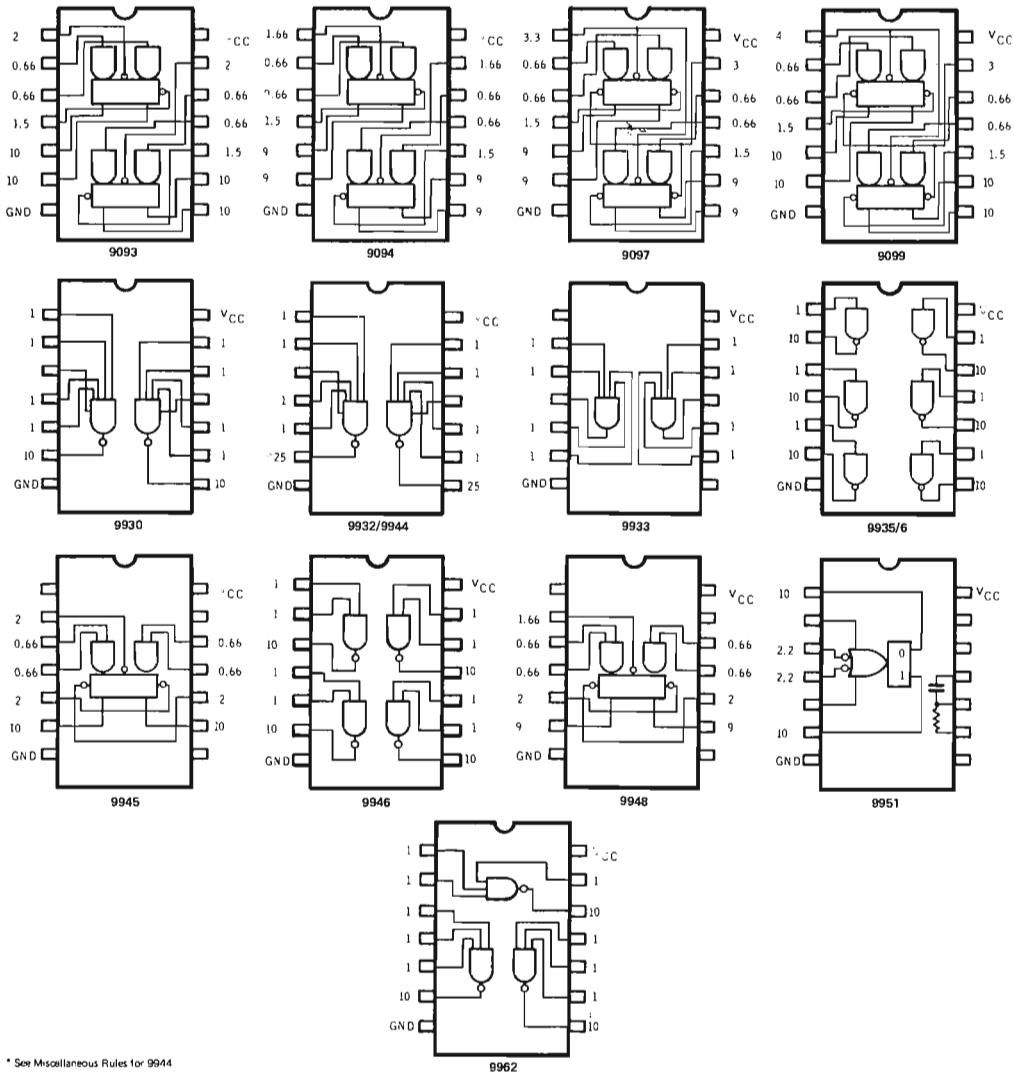
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
Flat ceramic package



NOTE : All dimensions in mm.

INPUT-OUTPUT LOAD/DRIVE FACTORS



* See Miscellaneous Rules for 9944

MISCELLANEOUS RULES

The number of elements driven by an output terminal may consist of any combination of elements whose sum of input load factors does not exceed the output drive factor.

An external resistor should be used with 9944. With an external resistor R the following output drive factors will be obtained :

R = 6 KΩ Drive Factor = 26
R = 2 KΩ Drive Factor = 25
R = 1 KΩ Drive Factor = 23
R = 510Ω Drive Factor = 20

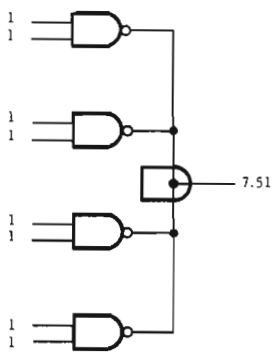
For increased output drive, the inputs and outputs of 1/2 DTL 9944 may be paralleled, up to 4 common outputs. For 4 paralleled elements:

each combined input, load factor = 4
each combined output, drive factor = 100 (R = 2 KΩ)

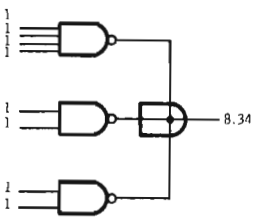
"WIRED OR" CONNECTION

1. Outputs of DTL gates may be tied together for the "wired OR" function
   ($\overline{ABCD} \cdot \overline{GHIJ} = \overline{ABCD + GHIJ}$). Subtract, for each added gate, 0.83 unit load from output drive factor.
2. Outputs of DTL 9932 may not be tied together for the "wired OR" function.

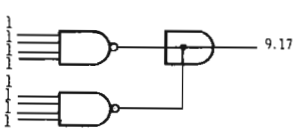
"WIRED OR" Examples :



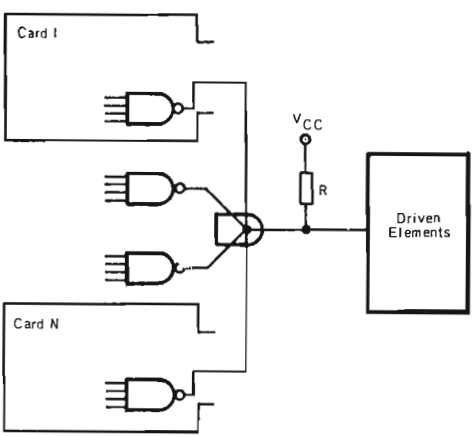
4 × ¼ DTL 9946



½ 9930 and
2 x ¼ 9946



DTL 9930 WIRED OR



Each output driver is 1/2 DTL 9944. Note that the DTL 9944 is a direct high fan-out replacement for DTL 9930, except that an external resistor must be used. The F.O. will be the same as one 1/2 DTL 9944 buffer used with that resistor.

DELAY TIME PERFORMANCE INTO CAPACITIVE LOADS

Most delay attributable to capacitive loads is associated with the positive going output. Two R-C time constants are seen in the positive going output. In the 1st time period, from the saturated low level to threshold, the R of the RC time constant can be given by 6 KΩ in parallel with $\frac{3.75\ K\Omega}{\text{active fanout}}$

Above the threshold which occurs at about 1.4 to 1.5 volts at 25°C, the R of the 2nd R C time constant is 6 kΩ and the rate of the voltage rise above threshold is slow. The logic signal propagates through at the threshold level, so voltage rise above threshold does not affect speed. By noting that both rise domains drive toward V_{CC}, the voltage rise waveform may be calculated. DTL gate inputs are ~ 2 pf per input for active or inactive fanout; the remaining capacitance is from board, wiring, and connectors.

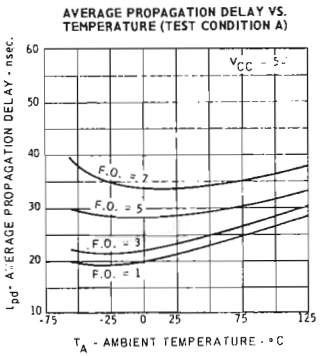


FIG. 1

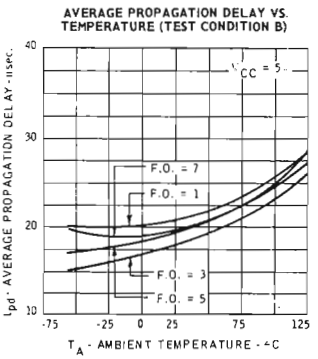
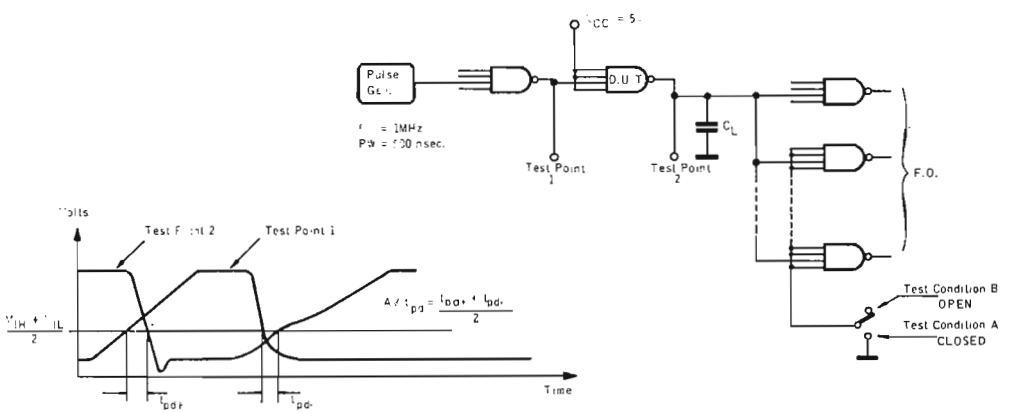


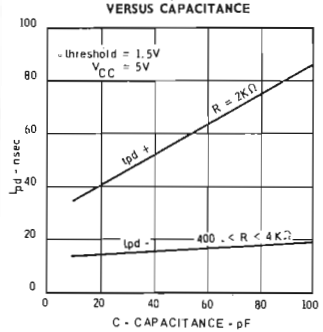
FIG. 2

TEST CONDITIONS FOR FIG. 1 AND 2

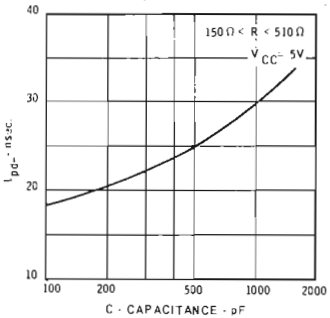


t_{pd} CURVES VERSUS OUTPUT CAPACITANCE (T_A = 25°C unless otherwise noted)

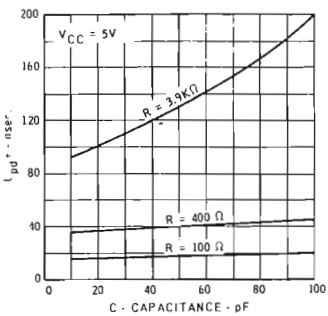
TYPICAL t_{pd} OF GATES VERSUS CAPACITANCE



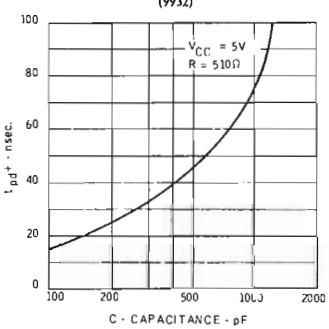
t_{pd} VERSUS CAPACITANCE (9932 - 9944)



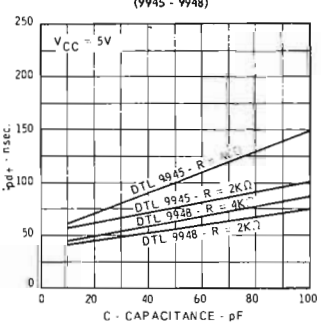
t_{pd} VERSUS CAPACITANCE (9944)



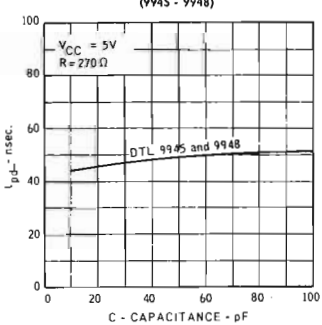
t_{pd+} VERSUS CAPACITANCE (9932)



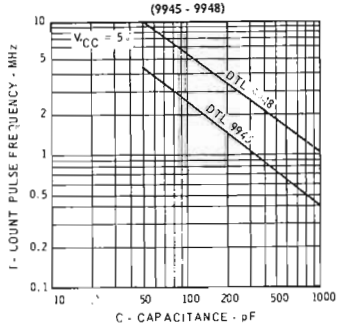
t_{pd} VERSUS CAPACITANCE (9945 - 9948)



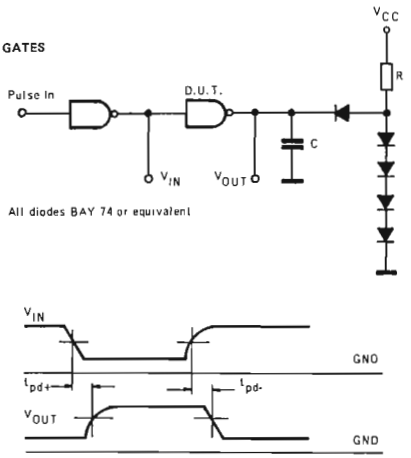
t_{pd-} VERSUS CAPACITANCE (9945 - 9948)

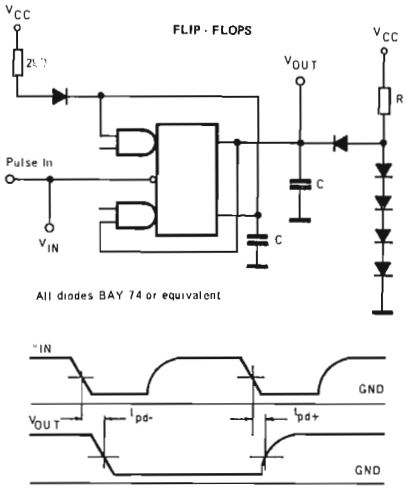


MAXIMUM BINARY COUNTING RATE VERSUS CAPACITANCE (9945 - 9948)

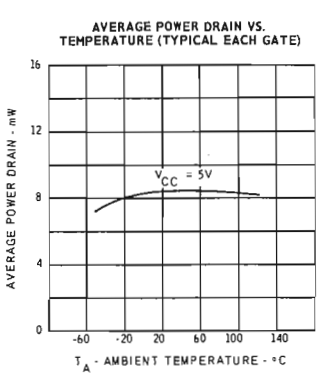


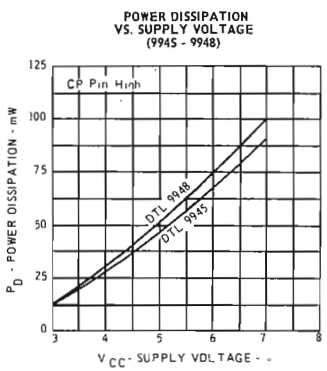
TEST CIRCUITS

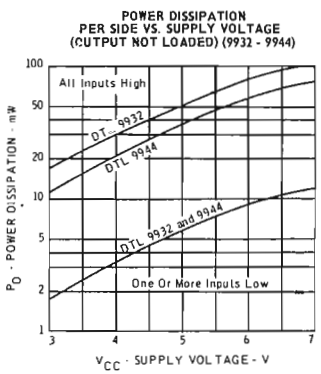




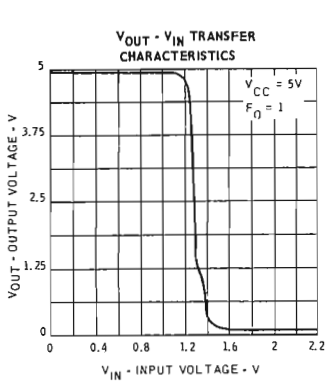
POWER DISSIPATION CURVES (T_A = 25° unless otherwise noted)

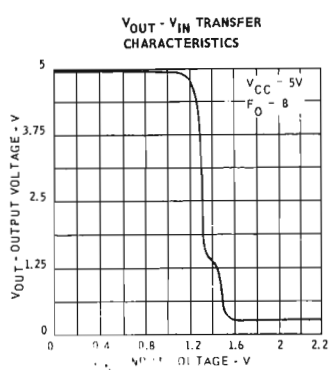


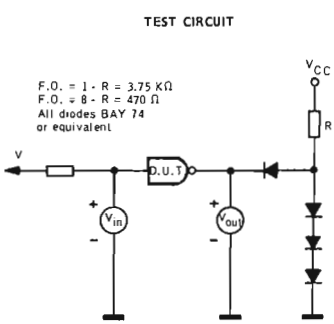




TRANSFER CHARACTERISTICS (T_A = 25°C unless otherwise noted)







NOISE IMMUNITY

There are two types of noise immunity which can be guaranteed : Signal Noise Immunity or Ground Noise Immunity.

(A) Signal noise immunity $|V_{IL} - V_{OL}| = V_{NS}$
or $|V_{OH} - V_{IH}| = V_{NC}$

where V_{IL} = Maximum Low Input Voltage that guarantees V_{OH}
V_{OL} = Maximum Low Output Voltage
V_{IH} = Minimum High Input Voltage that guarantees V_{OL}
V_{OH} = Minimum High Output Voltage

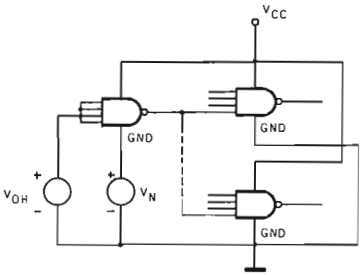
(B) Ground noise immunity, V_{NG}. The worst case noise immunity for diode-transistor logic circuits is usually ground noise V_{NG}.

Note that some curves show two values of V_{CC} at given temperature for the same noise immunity. The upper V_{CC} corresponds to noise immunity such that $V_N \approx V_{NS} \approx V_{NG} \approx V_{IL} - V_{OL}$. The driving device is hard in saturation and V_{NG} simply adds to V_{OL}. The lower V_{CC} corresponds to soft saturation where V_{NG} tends to turn off the drive gate. There is voltage gain therefore between V_{NG} and the output node and V_{NG} is significantly less than $V_{IL} - V_{OL}$.

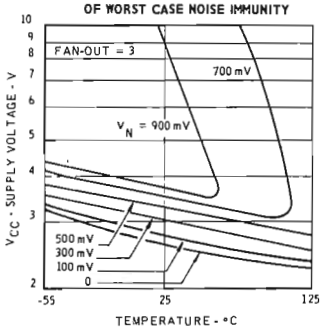
Each of the curves on this page shows V_N, the worst case of V_{NG} and V_{NS}.

As an example the curves for fan-out of 7 show a worst case $V_N = V_{NG}$ of 200 mV at V_{CC} = 4 V and -55°C. This, however, corresponds to a worst case signal noise immunity of $V_{IL} - V_{OL}$ 500 mV for the same fan-out, temperature, and V_{CC}.

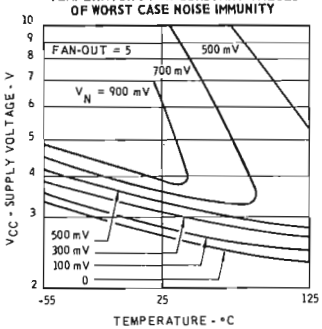
TEST CIRCUIT



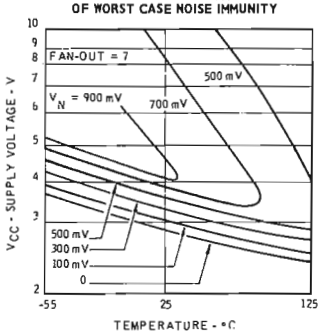
SUPPLY VOLTAGE VS. TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY



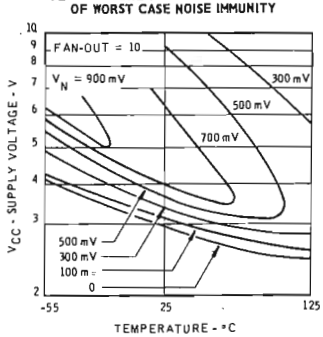
SUPPLY VOLTAGE VS. TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY



SUPPLY VOLTAGE VS. TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY



SUPPLY VOLTAGE VS. TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY



MINIMUM - MAXIMUM DC CURVES, I_F VS. V_{CC} & V_F

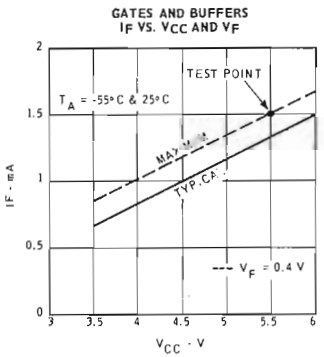


FIG. 1

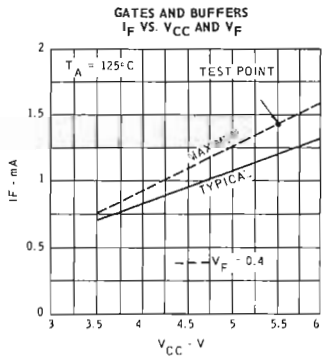


FIG. 2

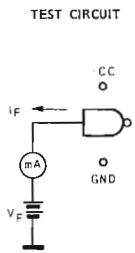


FIG. 3

OUTPUT LOW CURRENT VS. V_{CC} & V_{OL} FOR GATES

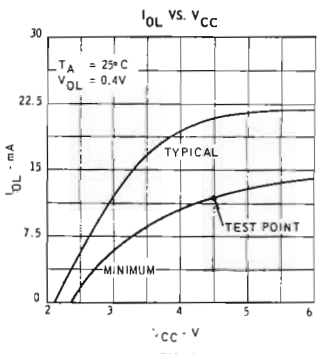


FIG. 4

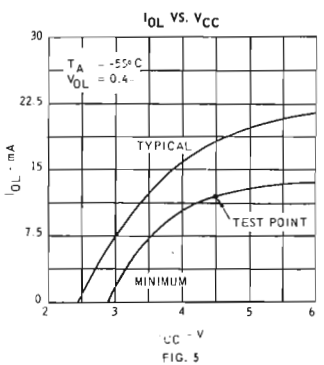


FIG. 5

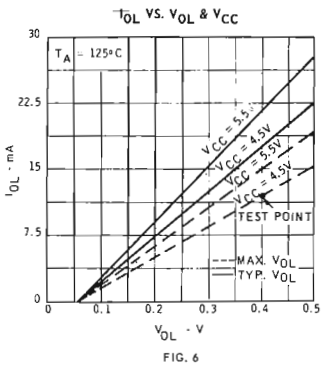


FIG. 6

BUFFERS GATES INPUT THRESHOLD VS. TEMPERATURE

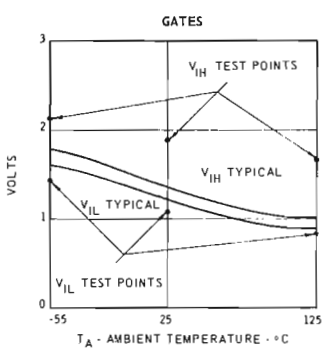


FIG. 7

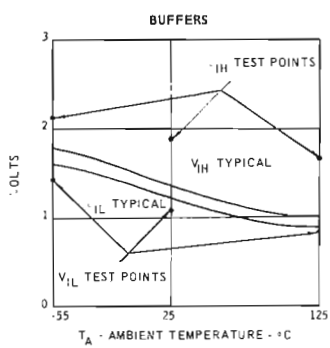


FIG. 8

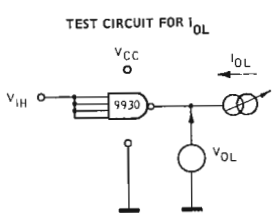
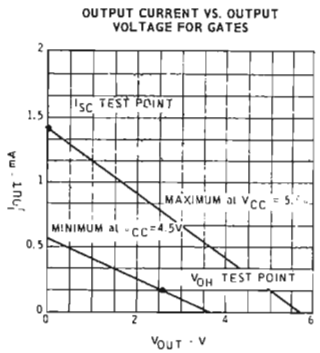
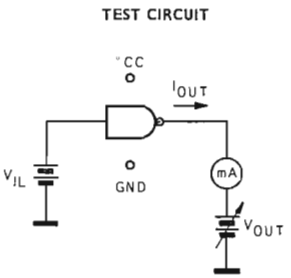


FIG. 9

OUTPUT CURRENT VS. OUTPUT VOLTAGE FOR GATES

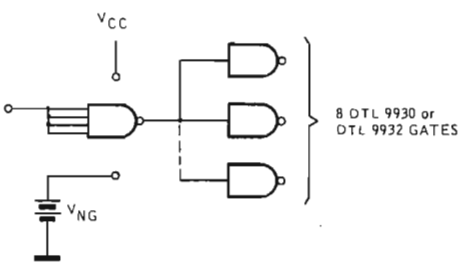




EXAMPLES OF USES FOR THE MINIMUM-MAXIMUM DC CURVES (Page 136)

EXAMPLE 1.

A low DTL 9930 output at -55°C fans out to 8 inputs of DTL 9930 or 9932 V_{CC} = 5 V. Positive DC ground noise (V_{NG}) of 350 mV is applied to the 1st 9930. Its output may thus rise to 0.75 Volt (V_{NG} + V_{OL}). 4.65 Volts (V_{CC} - V_{NG}) remain from V_{CC} pin to ground pin; this is above V_{CCL} = 4.5 V, and test I_{OL} is conservative. Maximum current flowing in each input of the 8 9930/9932's is given by Fig. 1 on Page 136 with V_F = 0.75 V and V_{CC} = 5 V : the current (I_F) is less than 1.25 mA and total current ($\leq 8 \times 1.25$ = 10 mA) is less than the I_{OL} test current used at -55°C to saturate the low output.
Above the 350 mV of V_{NG} already applied, the difference between the common node voltage (< 0.75 V) and the low input threshold ($V_{IL} \approx$ 1.40 V) of the 8 9930/9932's is still $\geq$ 350 mV, allowing for signal noise to be superposed above ground noise.



EXAMPLE 2.

The I_F and I_{OL} curves on Page 136 may be expressed in analytical form, as follows

$$I_F \leq \frac{V_{CC} - V_F - V_{FD}}{3\,k\Omega} \quad T_A < 25°C$$

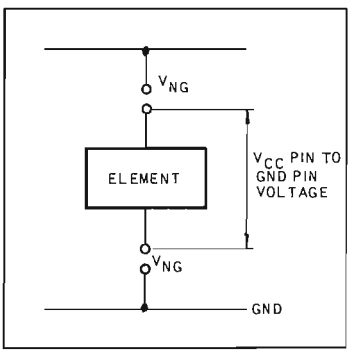
For T_A greater than 25°C, the 3 kΩ rises by 0.12%/°C to approximately 3.36 kΩ at 125°C. V_{FD} is the temperature dependent silicon forward diode drop and is about 0.7 V at 25°C and 1 mA. . . V_{FD}/°C is roughly 1.8 mV/°C.
The ratio of I_{OL}, on gates (figs. 4,5, and 6 at page 136) at V_{CC} below test V_{CC}, to I_{OL} at test V_{CC} can be given by

$$\frac{I_{OL} \text{ @ } -55°C}{\text{Test } I_{OL} \text{ @ } V_{CCL} = 4.5\,V} > \frac{V_{CC} - 3\,V}{4.5\,V - 3\,V} \quad \text{and by} \quad \frac{I_{OL} \text{ @ } 25°C}{\text{Test } I_{OL} \text{ @ } V_{CCL} = 4.5\,V} > \frac{V_{CC} - 2.3\,V}{4.5\,V - 2.3\,V}$$

Since, at 25°C, I_{OL} > 12 mA at V_{CCL} = 4.5 is guaranteed by the test point fig. 4 page 136 I_{OL} at V_{CC} pin to GND pin voltage of 3.6 V is $\frac{3.6 - 2.3}{4.5 - 2.3}$ 12 mA = 7.1 mA.
The similar expression for the 9932 power gate gives a very conservative value due to the phase splitter gain. Above V_{CCL}, I_{OL} is limited by V_{OL} with an essentially resistive ($\frac{V_{OL}}{I_{OL}}$ saturation resistance slope). Fig. 6 at 125°C shows this, with V_{CC} having relatively small effect.

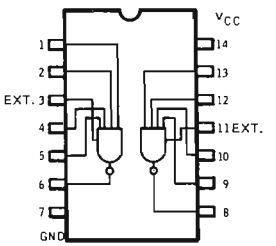
EXAMPLE 3.

The test sequences and tables of conditions and limits use two values of V_{CC}, V_{CCL} and V_{CCH}. With a nominal 5 volts V_{CC} for example, and assuming $\pm V_{CC} = + 0.2V$, testing at $V_{CCL} = 4.5$ V and $V_{CCH} = 5.5$ V allows simulation of ± 0.3V ground noise V_{NG} or V_{CC} line noise V_{NG}. Since there is gain associated with V_{NG}, particularly at lower temperatures and V_{CC} values : the test guarantees of output low current and voltage are the worst case test conditions to simulate worst case ground noise. Much better numbers could be shown, for example, in the ratio of output current to input current (I_{OL}/I_F) if both I_{OL} and I_F were measured at identical V_{CC} values and if input current was sunk into $V_F = V_{OL}$, the worst case low output level, or even into $V_F = V_{IL}$, the input threshold value. However, the test values would then guarantee only signal line noise immunity, where there is no gain associated with V_{NS}. By use of the Minimum/Maximum DC curves on Page 95 or by the Example 2 equations, limits for the single V_{CC} testing approach could be recovered. More important, each design or components engineer can develop the fanout, power, and noise margin tradeoffs for this unique application.

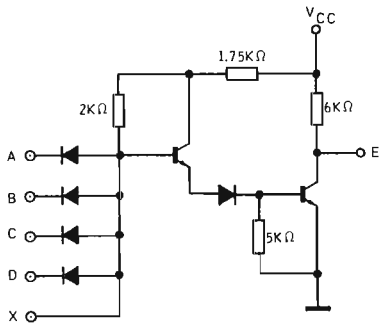


EXTENDED TEMPERATURE RANGE

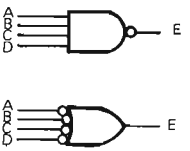
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



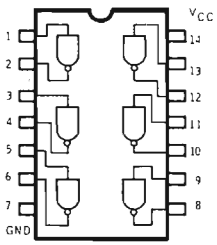
POSITIVE $E = \overline{A \cdot B \cdot C \cdot D}$
(NAND)
LOGIC

NEGATIVE $E = \overline{A + B + C + D}$
(NOR)
LOGIC

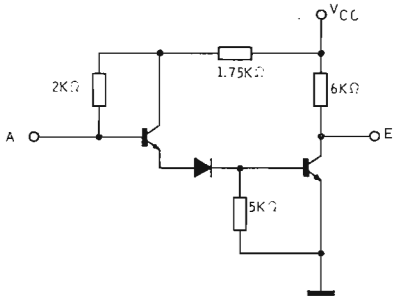
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	$V_{CC} = 4.5\ V$, $I_{OH} = -0.18\ mA$ one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OL} = 12\ mA$ inputs at V_{IH} (see below) $V_{CC} = 5.5V$, $I_{OL} = 15\ mA$ all inputs at $V_R = 5.5\ V$
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ on other inputs $V_R = 4\ V$
I_R	Input Leakage Current		2			2		5	µA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ ground on other inputs
I_{SC}	Output Short Circuit Current	-0.68	-1.33	-0.68		-1.33	-0.59	-1.33	mA	$V_{CC} = 5.5\ V$ one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					3.25			mA	$V_{CC} = 5V$ inputs open
t_{pd+}	Turn-off delay				25	80			nsec	$V_{CC} = 5\ V$ see test circuit
t_{pd-}	Turn-on delay				10	30			nsec	

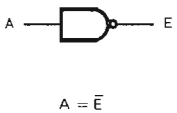
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION

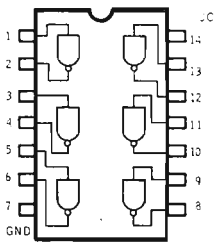


ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10 %)

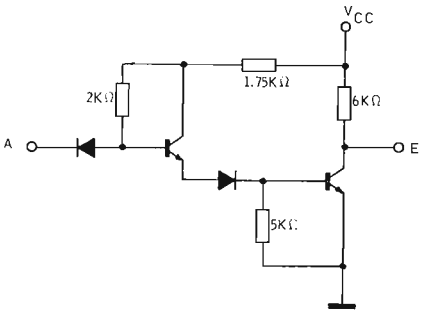
SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125° Min.	LIMITS 125° Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	V_{CC} = 4.5 V, I_{OH} = - 0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 12 mA inputs at V_{IH} (see below) V_{CC} = 5.5 V, I_{OL} = 15 mA all inputs at V_R = 5.5 V
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	V_{CC} = 5.5 V V_F = 0.4 V on other inputs V_R = 4 V
I_{SC}	Output Short Circuit Current	-0.68	-1.33	-0.68		-1.33	0.60	-1.33	mA	V_{CC} = 5.5 V one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					3.25			mA	V_{CC} = 5 V inputs open
t_{pd} +	Turn - off delay				25	50			nsec	V_{CC} = 5 V see test circuit
t_{pd} -	Turn - on delay				10	40			nsec	

NOTE : BAY-74 Diode must be connected to each gate when testing this element.

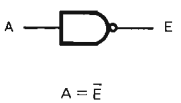
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION

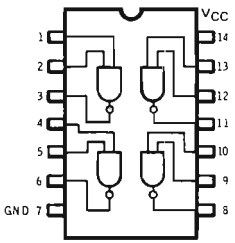


$A = \bar{E}$

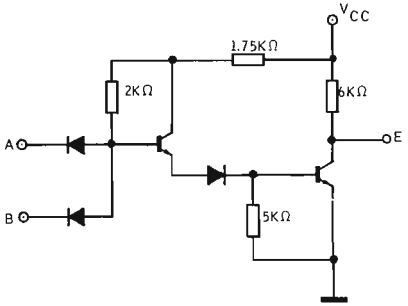
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10 %)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	V_{CC} = 4.5 V, I_{OH} = - 0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4*			0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 12 mA inputs at V_{IH} (see below) V_{CC} = 5.5V, I_{OL} = 15 mA all inputs at V_R = 5.5 V
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	V_{CC} = 5.5 V V_F = 0.4 V on other inputs V_R = 4 V
I_R	Input Leakage Current		2			2		5	µA	V_{CC} = 5.5 V V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.68	-1.33	-0.68		-1.33	-0.59	-1.33	mA	V_{CC} = 5.5 V one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					3.25			mA	V_{CC} = 5 V inputs open
t_{pd} +	Turn-off delay			25		80			nsec	V_{CC} = 5 V see test circuit
t_{pd} -	Turn-on delay			10		30			nsec	

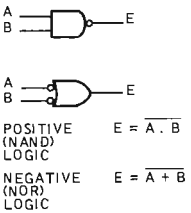
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



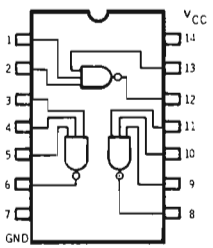
LOGIC FUNCTION



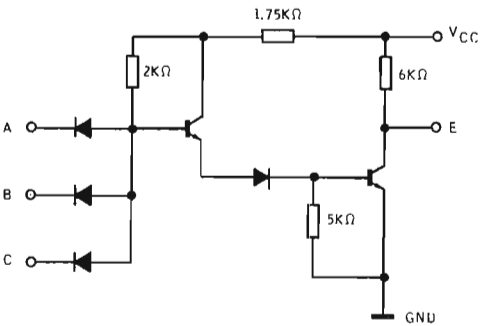
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10 %)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	V_{CC} = 4.5 V, I_{OH} = - 0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 12 mA inputs at V_{IH} (see below) V_{CC} = 5.5V, I_{OL} = 15 mA all inputs at V_R = 5.5 V
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	V_{CC} = 5.5 V V_F = 0.4 V on other inputs V_R = 4 V
I_R	Input Leakage Current		2			2		5	µA	V_{CC} = 5.5 V V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.68	-1.33	-0.68		-1.33	-0.59	-1.33	mA	V_{CC} = 5.5 V one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					3.25			mA	V_{CC} = 5 V inputs open
t_{pd+}	Turn-off delay				25	80			nsec	V_{CC} = 5 V see test circuit
t_{pd-}	Turn on delay				10	30			nsec	

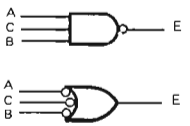
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



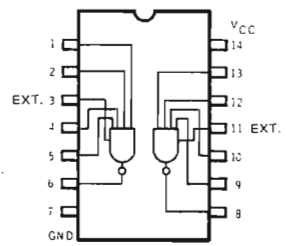
POSITIVE (NAND) LOGIC $E = \overline{A \cdot B \cdot C}$

NEGATIVE (NOR) LOGIC $E = \overline{A + B + C}$

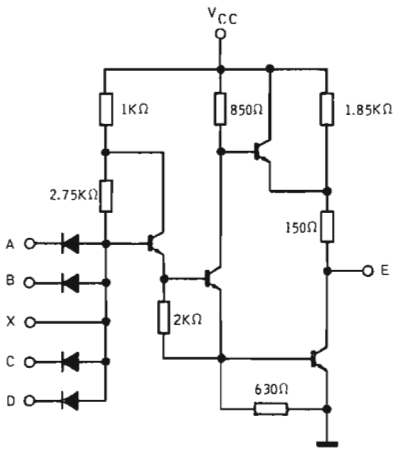
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	$V_{CC} = 4.5\ V$, $I_{OH} = -0.18\ mA$ one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OL} = 12\ mA$ inputs at V_{IH} (see below) $V_{CC} = 5.5V$, $I_{OL} = 15\ mA$ all inputs at $V_R = 5.5\ V$
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ on other inputs $V_R = 4\ V$
I_R	Input Leakage Current		2			2		5	μA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ ground on other inputs
I_{SC}	Output Short Circuit Current	-0.68	-1.83	-0.68		-1.33	-0.59	-1.33	mA	$V_{CC} = 5.5\ V$ one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					3.25			mA	$V_{CC} = 5\ V$ inputs open
t_{pd+}	Turn-off delay			25		80			nsec	$V_{CC} = 5\ V$ see test circuit
t_{pd-}	Turn-on delay			10		30			nsec	

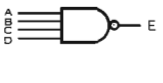
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



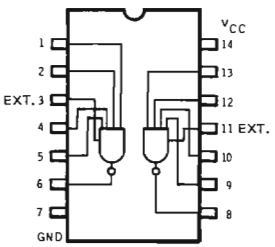
POSITIVE $E = \overline{A \cdot B \cdot C \cdot D}$
(NAND)
LOGIC

NEGATIVE $E = \overline{A+B+C+D}$
(NDR)
LOGIC

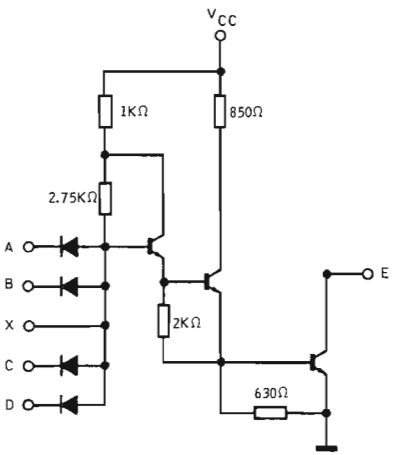
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS 55°C Min.	55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	$V_{CC} = 4.5\ V$ $I_{OH} = -2$ @ -55°C, inputs $= -2.5$@25°C at V_{IL} $= -4$ @125°C (see below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OL} = 36$ mA inputs at V_{IH} (see below) $V_{CC} = 5.5\ V$ $I_{OL} = 37.5$ mA all inputs at 5.5 V
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ on other inputs $V_R = 4\ V$
I_R	Input Leakage Current		2			2		5	μA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ ground on other inputs
I_{SC}	Output Short Circuit Current	16		18			16		mA	$V_{CC} = 5.5\ V$ one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)					13.3			mA	$V_{CC} = 5\ V$ inputs open
t_{pd+}	Turn-off delay			25		80			nsec	$V_{CC} = 5\ V$ see test circuit
t_{pd-}	Turn - on delay			15		40			nsec	$V_{CC} = 5\ V$ see test circuit

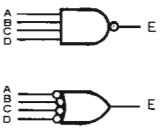
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



POSITIVE $E = \overline{A \cdot B \cdot C \cdot D}$
(NAND)
LOGIC

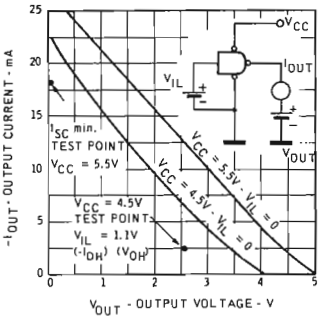
NEGATIVE $E = \overline{A+B+C+D}$
(NOR)
LOGIC

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

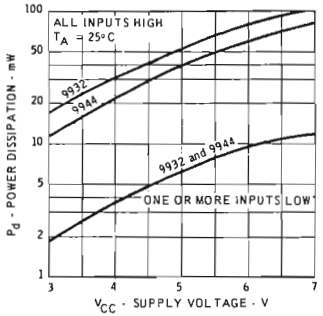
SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OL} = 36\ mA$ inputs at V_{IH} (see below) $V_{CC} = 5.5\ V$ $I_{OL} = 40.5\ mA$ all inputs at $V_R = 5.25\ V$
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ on other inputs $V_R = 4\ V$
I_R	Input Leakage Current		2			2		5	µA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ Ground on other inputs
I_{CEX}	Output Leakage Current		50			100		200	µA	$V_{CC} = 4.5\ V$ one input grounded, output at V_{CC}
I_{PD}	Power Dissipation Current (each gate)					10			mA	$V_{CC} = 5\ V$ inputs open
t_{pd+}	Turn - off delay				15	50			nsec	$V_{CC} = 5\ V$ see test circuits
t_{pd-}	Turn - on delay				10	35			nsec	

MINIMUM - MAXIMUM AND TYPICAL DC CURVES

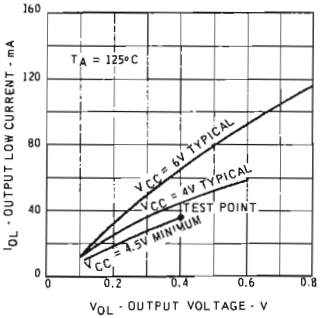
OUTPUT CURRENT WITH INPUTS LOW (9932)



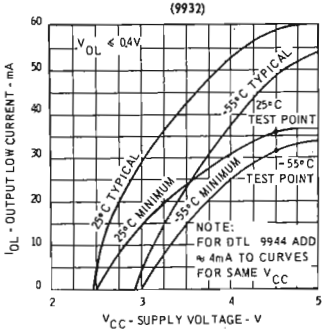
POWER DISSIPATION PER SIDE VS. SUPPLY VOLTAGE (OUTPUT NOT LOADED) (9932, 9944)



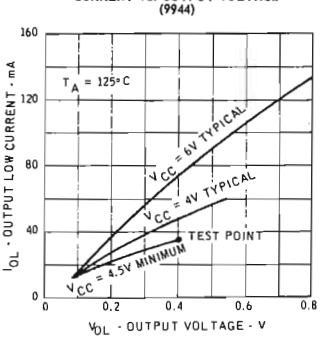
OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE (9932)



OUTPUT LOW CURRENT VS. SUPPLY VOLTAGE (9932)



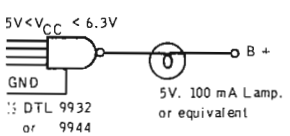
OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE (9944)



MISCELLANEOUS APPLICATIONS

LAMP DRIVING

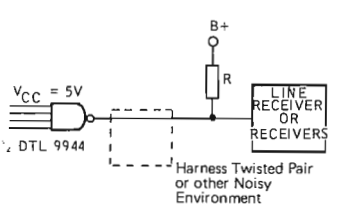
SUGGESTED RATINGS	DIP	FLAT
Power Dissipation	400 mW	240 mW
Max Hot Lamp Current one side only ON	120 mA	100 mA
Max Hot Lamp Current both sides ON	90 mA	75 mA



"Cold" lamp current is limited by saturation resistance, emitter resistance, and base current to about 200 to 250 mA. Most significant thermal time constants for 9932 and 9944 : DIP 50 msec Flat 100 msec.
Thermal time constant is measured by forward diode drop in one gate with power pulsed into opposite gate.

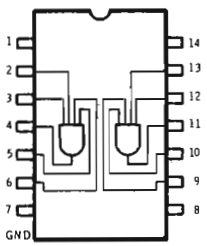
INTERFACING

B + up to 12 volts. Line Receiver may have nominal low level of 1 volt; nominal threshold ≈ 4 V and nominal high level 8 V, for example. Resistor selected should be as low as possible consistent with required low input level of receiver, number of receivers, and power dissipation of system For guaranteed operation in both applications the use of selected units is desirable. Operation as a lamp driver requires high gain units, and for interfacing high voltage units may ba required.

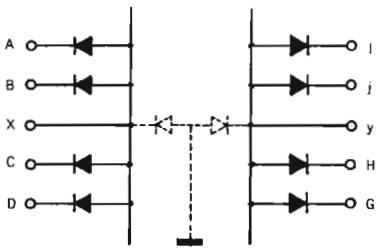


EXTENDED TEMPERATURE RANGE

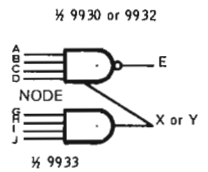
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



LOGIC FUNCTION



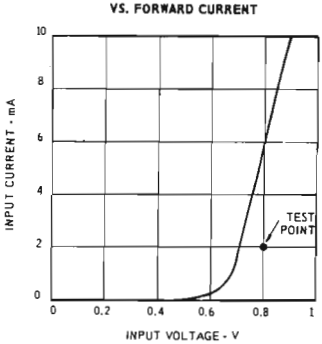
POS. LOGIC $E = \overline{A \cdot B \cdot C \cdot D \cdot G \cdot H \cdot I \cdot J}$

NEG. LOGIC $E = \overline{A + B + C + D + G + H + I + J}$

ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{FD}	Forward Drop Voltage	0.84	0.98	0.70	0.82	0.48	0.62	V	$I_{FD} = 2$ mA applied to output, input grounded
I_R	Reverse Current		2		2		5	μA	$V_R = 4$ V, ground on other inputs
I_R	Output Reverse Current		10		10		25	μA	$V_R = 4$ V on output

FORWARD VOLTAGE VS. FORWARD CURRENT

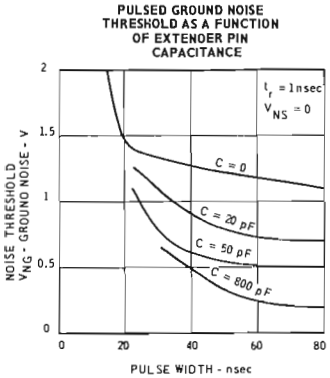


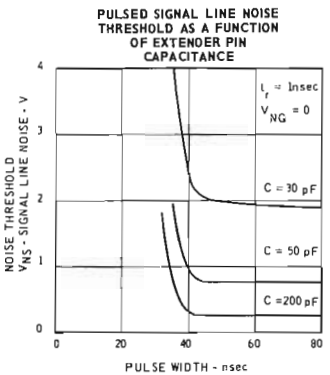
FAN-IN EXTENSION

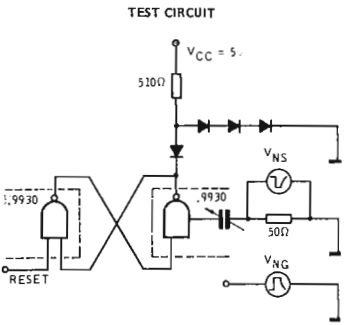
DTL 9933 elements may be used to extend fan-in capability to more than 20 without adversely affecting the noise immunity or load driving capability of the element to which they are connected.
Good practice dictates that extension interconnection paths be as short as possible to minimize the effects of distributed capacitance on circuit performance. The effects of capacitance are summarized on the back page. Typical input capacitance of DTL 9933 is 2 pF and output capacitance is 5 pF.

EXTENDED TEMPERATURE RANGE

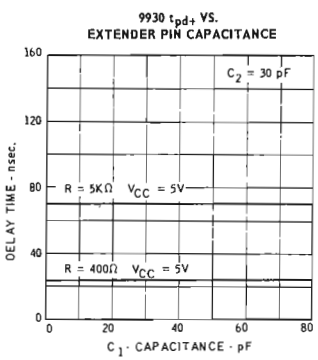
TYPICAL CURVES TO SHOW THE EFFECTS OF EXTENDER PIN CAPACITANCE ON NOISE THRESHOLD OF DTL 9930 DUAL GATE

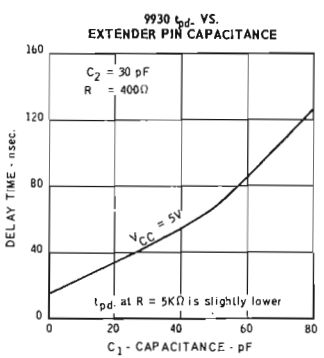


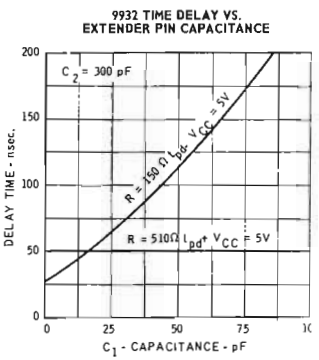


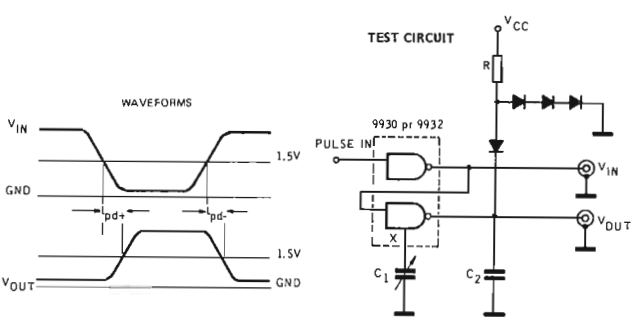


TYPICAL CURVES TO SHOW THE EFFECTS OF EXTENDER PIN CAPACITANCE (Using DTL 9933) ON TIME DELAY OF DTL 9930 DUAL GATE AND DTL 9932 DUAL BUFFER





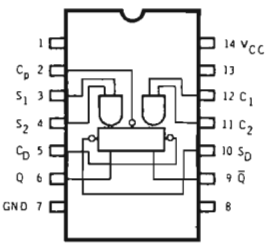




C_1 represents the sum of the DTL 9933 Dual Extender Element output capacitances (~ 5 pF per output) and associated board, connector and wiring capacitances.

CONNECTION DIAGRAM

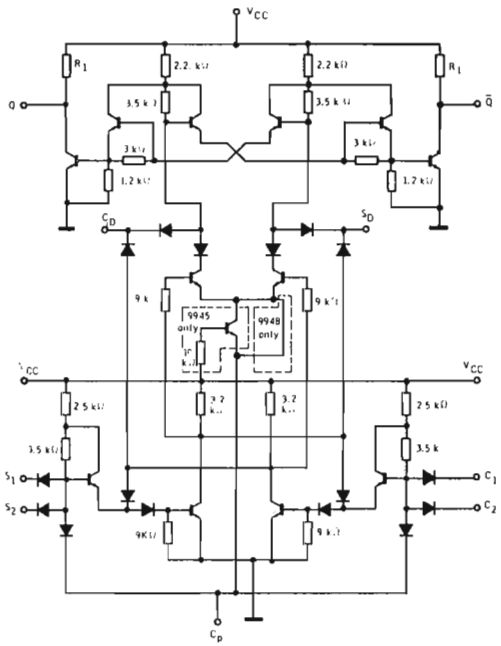
(top view)



NOTE: The DTL 9945 incorporates the standard 6KΩ output pull-up resistor, while the DTL 9948 features a 2kΩ output pull-up resistor for improved switching times, thus reducing however the drive capability.

Note :
DTL 9945 - $R_1 = 6k\Omega$
DTL 9948 - $R_1 = 2k\Omega$

SCHEMATIC DIAGRAM



LOGIC FUNCTION

Synchronous Entry					Asynchronous Entry				J - K Mode Truth Table			
Inputs				Outputs	Inputs		Outputs		Inputs		Outputs	
t_n				$t_n + 1$					t_n		$t_n + 1$	
S_1	S_2	C_2	C_1	Q	C_D	S_D	Q	$\bar{Q}$	S_1	C_1	Q	$\bar{Q}$
L	X	L	X	NC	H	H	NC	NC	L	H	L	H
L	X	X	L	NC	H	L	H	L	H	L	H	L
X	L	L	X	NC	L	H	L	H	H	H	$\bar{Q}_n$	Q_n
X	L	X	L	NC	L	L	H	H	L	L	Q_n	$\bar{Q}_n$
L	X	H	H	L								
X	L	H	H	L					For J - K Mode Operation :			
H	H	L	X	H					Connected 4 to 9 and 11 to 6.			
H	H	X	L	H								
H	H	H	H	Undeter-mined								

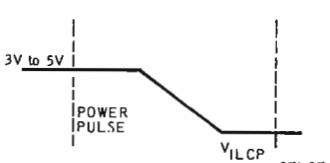
NOTES :

1) Abbreviation used in the body of tables :
   L = low, the more negative voltage level
   H = high, the more positive voltage level (In all cases, unused pins have the same effect as high).
   X = immaterial, either H or L has equal effect
   NC = no chenge , the clock pulse has no effect on outputs
   Q_n = outputs state at time t_n
2) The L symbol in the S and C input column is defined as meaning that the input does not go high at any time while the clock is high . The H symbol in the S and C input column is defined as meaning that the input is high at same time while the clock is high.

9945 ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	V_{CC} = 4.5 V, I_{OH} = -0.18 mA V_{IL} (see below) on proper asynchronous input
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 12 mA V_{CC} = 5.5 V I_{OL} = 15 mA V_{IH} (see below) on proper asynchronous input
V_{IH}	Input High Voltage	2.1		1.9		1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4		1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	S & C Inputs Load Current		-0.98		-0.98		-0.92	mA	V_{CC} = 5.5 V V_F = 0.4 V V_R = 4 V on other inputs
I_{FS}	S_D, C_D Inputs Load Current		-2.93		-2.93		-2.57	mA	V_{CC} = 5.5 V V_F = 0.4 V V_R = 4 V on other inputs
I_{FCP}	Clock Input Load Current		-2.93		-2.93		-2.57	mA	V_{CC} = 5.5 V V_F = 0.4 V V_{IL} on S_D
I_R	S, C, S_D, C_D Inputs Leakage Current		2		2		5	µA	V_{CC} = 5.5 V V_R = 4 V ground on other inputs
I_{RCP}	Clock Input Leakage Current		10		10		20	µA	V_{CC} = 4 V V_R = 4 V S and C_D inputs grounded
I_{PD}	Power Dissipation Current				14			mA	V_{CC} = 5 V
I_{SC}	Output Short Circuit Current	-0.70	-1.33	-0.70	-1.33	-0.63	-1.30	mA	V_{CC} = 5.5 V high output grounded
t_{pd+}	Turn-off delay			35	75			nsec	V_{CC} = 5 V see test circuit
t_{pd-}	Turn-on delay			30	75			nsec	

CLOCK PULSE DESCRIPTION



V_{ILCP} = 1 V @ 25° C
= 0V @ -55° C and 125° C

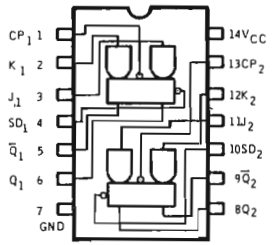
9948 ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10 %)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		- 55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	V_{CC} = 4.5 V I_{OH} = - 0.54 mA V_{IL} (see below) on proper asynchronous input
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 13 mA V_{CC} = 5.5 V I_{OL} = 13.6 mA V_{IH} (see below) on proper asynchronous input
V_{IH}	Input High Voltage	2		1.9		1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4		1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	S & C Inputs Load Current		-0.98		-0.98		-0.92	mA	V_{CC} = 5.5 V V_F = 0.4 V on other inputs V_R = 4 V
I_{FS}	C_D, S_D Input Load Current		-2.93		-2.93		-2.57	mA	V_{CC} = 5.5 V V_F = 0.4 V
I_{FCP}	Clock Input Load Current		-2.35		-2.35		-2.03	mA	V_{CC} = 5.5 V V_F = 0.4 V V_{IL} on S_D
I_R	S, C, S_D, C_D Inputs Leakage Current		2		2		5	µA	V_{CC} = 5.5 V V_R = 4 V ground on other inputs
I_{RCP}	Clock Input Leakage Current		10		10		20	µA	V_{CC} = 4 V V_R = 4 V S and C_D inputs grounded
I_{PD}	Power Dissipation Current				16.2			mA	V_{CC} = 5 V
I_{SC}	Output Short Circuit Current	-2.10	-3.96	-2.10	-3.96	-1.86	-3.54	mA	V_{CC} = 5.5 V high output grounded
t_{pd} +	Turn off delay			30	65			nsec	V_{CC} = 5 V see test circuit
t_{pd} -	Turn on delay			30	75			nsec	

CLOCK PULSE DESCRIPTION : SEE 9945

NOTE : The DTL 9093 and 9094 are respectively dual DTL 9945 and 9948 flip-flops.

CONNECTION DIAGRAM
(top view)



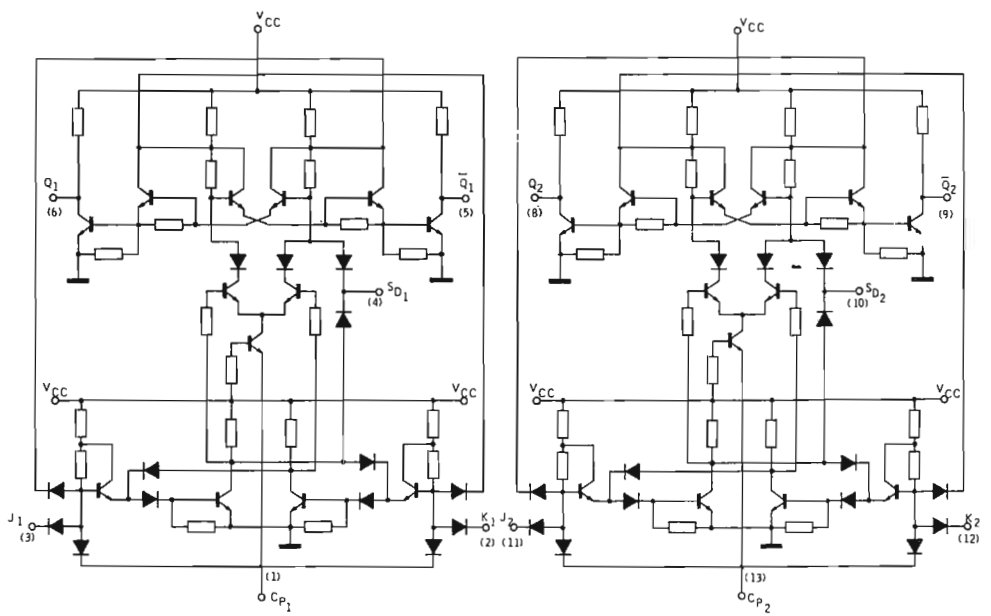
LOGIC FUNCTION

Asynchronous Entry			J-K Mode Truth Table			
Input	Outputs		Inputs		Outputs	
			t_n		$t_n + 1$	
4 (10)	6 (8)	5 (9)	3 (11)	2 (12)	6 (8)	5 (9)
H	NC	NC	L	H	L	H
L	H	L	H	L	H	L
			H	H	$\bar{Q}_n$	Q_n
			L	L	Q_n	$\bar{Q}_n$

NOTES :

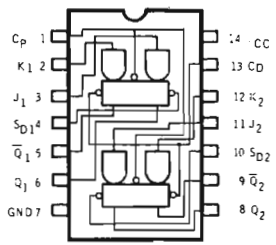
1) Abbreviations used in the body of tables :
   L = low, the more negative voltage level
   H = high, the more positive voltage level
   (In all cases, unused pins have the same effect as high).
   NC = no change, the clock pulse has no effect on outputs.
   Q_n = outputs state at time t_n
2) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is high.
   The H symbol in the J and K input column is defined as meaning that the input is high at same time while the clock is high.

SCHEMATIC DIAGRAM 9093/9094 (9093 SHOWN)



)TE : The DTL 9097 and 9099 are respectively dual DTL 9948 and 9945 flip-flops.

CONNECTION DIAGRAM
(top view)



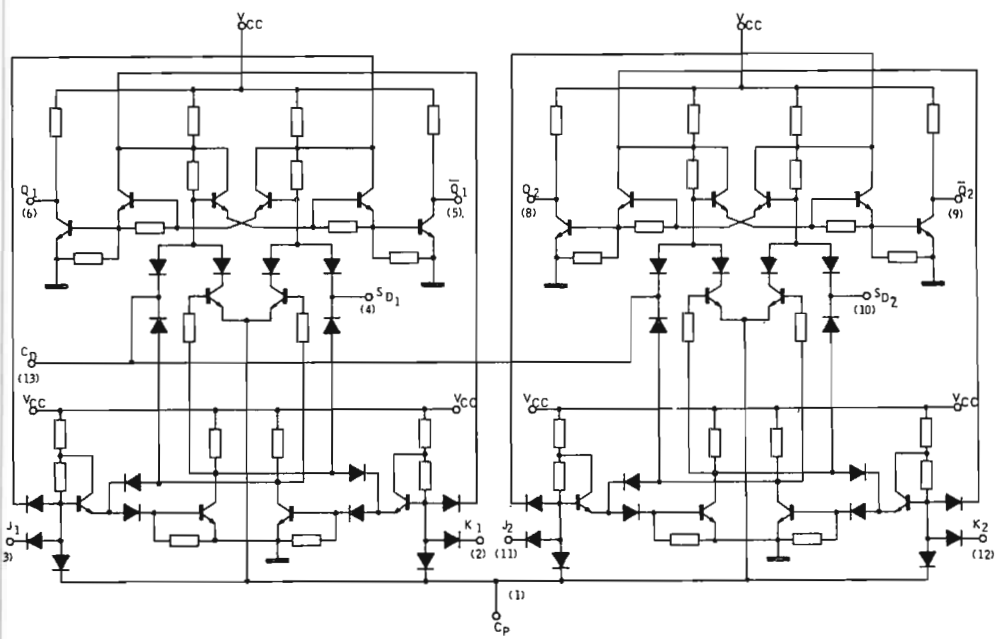
LOGIC FUNCTION

Asynchronous Entry				J-K Mode Truth Table			
Inputs		Outputs		Inputs		Outputs	
				t_n		$t_n + 1$	
13	4 (10)	6 (8)	5 (9)	3 (11)	2 (12)	6 (8)	5 (9)
H	H	NC	NC	L	H	L	H
H	L	H	L	H	L	H	L
L	H	L	H	H	H	$\overline{Q}_n$	Q_n
L	L	H	H	L	L	Q_n	$\overline{Q}_n$

NOTES :

1) Abbreviation used in the body of tables :
   L = low, the more negative voltage level
   H = high, the more positive voltage level
   (In all cases, unused pins have the same effect as high).
   NC = no change, the clock pulse has no effect on outputs.
   Q_n = outputs state at time t_n
2) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is high.
   The H symbol in the J and K input column is defined as that meaning the input is high at same time while the clock is high.

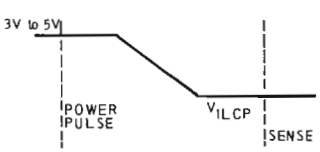
CHEMATIC DIAGRAM 9097/9099 (9097 SHOWN)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	V_{CC} = 4.5 V I_{OH} = -0.18 mA V_{IL} (see below) and V_R = 4 V on asynchronous inputs
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 13.8 mA V_{CC} = 5.5 V I_{OL} = 15 mA Ground and V_R = 4 V on asynchronous inputs
V_{IL}	Input Low Voltage		1.4		1.1		0.8	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2.1		1.9		1.7		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current J and K Inputs		-0.98		-0.98		-0.92	mA	V_{CC} = 5.5 V V_F = 0.4 V
I_{FCP}	Clock Input Load Current 9093 9099		 -2.93 -5.86		 -2.93 -5.86		 -2.57 -5.14	mA	V_{CC} = 5.5 V V_F = 0.4 V V_{IL} (see above) on asynchronous input
I_{FS}	Set Input Load Current		-2.2		-2.2		-1.93	mA	V_{CC} = 5.5 V V_F = 0.4 V ground on J inputs
I_{FC}	Clear Input Load Current		-4.40		-4.40		-3.86	mA	V_{CC} = -5.5 V V_F = 0.4 V Ground on K inputs
I_R	Input Leakage Current J and K Inputs		2		2		5	µA	V_{CC} = 5.5 V V_R = 4 V Ground on clock
I_{RS}	Set Input Leakage Current		2		2		5	µA	V_{CC} = 5.5 V V_R = 4 V Ground on K inputs
I_{RC}	Clear Input Leakage Current		4		4		10	µA	V_{CC} = 5.5 V V_R = 4 V Ground on J inputs
I_{RCP}	Clock Input Leakage Current 9093 9099		 10 20		 10 20		 20 40	µA	V_{CC} = 4 V V_R = 4 V Ground on J inputs
I_{SC}	Output Short Circuit Current	-0.70	-1.33	0.70	-1.33	-0.63	-1.30	mA	V_{CC} = 5.5 V High output grounded
I_{PD}	Power Dissipation Current				28			mA	V_{CC} = 5 V
t_{pd+}	Turn-off delay			35	75			nsec	V_{CC} = 5 V
t_{pd-}	Turn-on delay			30	75			nsec	see test circuit

CLOCK PULSE DESCRIPTION :



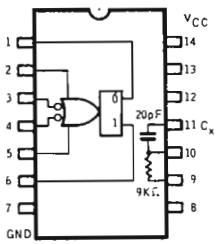
V_{ILCP} = 1 V @ 25° C
= 0V @ -55° C and 125° C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%)

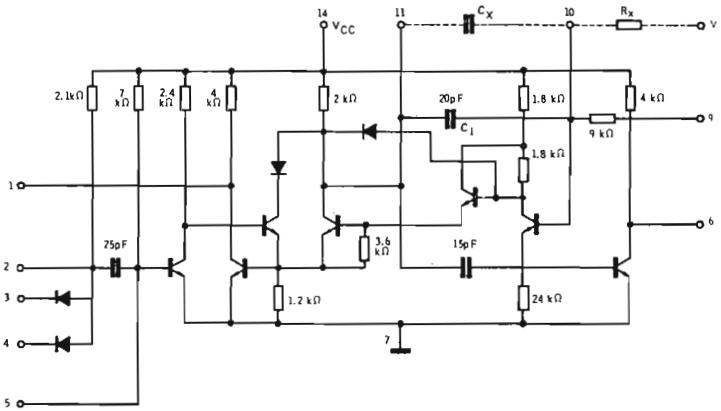
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min. Max.		
V_{OH}	Output High Voltage	2.5		2.6			2.5	V	V_{CC} = 4.5 V I_{OH} = -0.54 mA V_{IL} (see below) and V_R = 4 V on asynchronous inputs
V_{OL}	Output Low Voltage		0.4			0.4	0.4	V	V_{CC} = 4.5 V I_{OL} = 12.3 mA V_{CC} = 5.5 V I_{OL} = 13.6 mA Ground and V_R = 4 V on asynchronous inputs
V_{IH}	Input High Voltage	2.1		1.9			1.7	V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1	0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current J and K Inputs		-0.98			-0.98	-0.92	mA	V_{CC} = 5.5 V V_F = 0.4 V
I_{FCP}	Clock Input Load Current 9094 9097		-2.35 -4.68			-2.35 -4.68	-2.03 -4.04	mA	V_{CC} = 5.5 V V_F = 0.4 V V_{IL} (see above) on asynchronous input
I_{FS}	Set Input Load Current		-2.2			-2.2	-1.93	mA	V_{CC} = 5.5 V V_F = 0.4 V Ground on J input
I_{FC}	Clear Input Load Current		4.4			4.4	3.86	mA	V_{CC} = 5.5 V V_F = 0.4 V Ground on K inputs
I_R	Input Leakage Current J and K Inputs		2			2	5	µA	V_{CC} = 5.5 V V_R = 4 V Ground on clock
I_{RCP}	Clock Input Leakage Current 9094 9097		10 20			10 20	20 40	µA	V_{CC} = 4 V V_R = 4 V Ground on J inputs
I_{RS}	Set Input Leakage Current		2			2	5	µA	V_{CC} = 5.5 V V_R = 4 V Ground on K inputs
I_{RC}	Clear Input Leakage Current		4			4	10	µA	V_{CC} = 5.5 V V_R = 4 V Ground on J inputs
I_{SC}	Output Short Circuit Current	-2.1	-3.96	-2.1		-3.96	-1.86 -3.54	mA	V_{CC} = 5.5 V High output grounded
I_{PD}	Power Dissipation Current					32.4		mA	V_{CC} = 5 V
t_{pd+}	Turn-off delay			30		65		nsec	V_{CC} = 5 V see test circuit
t_{pd-}	Turn-on delay			30		75		nsec	

CLOCK PULSE DESCRIPTION : **SEE 9093 - 9099**

LOGIC DIAGRAM
(top view)



SCHEMATIC DIAGRAM



GENERAL DESCRIPTION :

The DTL 9951 Monostable Multivibrator provides complementary output pulses which are typical 100 nsec wide. This pulse width is adjustable by the addition of external discrete passive components.
The output pulse width is very stable as either V_{CC} or temperature (or both) is varied when an external timing resistor is used instead of the interna diffused resistor.

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired) (1)

Output Current, into outputs	50 mA
Current into Pin 10	5 mA

NOTE: 1) In addition to abs. max. rating, pag. 87

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

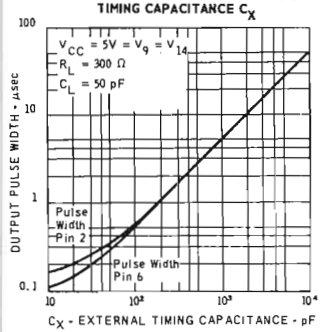
SYMBOL	CHARACTERISTICS	LIMITS - 55°C Min.	LIMITS - 55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.5			2.5		V	$V_{CC} = 4.5\ V$ $I_{OH} = -0.18$ mA Pin 2 grounded, Pin 9 at V_{CC}
V_{OL}	Output Low Voltage		0.4		0.4			0.45	V	$V_{CC} = 4.5\ V$ $I_{OL} = 15$ mA $V_{CC} = 5.5\ V$ $I_{OL} = 15$ mA when testing Pin 1, ground Pin 10 when testing Pin 6, V_{CC} on Pin 9
I_F	Input Load Current		-3.2		-3.2			-3	mA	$V_{CC} = 5.5\ V$ $V_F = 0\ V$ $V_R = 4\ V$
I_R	Input Leakage Current		5		5			10	µA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ Ground on Pin 2
I_{PD}	Power Dissipation Current				9				mA	$V_{CC} = 5\ V$ inputs grounded, V_{CC} on Pin 9
t_{pd+}	Turn-off delay (Pin 6)				40				nsec	$V_{CC} = 5\ V$ see test circuit
t_{pd-}	Turn-on delay (Pin 1)				40				nsec	
P_W	Pulse width (Pin 1)			90	220				nsec	
P_W	Pulse width (Pin 6)			70	160				nsec	

RULES FOR USE OF DTL 9951

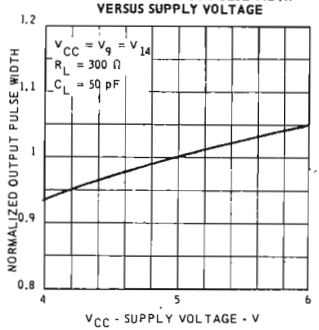
1) With Pin 9 connected to V_{CC} and no external capacitor (C_X), the output pulse width is approximately 150 nsec.
2) With Pin 9 connected to V_{CC} and an external capacitor (C_X) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5 (C_X + 20)$ with C_X in pF and T in nsec.
3) For improved pulse width control, Pin 9 is left open and a stable external resistor (R_X) of 9 kΩ minimum to 15 kΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression : $T \approx 0.5 R_X (C_X + 20)$ with R_X in kΩ, C_X in pF and T in nsec.
4) The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2 kΩ resistor between Pin11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5) The maximum input fall time to trigger : 15 nsec for a 1.4 volt swing; 40 nsec for a 2.4 volt swing; 80 nsec for a 4.4 volt swing.
6) The AC sensitivity of the inputs may be decreased by connecting a capacitor between Pin 5 and ground.
7) The minimum pulse width at output Pin 1 is approximately 100 nsec. This pulse width may be decreased to 50 nsec by connecting a 10 kΩ resistor between Pin 5 and V_{CC}.

TIMING CHARACTERISTICS

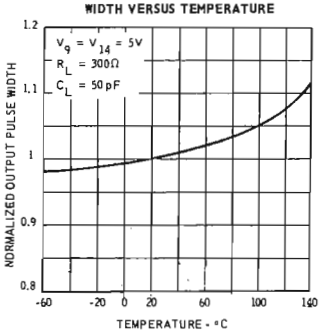
OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X



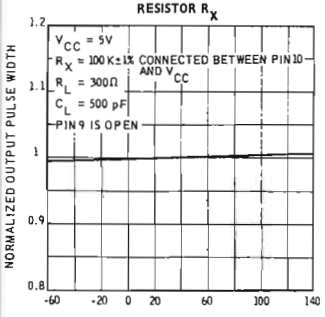
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



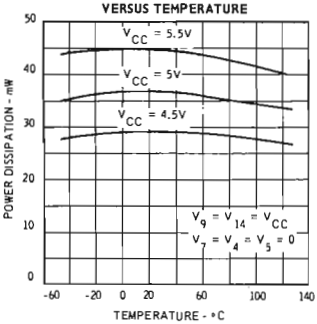
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE



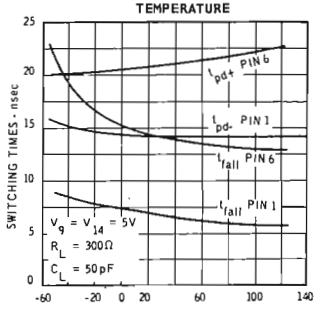
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE USING EXTERNAL TIMING RESISTOR R_X



POWER DISSIPATIDN VERSUS TEMPERATURE

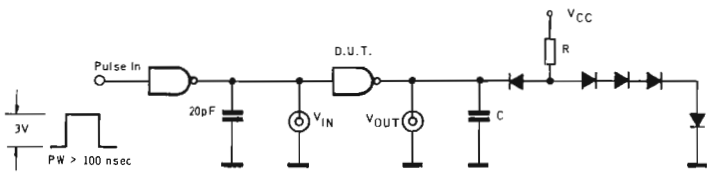


SWITCHING TIMES VERSUS TEMPERATURE



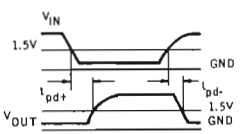
SWITCHING TIME TEST CIRCUITS

9930 - 9936 - 9948 - 9962 GATES t_{pd} TEST CIRCUIT



All diodes BAY 74 or equivalent
V_{CC} at PIN 14, GND at PIN 7

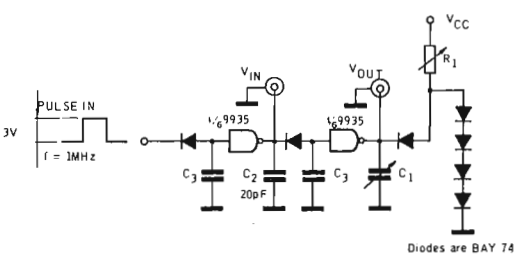
WAVEFORMS



TEST CONDITIONS

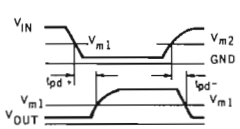
	R	C
t_{pd+}	3.9 k Ω	30 pF
t_{pd-}	400 Ω	50 pF

9935 GATE t_{pd} TEST CIRCUIT



Diodes are BAY 74

WAVEFORMS



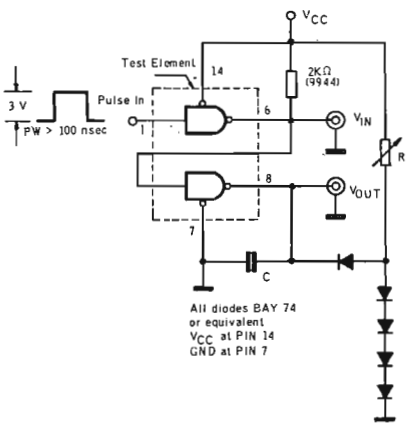
V_{m1}	V_{m2}
1.5 V	1.3 V

TEST CONDITIONS

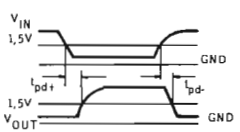
	R_1	C_1	C_2	C_3
t_{pd+}	3.9 K Ω	30pF	20pF	5pF
t_{pd-}	400 Ω	50pF	20pF	5pF

SWITCHING TIME TEST CIRCUITS

9932 - 9944 GATES t_{pd} TEST CIRCUIT



WAVEFORMS

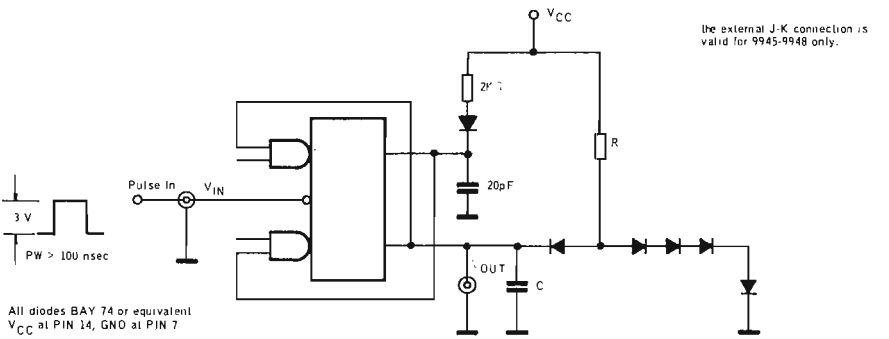


TEST CONDITIONS

	R	C
9944 t_{pd+}	510Ω	20pF
9944 t_{pd-}	150Ω	100pF
9932 t_{pd+}	510Ω	500pF
9932 t_{pd-}	150Ω	500pF

SWITCHING TIME TEST CIRCUITS

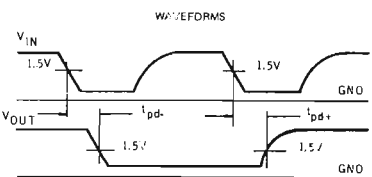
9945 · 9948 · 9093 · 9094 · 9097 · 9099 FLIP-FLOPS t_{pd} TEST CIRCUIT



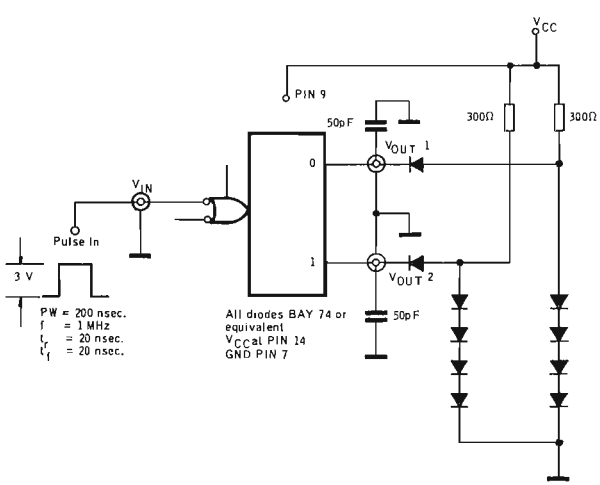
TEST CONDITIONS

	R	C
t_{pd+}	2K Ω	30pF
t_{pd-}	330 Ω	50pF

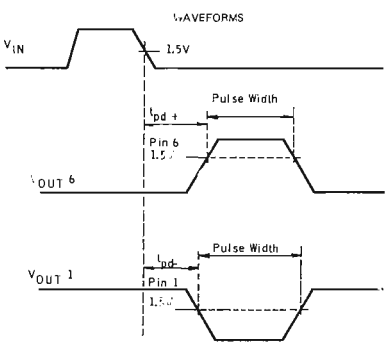
WAVEFORMS



9951 MONOSTABLE t_{pd} TEST CIRCUIT



WAVEFORMS



Diode-transistor logic

STANDARD TEMPERATURE RANGE 0°C ÷ 75°C

- COMPATIBLE WITH TTL, LPDTL PRODUCTS
- NOISE IMMUNITY 1 V
- OUTPUT DRIVE CAPABILITY OF 10
- POWER DISSIPATION 8.5mW PER GATE
- FAN-IN EXPANSION CAPABILITY
- WIRED-OR CAPABILITY
- SAME PIN CONFIGURATION AS THE CORRESPONDING TTL AND LPDTL PRODUCTS

The SGS Diode-Transistor Logic (DTL) family consists of a set of compatible integrated circuits designed for medium power, medium speed applications.
The circuits are fabricated within a silicon monolithic substrate using the standard planar epitaxial process.
These devices are available in the following packages: dual in-line ceramic package, dual in-line plastic package, flat ceramic package.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage (V_{CC}), Continuous	8 V
Supply Voltage (V_{CC}), Pulsed < 1 sec.	12 V
Output Current, Into Outputs	
DTL 9932 - 9944	100 mA
Other Elements	30 mA
Input Forward Current	-10 mA
Input Reverse Current	1 mA
Storage Temperature, Plastic	-55°C to 125°C
Storage Temperature, Ceramic	-65°C to 150°C
Temperature (Amb.) Under Bias, Ceramic	-55°C to 125°C

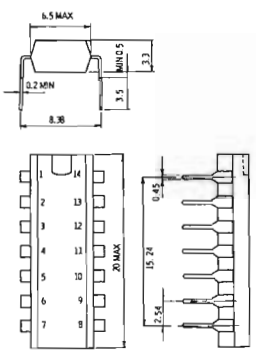
OPERATING CONDITIONS

Temperature Range	0° to 75°C
Supply Voltage	5 V ± 5%

ORDERING NUMBERS

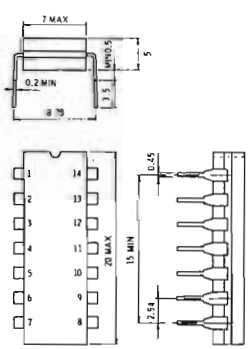
U6A XXXX 59X (for ceramic DIP; XXXX is type number)
U7A XXXX 59X (for plastic DIP; XXXX is type number)
U31 XXXX 59X (for flat package; XXXX is type number)

PHYSICAL DIMENSIONS
14-pin plastic DIP



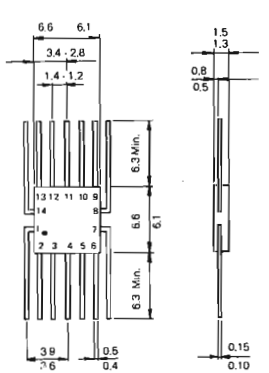
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
14-pin ceramic DIP



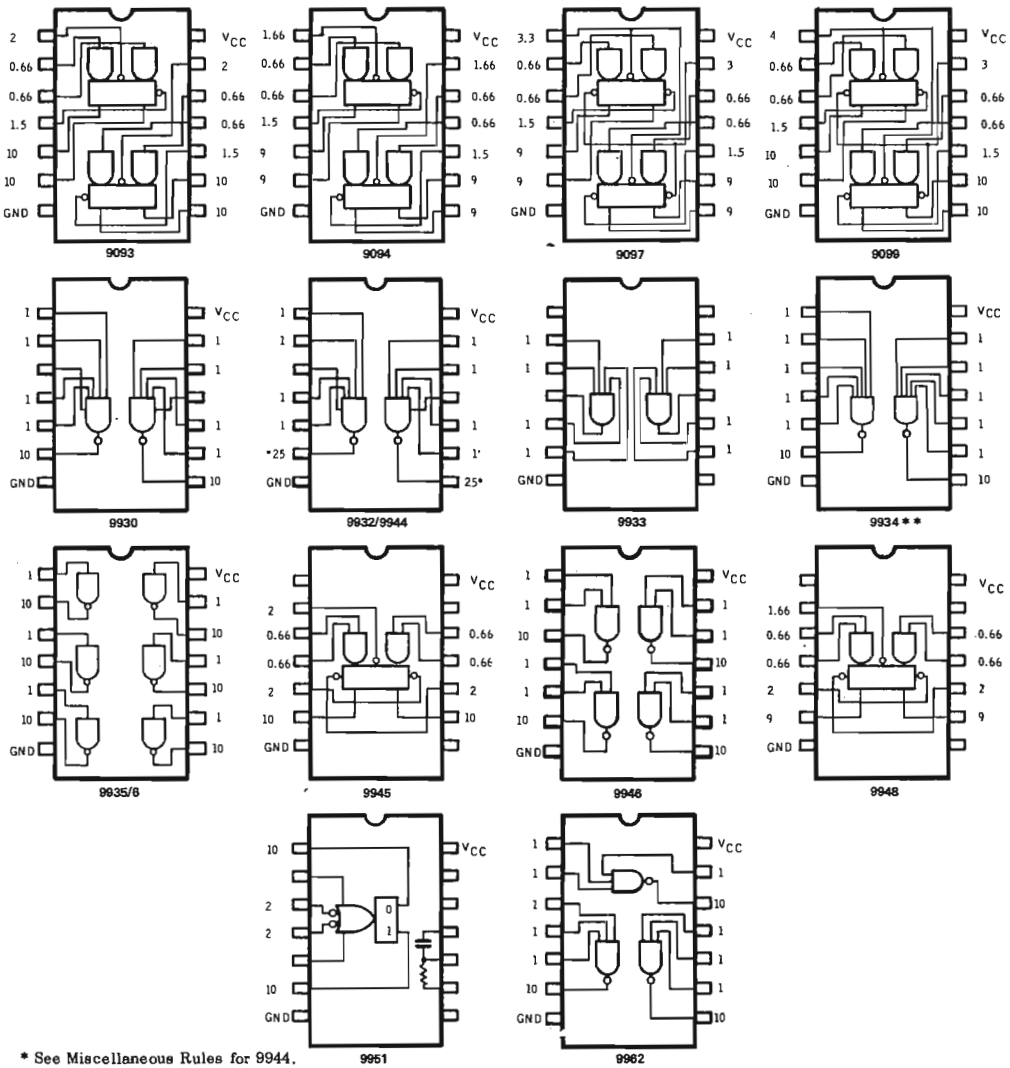
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
Flat package



NOTE : All dimensions in mm.

INPUT - OUTPUT LOAD/DRIVE FACTORS



* See Miscellaneous Rules for 9944.
** Plastic DIP only.

MISCELLANEOUS RULES

The number of elements driven by an output terminal may consist of any combination of elements whose sum of input load factors does not exceed the output drive factor.
An external resistor should be used with 9944. With an external resistor R the following output drive factors will be obtained:

R = 6 KΩ	Drive Factor = 26
R = 2 KΩ	Drive Factor = 25
R = 1 KΩ	Drive Factor = 23
R = 510Ω	Drive Factor = 20

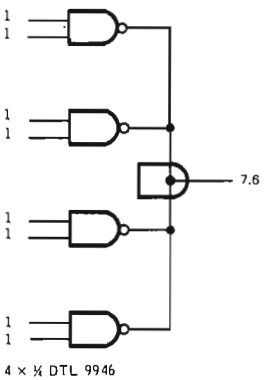
For increased output drive, the inputs and outputs of 1/2 DTL 9944 may be paralleled, up to 4 common outputs. For 4 paralleled elements:

each combined input, load factor = 4
each combined output, drive factor = 100 (R = 2 KΩ)

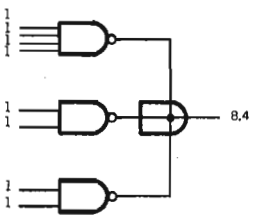
"WIRED OR" CONNECTION

1. Outputs of DTL gates may be tied together for the "wired OR" function:
   $(\overline{ABCD} \cdot \overline{GHIJ} = \overline{ABCD + GHIJ})$. Subtract, for each added gate, 0.8 unit load from output drive factor.
2. Outputs of DTL 9932 may not be tied together for the "wired OR" function.

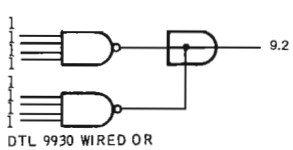
"WIRED OR" Examples:



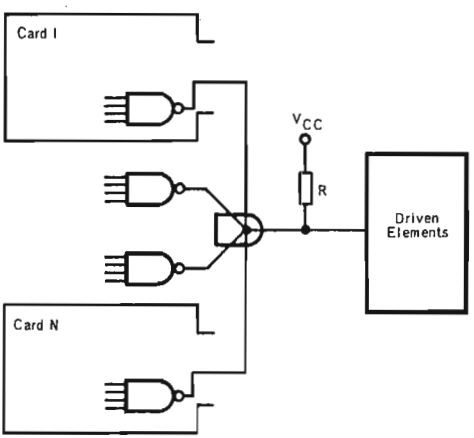
4 × ¼ DTL 9946



½ 9930 and
2 x ¼ 9946



DTL 9930 WIRED OR



Each output driver is 1/2 DTL 9944. Note that the DTL 9944 is a direct high fan-out replacement for DTL 9930, except that an external resistor must be used. The F.O. will be the same as one 1/2 DTL 9944 buffer used with that resistor.

DELAY TIME PERFORMANCE INTO CAPACITIVE LOADS

Most delay attributable to capacitive loads is associated with the positive going output. Two RC time constants are seen in the positive going output. In the 1st time period, from the saturated low level to threshold, the R of the RC time constant can be given by 6 KΩ in parallel with $\frac{3.75\ K\Omega}{\text{active fanout}}$.

Above the threshold which occurs at about 1.4 to 1.5 volts at 25°C, the R of the 2nd RC time constant is 6 kΩ and the rate of the voltage rise above threshold is slow. The logic signal propagates through at the threshold level, so voltage rise above threshold does not affect speed. By noting that both rise domains drive toward V_{CC}, the voltage rise waveform may be calculated. DTL gate inputs are ~ 2 pf per input for active or inactive fanout; the remaining capacitance is from board, wiring, and connectors.

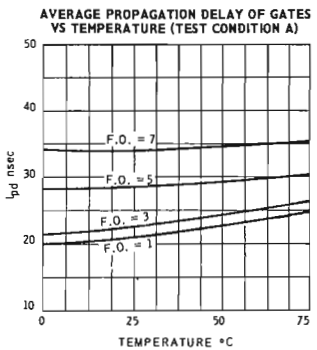


FIG. 1

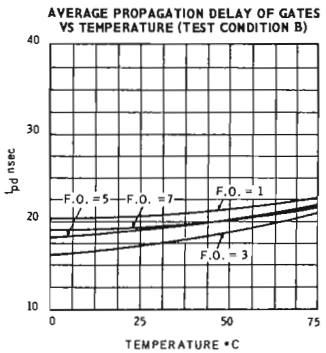
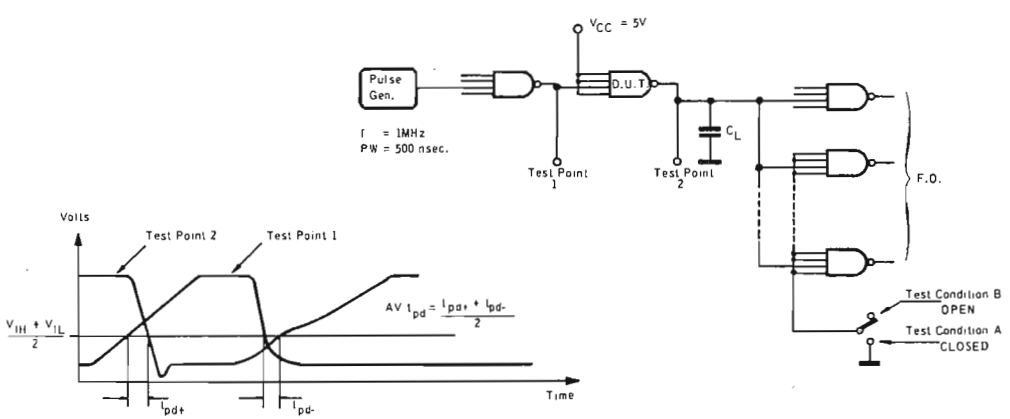


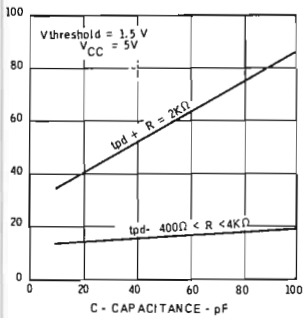
FIG. 2

TEST CONDITIONS FOR FIG. 1 AND 2

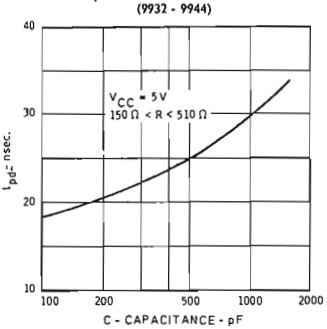


d CURVES VERSUS OUTPUT CAPACITANCE (T_A = 25°C unless otherwise noted)

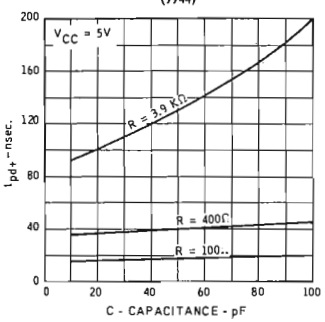
t_{pd} OF GATES VERSUS CAPACITANCE



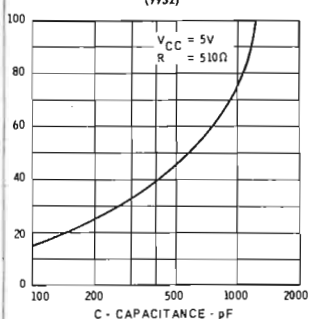
t_{pd-} VERSUS CAPACITANCE (9932 - 9944)



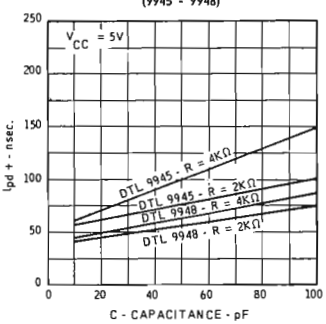
t_{pd+} VERSUS CAPACITANCE (9944)



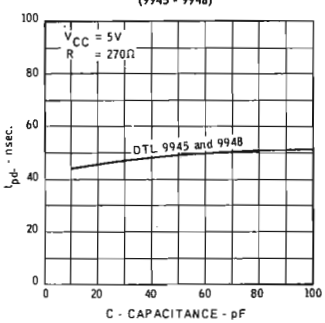
t_{pd+} VERSUS CAPACITANCE (9932)



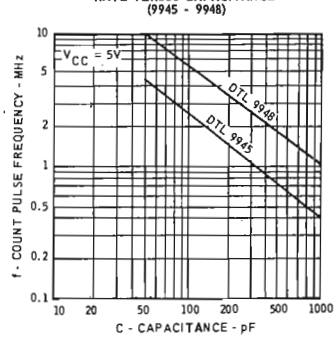
t_{pd+} VERSUS CAPACITANCE (9945 - 9948)



t_{pd-} VERSUS CAPACITANCE (9945 - 9948)

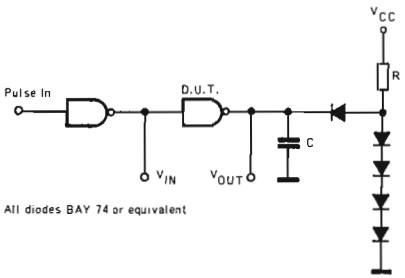


MAXIMUM BINARY COUNTING RATE VERSUS CAPACITANCE (9945 - 9948)



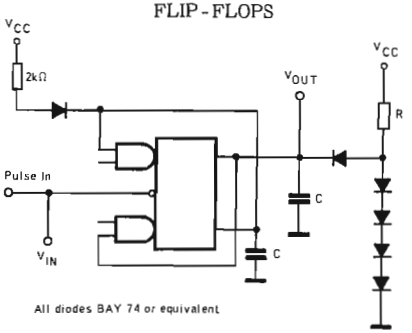
TEST CIRCUITS

GATES

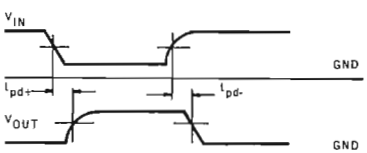


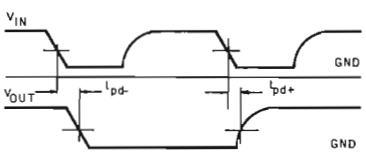
All diodes BAY 74 or equivalent

FLIP-FLOPS



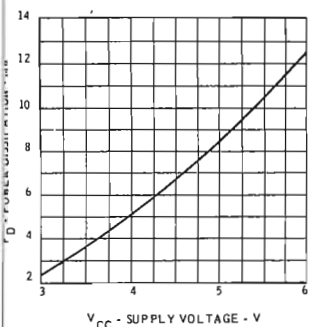
All diodes BAY 74 or equivalent



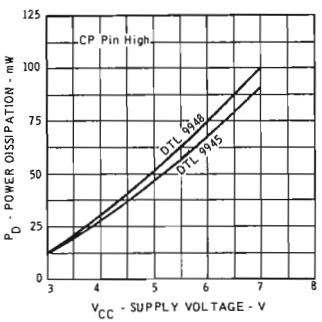


POWER DISSIPATION CURVES (T_A = 25°C unless otherwise noted)

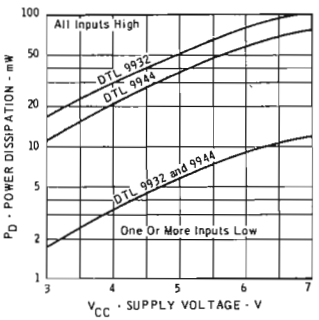
POWER DISSIPATION VS SUPPLY VOLTAGE, EACH GATE (9930, 9936, 9946, 9962)



POWER DISSIPATION VS. SUPPLY VOLTAGE (9945 - 9948)

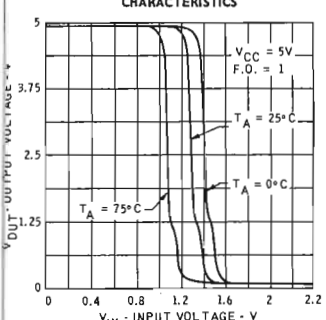


POWER DISSIPATION PER SIDE VS. SUPPLY VOLTAGE (OUTPUT NOT LOADED) (9932 - 9944)

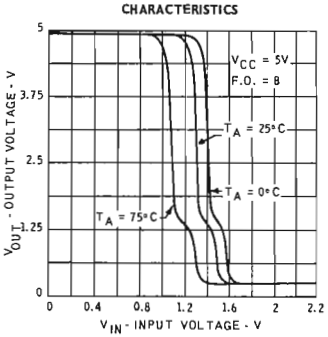


TRANSFER CHARACTERISTICS

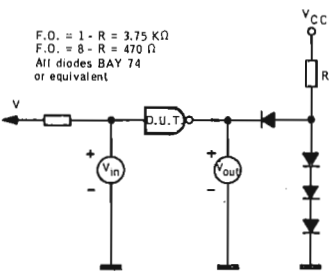
V_{OUT} - V_{IN} TRANSFER CHARACTERISTICS



V_{OUT} - V_{IN} TRANSFER CHARACTERISTICS



TEST CIRCUIT



NOISE IMMUNITY

V_{NS} is the maximum voltage which may be applied in the signal line without affecting the driven gate.
V_{NG} is the maximum voltage which may be applied in the ground connection without affecting the driven gate.
The variation of these two noise voltages with temperature and V_{CC} is shown in figures 1 through 5.
The guaranteed worst case noise curve shown on figure 5 is obtained by:

$$V_N = |V_{IL} - V_{OL}| \quad \text{or} \quad |V_{OH} - V_{IH}| \quad \text{whichever is smaller.}$$

where: V_{IL} = Maximum Low Input Voltage that guarantees V_{OH}

V_{OL} = Maximum Low Output Voltage

V_{IH} = Minimum High Input Voltage that guarantees V_{OL}

V_{OH} = Minimum High Output Voltage

(See the table of forcing functions and test limits for the values of these parameters).

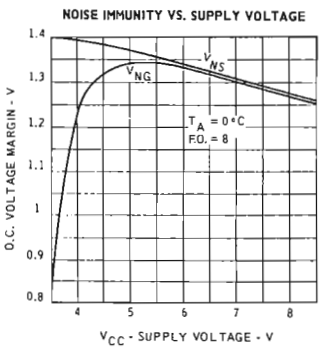


FIG. 1

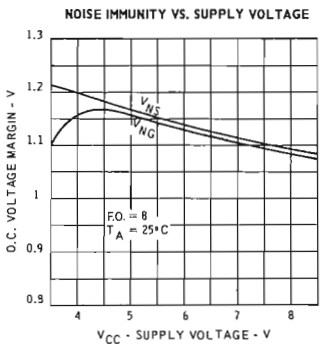


FIG. 2

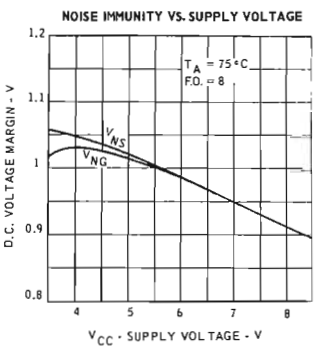


FIG. 3

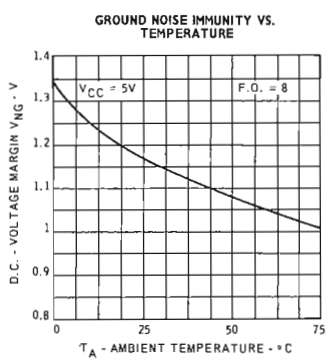


FIG. 4

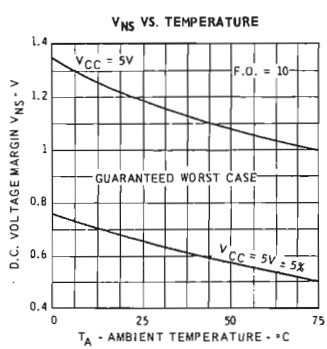
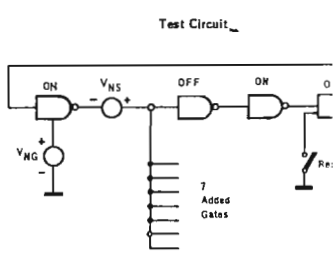
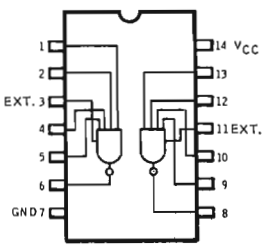


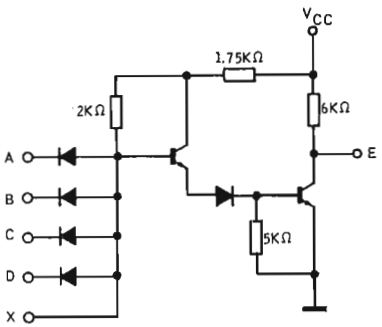
FIG. 5



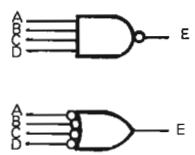
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



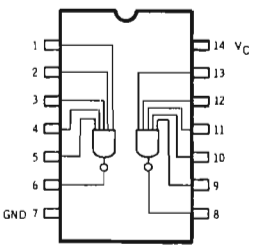
POSITIVE (NAND) LOGIC $E = \overline{A \cdot B \cdot C \cdot D}$

NEGATIVE (NOR) LOGIC $E = \overline{A + B + C + D}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

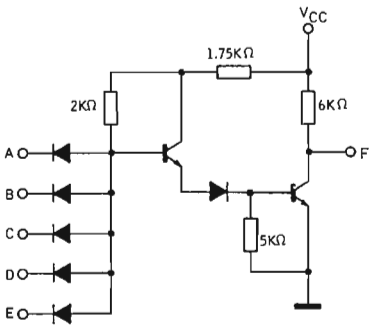
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)				3	4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	40			nsec	V_{CC} = 5 V see test circuit

CONNECTION DIAGRAM
(top view)

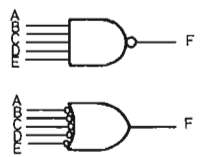


Plastic DIP only

SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



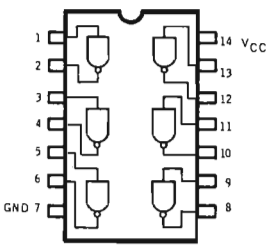
POSITIVE (NAND) LOGIC $F = \overline{A \cdot B \cdot C \cdot D \cdot E}$

NEGATIVE (NOR) LOGIC $F = \overline{A+B+C+D+E}$

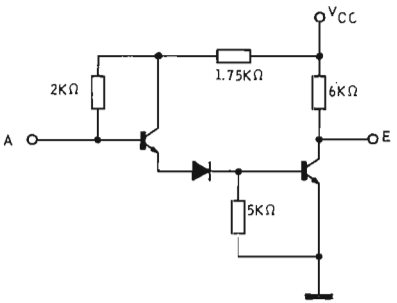
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)				3	4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	40			nsec	V_{CC} = 5 V see test circuit

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION

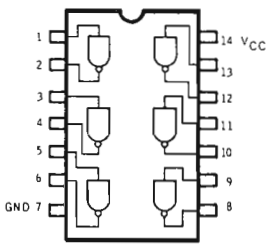
$A = \overline{E}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

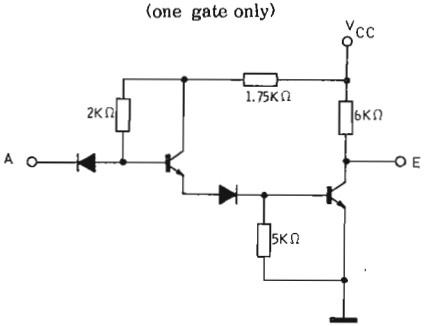
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75 V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25 V, I_{OL} = 15.2 mA all inputa at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52			-1.52		-1.52	mA	V_{CC} = 5.25V, V_F = 0.45V on other inputs V_R = 4V
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)					4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5V see test circuit
$t_{pd}-$	Turn-On Delay			10	30	40			nsec	V_{CC} = 5V see test circuit

NOTE : BAY-74 diode must be connected to each gate when testing this element.

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



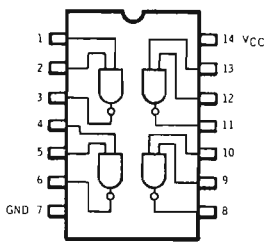
LOGIC FUNCTION

$A = \overline{E}$

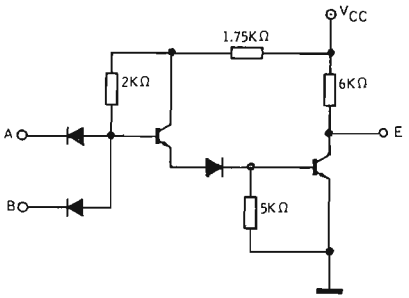
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)				3	4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	40			nsec	V_{CC} = 5 V see test circuit

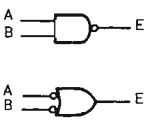
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



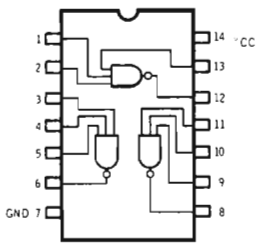
POSITIVE (NAND) LOGIC $E = \overline{A \cdot B}$

NEGATIVE (NOR) LOGIC $E = \overline{A + B}$

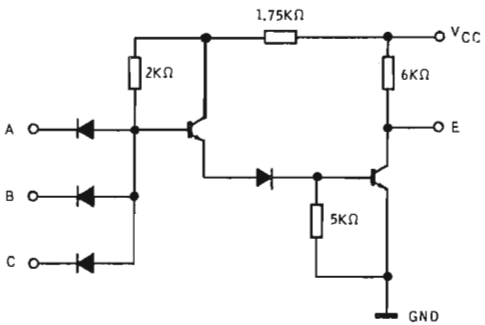
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	40			nsec	V_{CC} = 5 V see test circuit

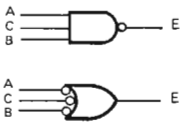
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



POSITIVE (NAND) LOGIC $E = \overline{A \cdot B \cdot C}$

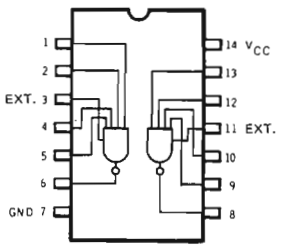
NEGATIVE (NOR) LOGIC $E = \overline{A + B + C}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

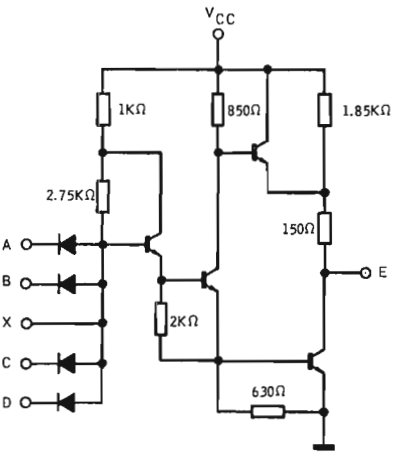
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)					4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	40			nsec	V_{CC} = 5 V see test circuit

STANDARD TEMPERATURE RANGE

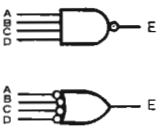
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



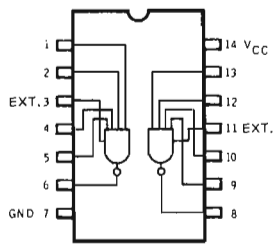
POSITIVE (NAND) LOGIC $E = \overline{A \cdot B \cdot C \cdot D}$

NEGATIVE (NOR) LOGIC $E = \overline{A+B+C+D}$

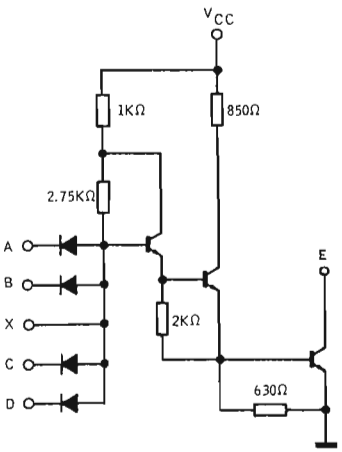
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	2.8		2.5		V	V_{CC} = 4.75V, I_{OH} = -2 mA @ 0°C one input = -2.5mA @ 25°C at V_{IL} = -3 mA @ 75°C (see below)
V_{OL}	Output Low Voltage		0.45			0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 33.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 38 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	15		16			14		mA	V_{CC} = 5V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)					15			mA	V_{CC} = 5 V inputs open
t_{pd+}	Turn-Off Delay			25	50	100			nsec	V_{CC} = 5 V see test circuit
t_{pd-}	Turn-On Delay			15	25	50			nsec	V_{CC} = 5 V see test circuit

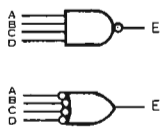
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



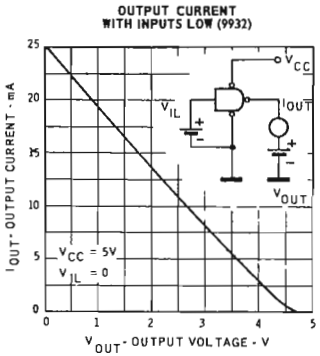
POSITIVE (NAND) LOGIC $E = \overline{A \cdot B \cdot C \cdot D}$

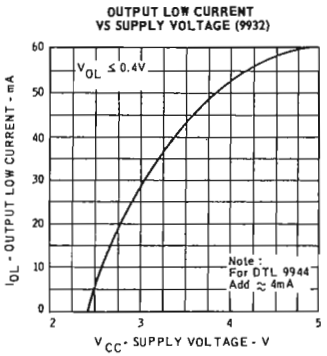
NEGATIVE (NOR) LOGIC $E = \overline{A+B+C+D}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OL}	Output Low Voltage		0.45		0.27	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 34 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 41 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25V, V_F = 0.45V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on other inputs
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CC} = 4.5V one input grounded, output at V_{CC}
I_{PD}	Power Dissipation Current (each gate)					10			mA	V_{CC} = 5 V inputs open
$t_{pd}+$	Turn-Off Delay			15	35	70			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	45			nsec	V_{CC} = 5 V see test circuit

OUTPUT CHARACTERISTICS (T_A = 25° C unless otherwise noted)

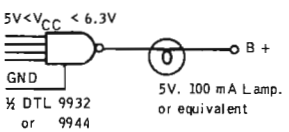




MISCELLANEOUS APPLICATIONS

Lamp Driving

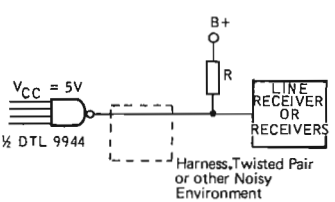
SUGGESTED RATINGS	DIP	FLAT	DIP pl.
Power Dissipation	400 mW	240 mW	300 mW
Max Hot Lamp Current one side only ON	120 mA	100 mA	110 mA
Max Hot Lamp Current both sides ON	90 mA	75 mA	80 mA



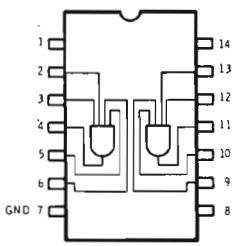
"Cold" lamp current is limited by saturation resistance, emitter resistance, and base current to about 200 to 250 mA. Thermal time constant is measured by forward diode drop in one gate with power pulsed into opposite gate.

Interfacing

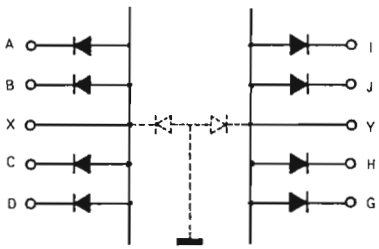
B + up to 12 volts. Line Receiver may have nominal low level of 1 volt; nominal threshold ≈ 4 V and nominal high level 8 V, for example. Resistor selected should be as low as possible consistent with required low input level of receiver, number of receivers, and power dissipation of system. For guaranteed operation in both applications the use of selected units is desirable. Operation as a lamp driver requires high gain units, and for interfacing high voltage units may be required.



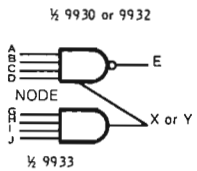
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



LOGIC FUNCTION



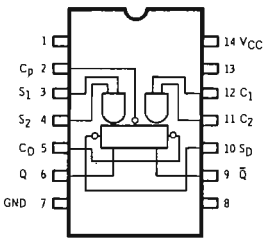
POS.LOGIC $E = \overline{A \cdot B \cdot C \cdot D \cdot G \cdot H \cdot I \cdot J}$

NEG.LOGIC $E = \overline{A+B+C+D+G+H+I+J}$

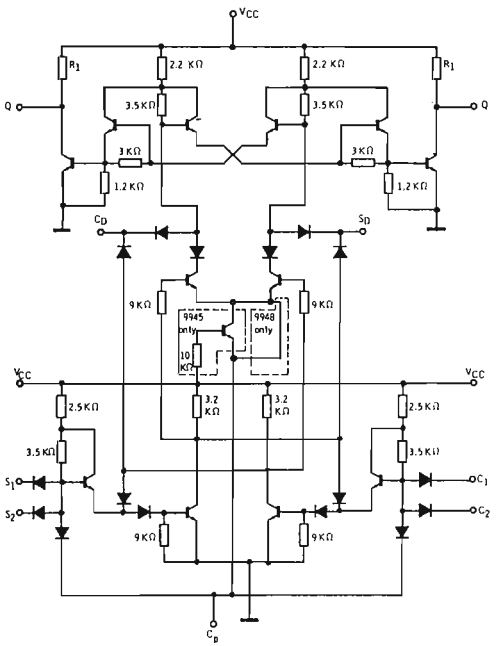
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{FD}	Forward Drop Voltage	0.70	0.90	0.66	0.84	0.56	0.76	V	I_{FD} = 2 mA applied to output, input grounded
I_R	Reverse Current		5		5		10	μA	V_R = 4 V, ground on other inputs
I_R	Output Reverse Current		25		25		50	μA	V_R = 4 V on output

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



NOTE: The DTL 9945 incorporates the standard 6KΩ output pull-up resistor, while the DTL 9948 features a 2KΩ output pull-up resistor for improved switching times, thus reducing however the drive capability.

Note:
DTL 9945 - R_1 = 6kΩ
DTL 9948 - R_1 = 2kΩ

LOGIC FUNCTION

Synchronous Entry Inputs				Output	Asynchronous Entry Inputs		Outputs		J - K Mode Truth Table Inputs		Outputs	
t_n				$t_n + 1$					t_n		$t_n + 1$	
S_1	S_2	C_2	C_1	Q	C_D	S_D	Q	$\overline{Q}$	S_1	C_1	Q	$\overline{Q}$
L	X	L	X	NC	H	H	NC	NC	L	H	L	H
L	X	X	L	NC	H	L	H	L	H	L	H	L
X	L	L	X	NC	L	H	L	H	H	H	$\overline{Q}_n$	Q_n
X	L	X	L	NC	L	L	H	H	L	L	Q_n	$\overline{Q}_n$
L	X	H	H	L								
X	L	H	H	L								
H	H	L	X	H								
H	H	X	L	H								
H	H	H	H	Undetermined								

For J - K Mode Operation:
Connected 4 to 9 and 11 to 6.

NOTES:

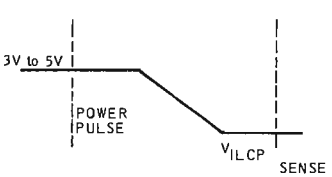
1) Abbreviation used in the body of tables:
L = low, the more negative voltage level.
H = high, the more positive voltage level (in all cases, unused pins have the same effect as high).
X = immaterial, either H or L has equal effect.
NC = no change, the clock pulse has no effect on outputs.
Q_n = outputs state at time t_n

2) The L symbol in the S and C input column is defined as meaning that the input does not go high at any time while the clock is high. The H symbol in the S and C input column is defined as meaning that the input is high at the same time as the clock is high.

9945 ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min. Max.		
V_{OH}	Output High Voltage	2.5		2.6	3.3		2.5	V	V_{CC} = 4.75V, I_{OH} = −0.18 mA V_{IL} (see below) on proper asynchronous input
V_{OL}	Output Low Voltage		0.45		0.25	0.45	0.45	V	V_{CC} = 4.75V, I_{OL} = 16 mA V_{CC} = 5.25V, I_{OL} = 16 mA V_{IH} (see below) on proper asynchronous input
V_{IH}	Input High Voltage	2		1.9			1.8	V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1	0.95	V	Guaranteed input low threshold for all inputs
I_F	S & C Inputs Load Current		-1			-1	-0.95	mA	V_{CC} = 5.25V, V_F = 0.45V V_R = 4 V on other inputs
I_{FS}	S_D, C_D Inputs Load Current		-2.96			-2.96	-2.85	mA	V_{CC} = 5.25V, V_F = 0.45V V_R = 4 V on other inputs
I_{FCP}	Clock Input Load Current		-2.96			-2.96	-2.85	mA	V_{CC} = 5.25V, V_F = 0.45V V_{IL} on S_D
I_R	S, C, S_D, C_D Inputs Leakage Current		5			5	10	μA	V_{CC} = 5.25V, V_R = 4 V ground on other inputs
I_{RCP}	Clock Input Leakage Current		20			20	30	, A	V_{CC} = 4 V, V_R = 4 V S and C_D inputs grounded
I_{PD}	Power Dissipation Current					15		mA	V_{CC} = 5 V
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56 -1.33	mA	V_{CC} = 5.25V high output grounded
$t_{pd}+$	Turn-Off Delay				30	90		nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay				30	90		nsec	V_{CC} = 5 V see test circuit

CLOCK PULSE DESCRIPTION



V_{ILCP} = 1V @ 25° C

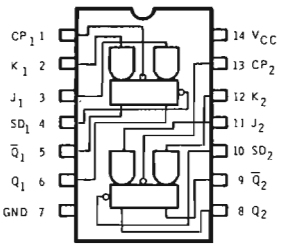
9948 ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.5		2.6	3.3		2.5		V	V_{CC} = 4.75V, I_{OH} = −0.54 mA V_{IL} (see below) on proper asynchronous input
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 14.6 mA V_{CC} = 5.25V, I_{OL} = 14.6 mA V_{IH} (see below) on proper asynchronous input
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	S & C Inputs Load Current		-1			-1		-0.95	mA	V_{CC} = 5.25V, V_F = 0.45V on other inputs V_R = 4 V
I_{FS}	C_D, S_D Inputs Load Current		-2.96			-2.96		-2.85	mA	V_{CC} = 5.25V, V_F = 0.45V
I_{FCP}	Clock Input Load Current		-2.38			-2.38		-2.26	mA	V_{CC} = 5.25V, V_F = 0.45V V_{IL} on S_D
I_R	S, C, S_D, C_D Inputs Leakage Current		5			5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on other inputs
I_{RCP}	Clock Input Leakage Current		20			20		30	μA	V_{CC} = 4 V, V_R = 4 V S and C_D inputs grounded
I_{PD}	Power Dissipation Current					17.5			mA	V_{CC} = 5 V
I_{SC}	Output Short Circuit Current	-1.86	-4.41	-1.86		-4.41	-1.68	-4.20	mA	V_{CC} = 5.25V high output grounded
t_{pd+}	Turn-Off Delay			30		80			nsec	V_{CC} = 5 V see test circuit
t_{pd-}	Turn-On Delay			30		80			nsec	V_{CC} = 5 V see test circuit

CLOCK PULSE DESCRIPTION : SEE 9945

NOTE: The DTL 9093 and 9094 are respectively dual DTL 9945 and 9948 flip-flops.

CONNECTION DIAGRAM
(top view)



LOGIC FUNCTION

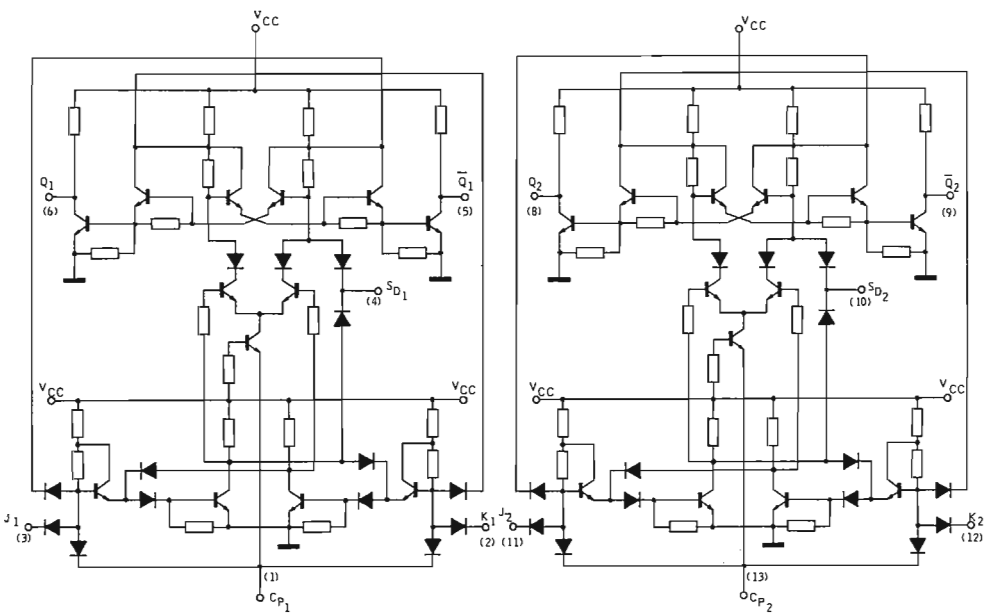
Asynchronous Entry			J-K Mode Truth Table			
Input	Outputs		Inputs		Outputs	
			t_n		$t_n + 1$	
4 (10)	6 (8)	5 (9)	3 (11)	2 (12)	6 (8)	5 (9)
H	NC	NC	L	H	L	H
L	H	L	H	L	H	L
			H	H	$\bar{Q}_n$	Q_n
			L	L	Q_n	$\bar{Q}_n$

NOTES:

1) Abbreviations used in the body of tables:
   L = low, the more negative voltage level
   H = high, the more positive voltage level
   (in all cases, unused pins have the same effect as high).
   NC = no change, the clock pulse has no effect on outputs.
   Q_n = outputs state at time tn

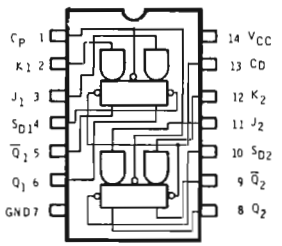
2) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is high.
   The H symbol in the J and K input column is defined as meaning that the input is high at the same time as the clock is high.

SCHEMATIC DIAGRAM 9093/9094 (9093 SHOWN)



NOTE: The DTL 9097 and 9099 are respectively dual DTL 9948 and 9945 flip-flops.

CONNECTION DIAGRAM
(top view)



LOGIC FUNCTION

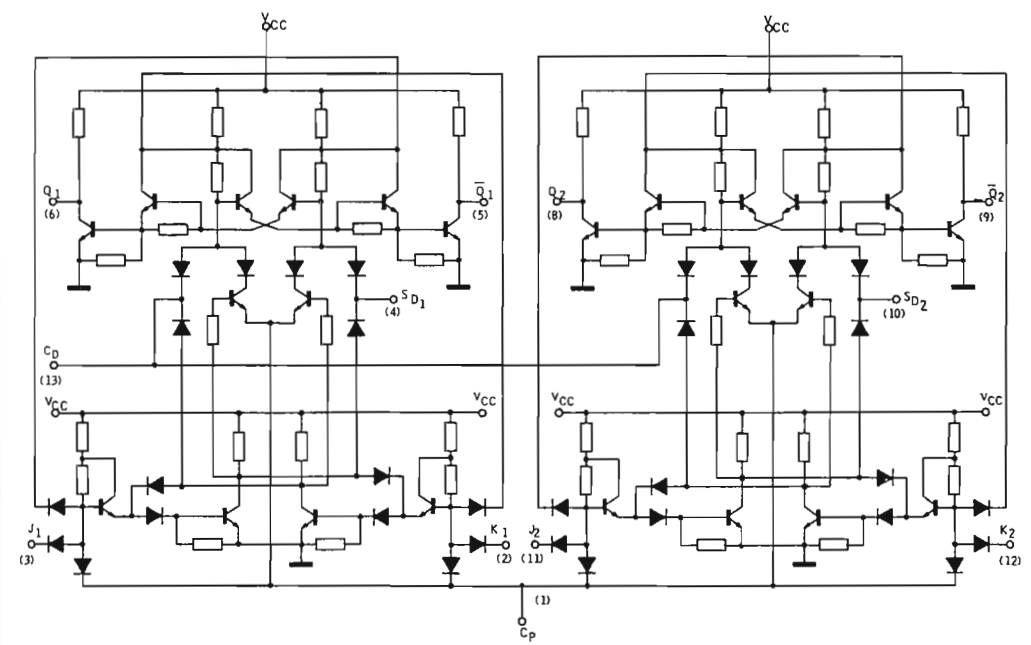
Asynchronous Entry				J-K Mode Truth Table			
Inputs		Outputs		Inputs		Outputs	
				t_n		$t_n + 1$	
13	4 (10)	6 (8)	5 (9)	3 (11)	2 (12)	6 (8)	5 (9)
H	H	NC	NC	L	H	L	H
H	L	H	L	H	L	H	L
L	H	L	H	H	H	$\overline{Q}_n$	Q_n
L	L	H	H	L	L	Q_n	$\overline{Q}_n$

NOTES:

1) Abbreviations used in the body of tables:
   L = low, the more negative voltage level
   H = high, the more positive voltage level
   (in all cases, unused pins have the same effect as high).
   NC = no change, the clock pulse has no effect on outputs.
   Q_n = outputs state at time t_n.

2) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is high.
   The H symbol in the J and K input column is defined as meaning that the input is high at the same time as the clock is high.

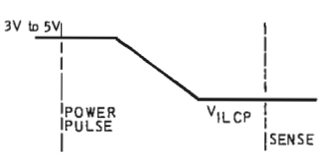
SCHEMATIC DIAGRAM 9097/9099 (9097 SHOWN)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA V_{IL} (see below) and V_R = 4 V on asynchronous inputs
V_{OL}	Output Low Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 16 mA V_{CC} = 5.25V, I_{OL} = 16 mA ground and V_R = 4 V on asynchronous inputs
V_{IL}	Input Low Voltage		1.2		1.1		0.95	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.9		1.8		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current J and K Inputs		-1		-I		-0.95	mA	V_{CC} = 5.25V, V_F = 0.45V
I_{FCP}	Clock Input Load Current 9093 9099		-2.98 -5.96		-2.98 -5.96		-2.86 -5.72	mA	V_{CC} = 5.25V, V_F = 0.45V V_{IL} (see above) on asynchronous input
I_{FS}	Set Input Load Current		-2.23		-2.23		-2.15	mA	V_{CC} = 5.25V, V_F = 0.45V ground on J inputs
I_{FC}	Clear Input Load Current		-4.40		-4.40		-4.28	mA	V_{CC} = 5.25V, V_{CC} = 0.45V ground on K inputs
I_R	Input Leakage Current J and K Inputs		5		5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on clock
I_{RS}	Set Input Leakage Current		5		5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on K inputs
I_{RC}	Clear Input Leakage Current		10		10		20	μA	V_{CC} = 5.25V, V_R = 4 V ground on J inputs
I_{RCP}	Clock Input Leakage Current 9093 9099		20 40		20 40		30 60	μA	V_{CC} = 4 V, V_R = 4 V ground on J inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65	-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V high output grounded
I_{PD}	Power Dissipation Current 9093 9099				30 28			mA	V_{CC} = 5 V
t_{pd+}	Turn-Off Delay			30	90			nsec	V_{CC} = 5 V see test circuit
t_{pd-}	Turn-On Delay			30	90			nsec	V_{CC} = 5 V see test circuit

CLOCK PULSE DESCRIPTION:



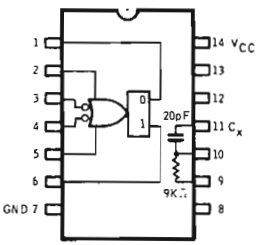
V_{ILCP} = 1V @ 25° C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

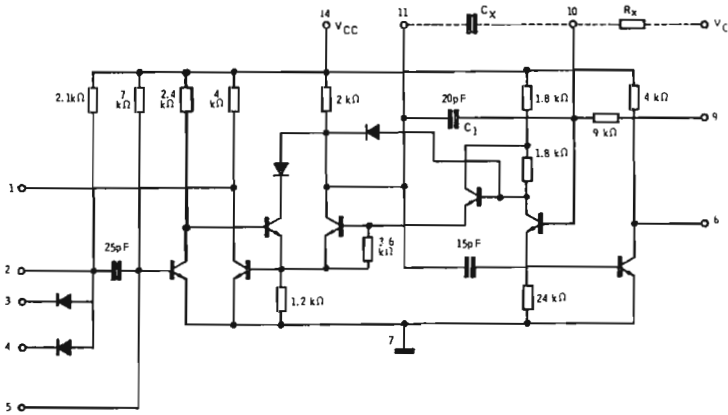
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	V_{CC} = 4.75V, I_{OH} = 0.54 mA V_{IL} (see below) and V_R = 4 V on asynchronous inputs
V_{OL}	Output Low Voltage		0.45		0.45		0.45	V	V_{CC} = 5.25V, I_{OL} = 14.6 mA V_{CC} = 4.75V, I_{OL} = 14.6 mA ground and V_R = 4 V on asynchronous inputs
V_{IH}	Input High Voltage	2		1.9		1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2		1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current J and K Inputs		-1		-1		-0.95	mA	V_{CC} = 5.25V, V_F = 0.45V
I_{FCP}	Clock Input Load Current 9094 9097		 -2.38 -4.76		 -2.38 -4.76		 -2.20 -4.76	mA	V_{CC} = 5.25V, V_F = 0.45V V_{IL} (see above) on asynchronous input
I_{FS}	Set Input Load Current		-2.23		-2.23		-2.15	mA	V_{CC} = 5.25V, V_F = 0.45V ground on J inputs
I_{FC}	Clear Input Load Current		-4.40		-4.40		-4.28	mA	V_{CC} = 5.25V, V_F = 0.45V ground on K inputs
I_R	Input Leakage Current J and K inputs		5		5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on clock
I_{RCP}	Clock Input Leakage Current 9094 9097		 20 40		 20 40		 30 60	μA	V_{CC} = 4 V, V_R = 4 V ground on J inputs
I_{RS}	Set Input Leakage Current		5		5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on K inputs
I_{RC}	Clear Input Leakage Current		10		10		20	μA	V_{CC} = 5.25V, V_R = 4 V ground on J inputs
I_{SC}	Output Short Circuit Current	-1.86	-4.41	-1.86	-4.41	-1.68	-4.20	mA	V_{CC} = 5.25V high output grounded
I_{PD}	Power Dissipation Current 9094 9097				 35 32.4			mA	V_{CC} = 5 V
$t_{pd}+$	Turn-Off Delay			30	80			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			30	80			nsec	V_{CC} = 5 V see test circuit

CLOCK PULSE DESCRIPTION : SEE 9093 - 9099

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V)

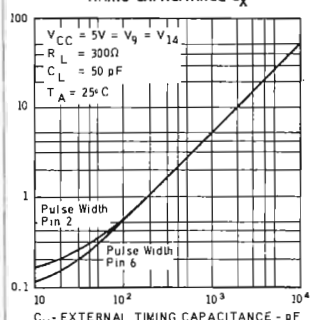
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	3.2		3.2		3.2		V	V_{CC} = 5V, I_{OH} = 0.15 mA Pin 2 grounded, Pin 9 at V_{CC}
V_{OL}	Output Low Voltage		0.45		0.45		0.5	V	V_{CC} = 5V, I_{OL}=14.8 mA @ 0°C and 25°C I_{OL}=14 mA @ 75°C when testing Pin 1, ground Pin 10 when testing Pin 6, V_{CC} on Pin 9
I_F	Input Load Current	-2.8		-2.8		-2.66		mA	V_{CC} = 5V, V_F = V_{OL} V_R = 4 V (see above)
I_R	Input Leakage Current	5		5		10		μA	V_{CC} = 5V, V_R = 4 V ground on Pin 2
I_{PD}	Power Dissipation Current			10.8				mA	V_{CC} = 5 V inputs grounded, V_{CC} on Pin 9
$t_{pd}+$	Turn-Off Delay (Pin 6)			40				nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay (Pin 1)			40				nsec	V_{CC} = 5 V see test circuit
P_W	Pulse Width (Pin 1)			90	330			nsec	V_{CC} = 5 V see test circuit
P_W	Pulse Width (Pin 6)			70	270			nsec	V_{CC} = 5 V see test circuit

RULES FOR USE OF DTL 9951

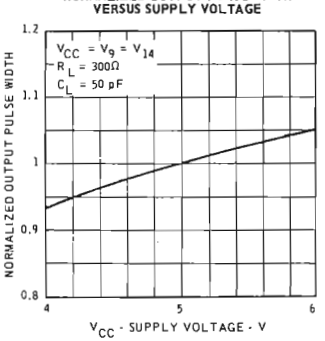
1) With Pin 9 connected to V_{CC} and no external capacitor (C_x), the output pulse width is approximately 100 nsec.
2) With Pin 9 connected to V_{CC} and an external capacitor (C_x) connected between Pins 10 and 11, the output pulse width (T) is: $T \sim 6.4\ (C_x + 20)$ with C_x in pF and T in nsec.
3) For improved pulse width control, Pin 9 is left open and a stable external resistor (R_x) of 9 kΩ minimum to 15 kΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \sim 0.64\ R_x\ (C_x + 20)$ with R_x in kΩ, C_x in pF and T in nsec.
4) The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2kΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5) The maximum input fall time to trigger: 15 nsec for a 1 V swing; 40 nsec for a 2 V swing; 80 nsec for a 4 V swing.
6) The AC sensitivity of the inputs may be decreased by connecting a capacitor between Pin 5 and ground.
7) The minimum pulse width at output Pin 1 is approximately 100 nsec. This pulse width may be decreased to 50 nsec by connecting a 10 kΩ resistor between Pin 5 and V_{CC}.

TIMING CHARACTERISTICS

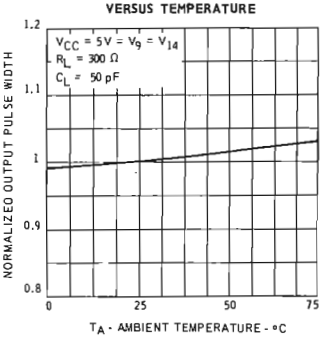
OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X



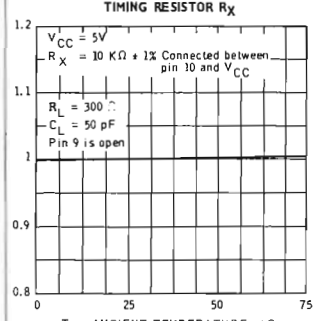
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



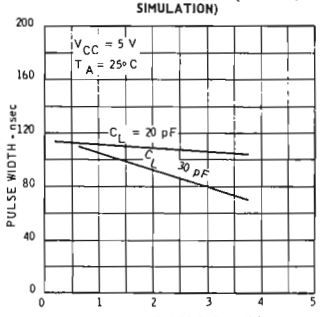
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE



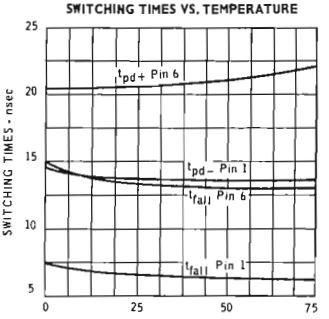
NORMALIZED OUTPUT PULSE WIDTH VS. TEMPERATURE USING EXTERNAL TIMING RESISTOR R_X



PIN 6 OUTPUT PULSE WIDTH VERSUS LOAD RESISTANCE (FAN-OUT SIMULATION)

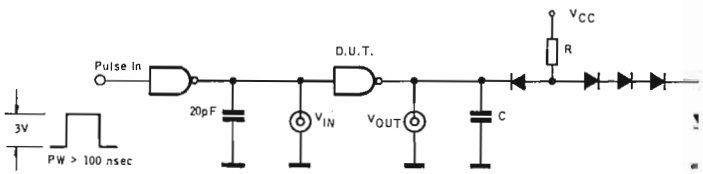


SWITCHING TIMES VS. TEMPERATURE



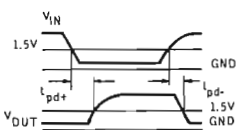
SWITCHING TIME TEST CIRCUITS

9930 - 9934 - 9936 - 9946 - 9962 GATES t_{pd} TEST CIRCUIT



Diodes are BAY 74

WAVEFORMS

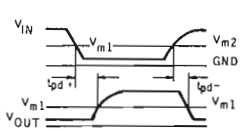


TEST CONDITIONS

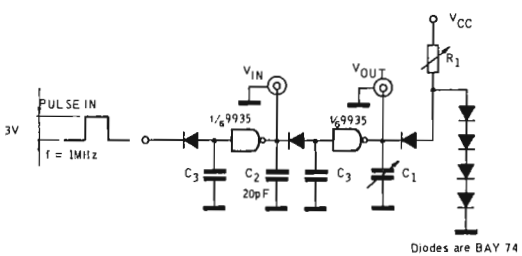
	R	C
t_{pd} +	3.9 kΩ	30 pF
t_{pd} -	400 Ω	50 pF

9935 GATE t_{pd} TEST CIRCUIT

WAVEFORMS



V_{m1}	V_{m2}
1.5V	1.3V



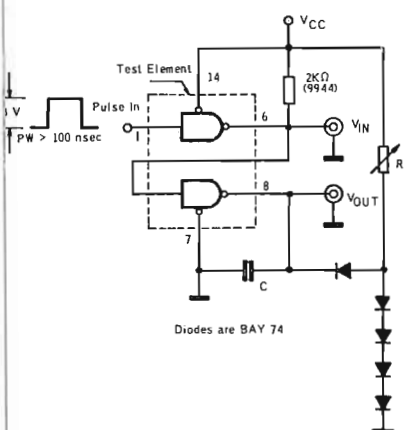
Diodes are BAY 74

TEST CONDITIONS

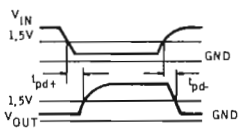
	R_1	C_1	C_2	C_3
t_{pd} +	3.9 kΩ	30 pF	20 pF	5 pF
t_{pd} -	400 Ω	50 pF	20 pF	5 pF

SWITCHING TIME TEST CIRCUITS

9932 - 9944 GATES t_{pd} TEST CIRCUIT



WAVEFORMS

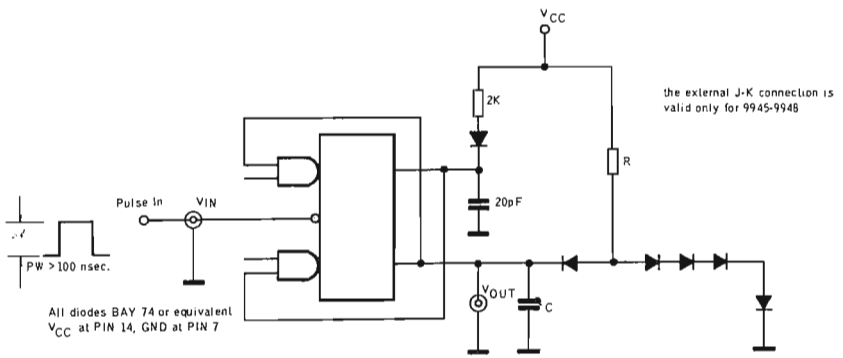


TEST CONDITIONS

	R	C
9944 t_{pd} +	510Ω	20 pF
9944 t_{pd} -	150Ω	100 pF
9932 t_{pd} +	510Ω	500 pF
9932 t_{pd} -	150Ω	500 pF

SWITCHING TIME TEST CIRCUITS

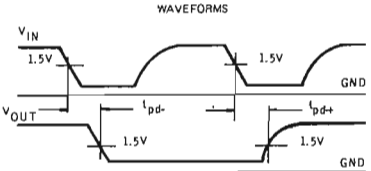
9945 - 9948 - 9093 - 9094 - 9097 - 9099 FLIP-FLOPS t_{pd} TEST CIRCUIT



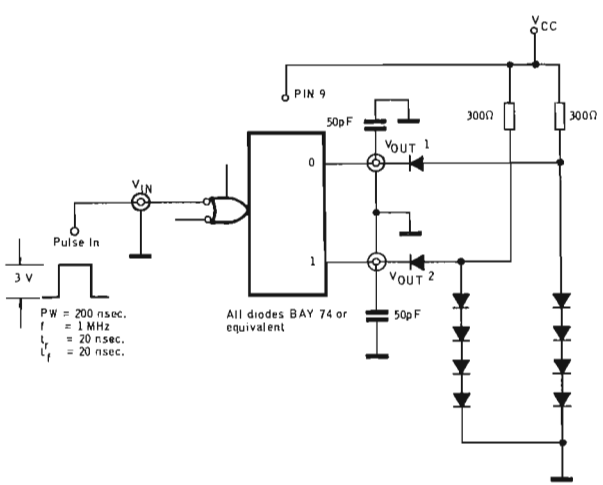
TEST CONDITIONS

	R	C
$t_{pd}+$	2KΩ	30 pF
$t_{pd}-$	330Ω	50 pF

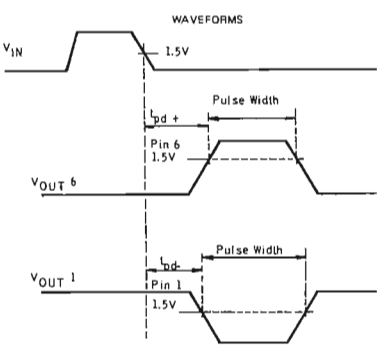
WAVEFORMS



9951 MONOSTABLE t_{pd} TEST CIRCUIT



WAVEFORMS



TTL INTEGRATED CIRCUITS

TTL INTEGRATED CIRCUITS

E. = Extended temperature range
S. = Standard temperature range

transistor-transistor logic family

EXTENDED TEMPERATURE RANGE - 55°C + 125°C

- Compatible with DTL and LPDTL products
- Input diode clamping
- Noise immunity 1V
- Worst case noise immunity 0.4V
- Output drive capability of 10
- Power dissipation 11 mW per gate
- Gate propagation delay of 6 nsec
- Output pull-up circuit
- Same pin configuration as the corresponding DTL and LPDTL products

The Transistor-Transistor logic integrated circuit family (TTL) combines a high fanout, high noise immunity, low power dissipation and good capacitive load driving capability with low propagation delay times. The circuits are fabricated within a silicon monolithic substrate using Planar Epitaxial processes.

TTL elements are available in two hermetically sealed ceramic packages: the Dual in Line Package (D), designed for low cost insertion, and the 14 lead flat package (F) for maximum component density.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

V_{CC} pin potential to Ground	- 0.5 V to 8 V
Input Voltage (see Note)	- 0.5 V to 5.5 V
Gate Output Voltage, Inputs Low	- 0.5 V to V_{CC}
Gate Current Into Output Terminal, Inputs High (except T109)	50 mA
Gate Current Into Output Terminal, Inputs High T109	100 mA
Flip-Flop Output Voltage when output is normally high	- 0.5 V to V_{CC}
Flip-Flop Current Into Output Terminal when output is normally low	50 mA
Storage Temperature Range	- 65°C to 150°C
Temperature (Ambient) Under Bias	- 55°C to 125°C

OPERATING CONDITIONS

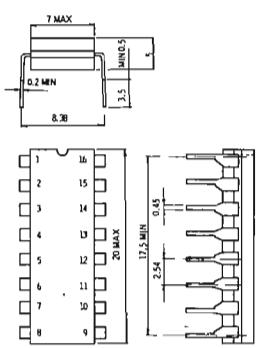
Temperature Range	- 55°C to 125°C
Supply Voltage (V_{CC})	5 V ± 10%

ORDERING NUMBER

T1XXD2 (for Dual in-Line Package)
T1XXF2 (for Flat Package)

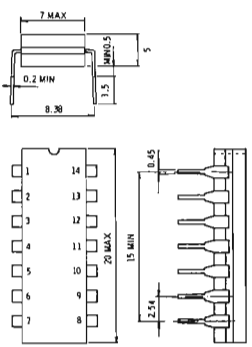
NOTE - Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than -0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

PHYSICAL DIMENSIONS
16-pin ceramic DIP



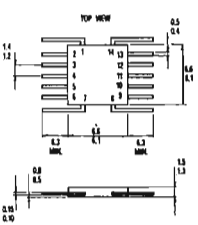
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
14-pin ceramic DIP



Note : all dimensions in mm.

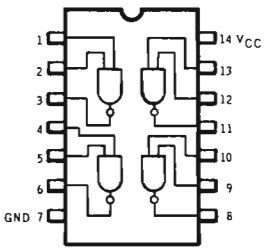
PHYSICAL DIMENSIONS
Flat ceramic package



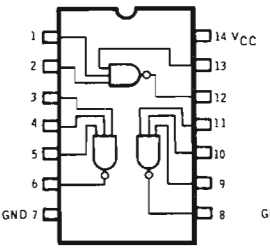
Note: All dimensions in mm.

EXTENDED TEMPERATURE RANGE

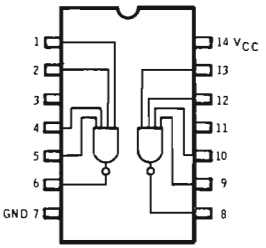
CONNECTION DIAGRAMS (top view)



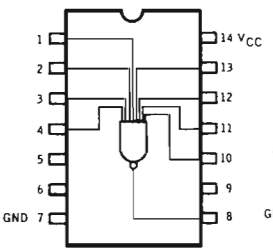
T 102



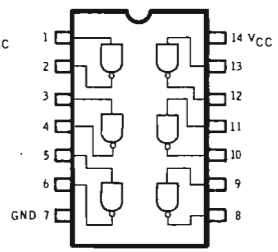
T 103



T 104

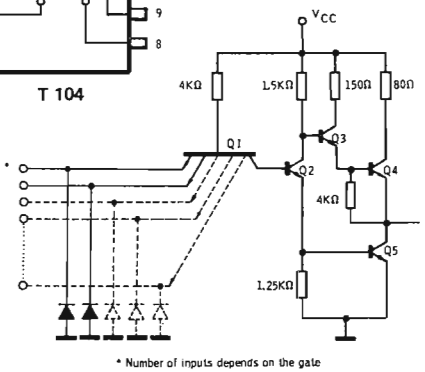


T 107



T 116

BASIC GATE CIRCUIT



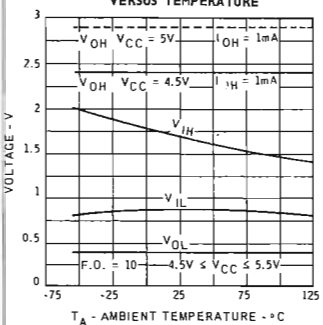
* Number of inputs depends on the gate

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

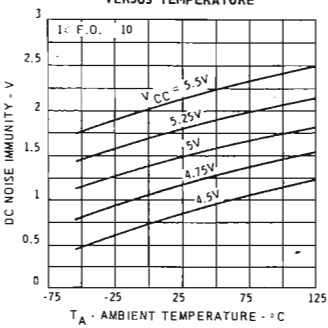
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		- 55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.5 V, I_{OH} = -1.32 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC} = 5.5 V, I_{OL} = 17.6 mA V_{CC} = 4.5 V, I_{OL} = 13.6 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		- 1.6		-1.1	-1.6		-1.6	mA	V_{CC} = 5.5 V, V_F = 0.4 V V_R = 5.5 V on other inputs
I_R	Input Leakage Current				10	60		60	µA	V_{CC} = 5.5 V, V_R = 4.5 V, Gnd on other inputs
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC} = 5.5 V Inputs and output grounded
I_{PD}	Power Dissipation Current (each gate)		5.5		3.5	5.5		5.5	mA	V_{CC} = 5 V inputs open
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			3 3		10 12			nsec nsec	V_{CC} = 5 V, C_L = 15 pF See test circuit

EXTENDED TEMPERATURE RANGE

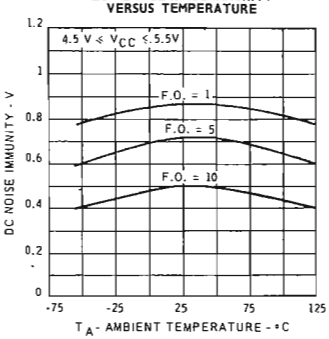
WORST CASE LOGIC LEVELS VERSUS TEMPERATURE



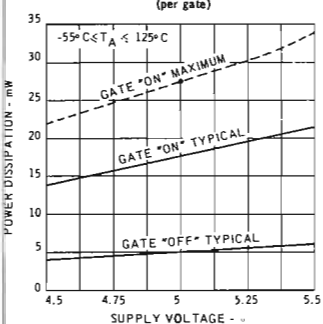
HIGH LEVEL NOISE IMMUNITY VERSUS TEMPERATURE



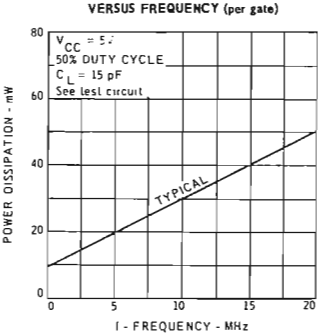
LOW LEVEL NOISE IMMUNITY VERSUS TEMPERATURE



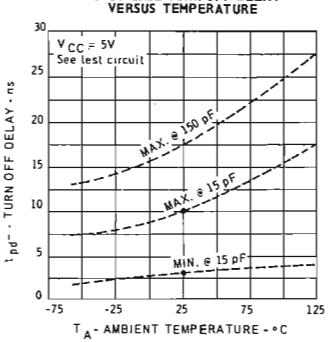
WORST CASE POWER DISSIPATION VERSUS SUPPLY VOLTAGE (per gate)



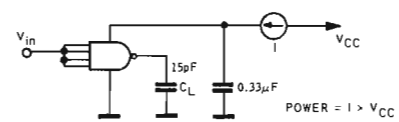
WORST CASE POWER DISSIPATION VERSUS FREQUENCY (per gate)



WORST CASE TURN OFF DELAY VERSUS TEMPERATURE

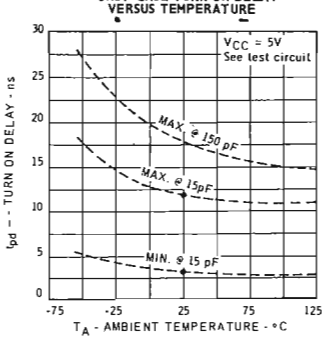


AC POWER TEST CIRCUIT

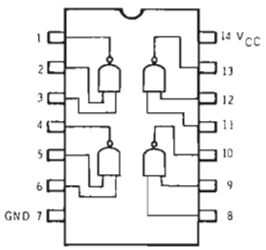


Note: Capacitance includes probe and jig capacity
All inputs to be tied together

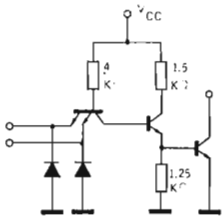
WORST CASE TURN ON DELAY VERSUS TEMPERATURE



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



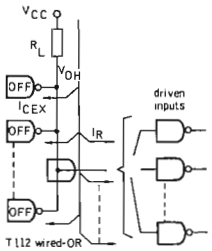
ELECTRICAL CHARACTERISTICS (T_A - 55°C to 125°C, V_{CC} = 5 V ± 10%)

SYMBOL AND CHARACTERISTICS		LIMITS						UNIT	CONDITIONS AND COMMENTS
		- 55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC} = 5.5V I_{OL} = 17.6 mA V_{IH} = value indicated below
V_{IH}	Input High Threshold	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Threshold		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.5 V V_F = 0.4V V_R = 5.5V on other input
I_R	Input Leakage Current				10	60		60	µA	V_{CC} = 5.5V V_R = 4.5V ground on other input
I_{CEX}	Output Leakage Current					150		150	µA	V_{CC} = 4.5V inputs grounded 4.5V applied to output
I_{PD}	Power Dissipation Current (each gate)		5.5		3.5	5.5		5.5	mA	V_{CC} = 5V inputs open
t_{pd+}	Turn-Off Delay					32			nsec	V_{CC} = 5V
t_{pd-}	Turn-On Delay					12				C_L = 15 pF see test circuit

WIRED-OR APPLICATIONS

The T102 allows wired-OR operation when a proper load resistor (R_L) is connected between V_{CC} and output pins. General rules to calculate the allowed number of wired-OR gates with a requested drive factor are explained here below.
For a given number (K) of wired-OR gates end a given number (n) of driven CCSL gates, two equations can be written in order to determine the value of the external resistor (R_L) that guarantees a correct operation with respect to the same Noise Immunity levels as the CCSL family.

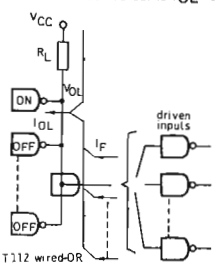
High Level : if all the wired-OR gates outputs are at the high level, a total current flows from supply through the external resistor R_L, that is the sum of the output leakage current I_{CEX} of the output wired-OR transistor and the input leakage current I_R of the driven gates. This current takes the output voltage to a value that should not be less than the V_{OH} voltage, that guarantees the high level Noise Immunity. Therefore, to limit this voltage drop, following R_L limitation should be respected :



$$R_{L\,max} = \frac{V_{CC} - V_{OH}}{K I_{CEX} + n I_R}$$

note that the resulting R_L value is a worst case as I_{CEX} given in present data sheet is measured at 4.5V instead of 2.4V. Besides even I_R is measured at 4.5 V.

Low level : when almost one of the wired-OR gates is at the low level (ON), a current flow from supply, through R_L, to the output of the ON transistor This current is the ratio of R_L and the allowed voltage drop, (the output leakage current of the OFF wired-OR gates is negligible). In addition, the output ON transistor sinks the output load current I_F of the driven inputs - The V_{OL} voltage guarantees the low level Noise Immunity, that is total sunk current should not overcome I_{OL} value; therefore, to limit the currant through R_L, following limitation should be respected :



$$R_{L\,min} = \frac{V_{CC} - V_{OL}}{I_{OL} - n I_F}$$

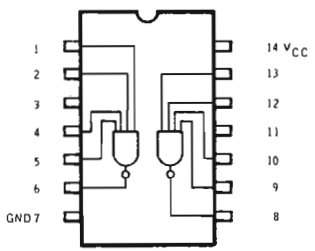
If more than one gate is ON, allowed R_L value is higher.
The two combined equations give maximum and minimum values among which should range R_L value :

$$\frac{V_{CC} - V_{OL}}{I_{OL} - n I_F} \leq R_L \leq \frac{V_{CC} - V_{OH}}{K I_{CEX} + n I_R}$$

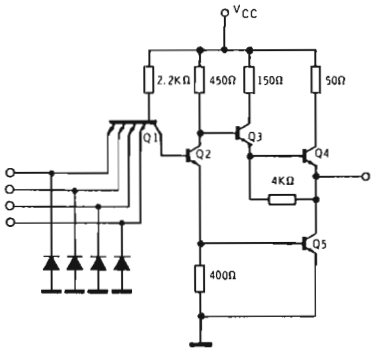
n = number of driven inputs

K = number of wired-OR T112 gates

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)

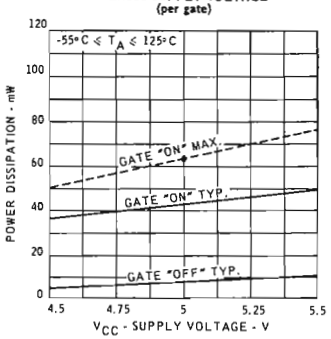


For noise immunity and operating level curves, refer to the gate section.

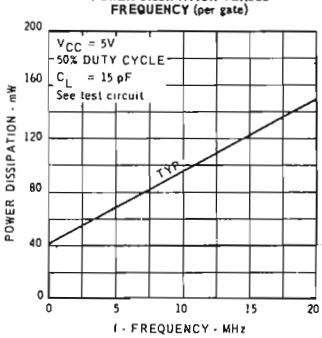
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		- 55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.5 V, I_{OH} = - 3.6 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC} = 5.5 V, I_{OL} = 48 mA V_{CC} = 4.5 V, I_{OL} = 40.8 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Gueranteed input low threshold for all inputs
I_F	Input Load Current		-3.2		-2.2	-3.2		-3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V, V_R = 5.5 V on other inputs
I_R	Input Leakage Current				20	120		120	µA	V_{CC} = 5.5 V, V_R = 4.5 V, Gnd on other inputs
I_{PD}	Power Dissipation Current (each gate)		12,9		8.6	12,9		12,9	mA	V_{CC} = 5 V inputs open
I_{SC}	Output Short Circuit Current	-40	-150	-40		-150	-40	-150	mA	V_{CC}= 5.5 V inputs and output grounded
t_{pd} + t_{pd} -	Turn Off Delay Turn On Delay			4 3		15 10			nsec nsec	V_{CC} = 5 V, C_L = 15 pF See test circuit

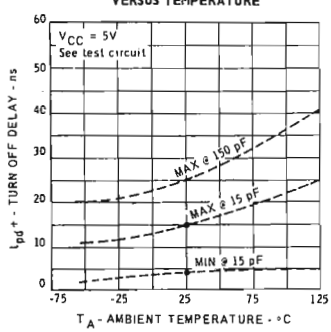
WORST CASE POWER DISSIPATION VERSUS SUPPLY VOLTAGE (per gate)



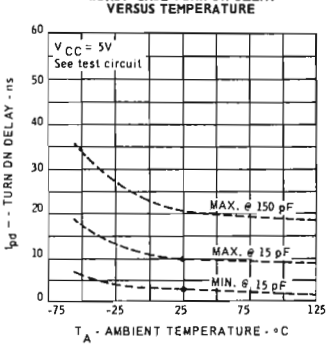
POWER DISSIPATION VERSUS FREQUENCY (per gate)



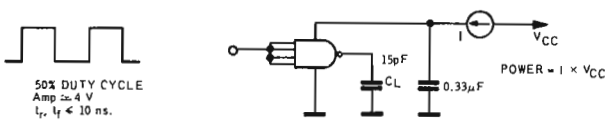
WORST CASE TURN OFF DELAY VERSUS TEMPERATURE



WORST CASE TURN ON DELAY VERSUS TEMPERATURE



AC POWER TEST CIRCUIT

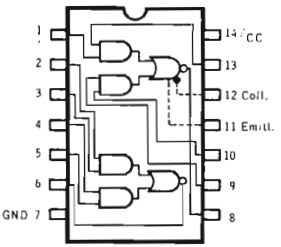


NOTE : Capacitance includes probe and jig capacity · All inputs are to be tied together

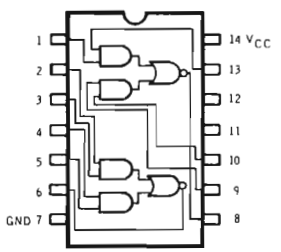
EXTENDED TEMPERATURE RANGE

The TTL T105 and T108 are AND – NOR gates which may be NOR expanded with the use of the T106 element.

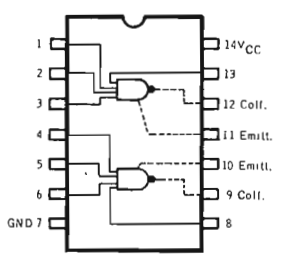
CONNECTION DIAGRAMS
(top view)



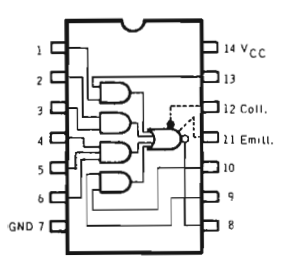
T 105



T 115

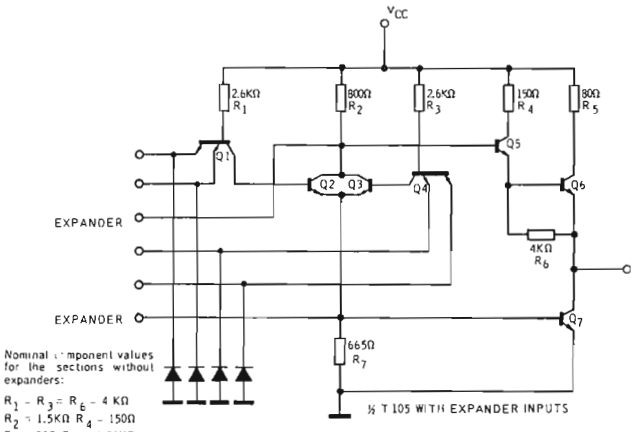


T 106

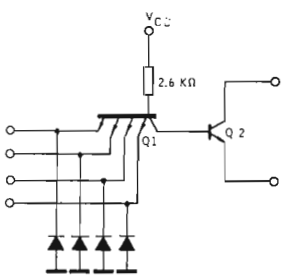


T 108

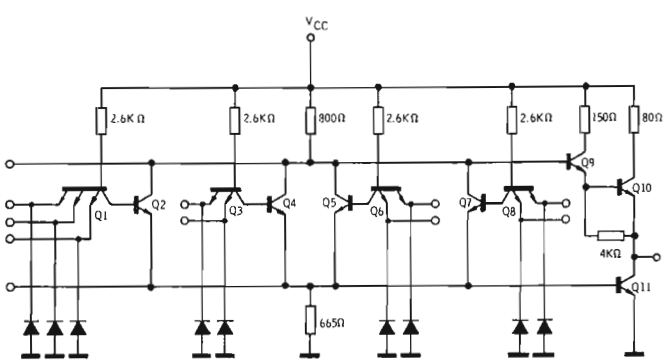
SCHEMATIC DIAGRAMS



T 105 - T 115



T 106 (one gate)



T 108

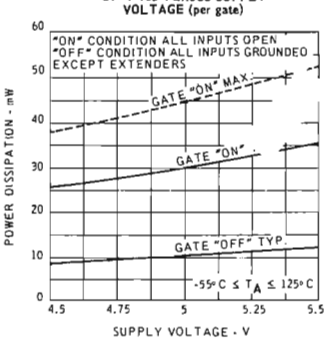
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		- 55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min. Max.		
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4	V	V_{CC} = 4.5 V I_{OH} = - 1.32 mA V_{IL} See below
V_{OL}	Output Low Voltage		0.4		0.2	0.4	0.4	V	V_{CC} = 5.5 V I_{OL} = 17.6 mA V_{IH} = 5.5 V V_{CC} = 4.5 V I_{OL} = 13.6 mA V_{IH} See below
V_{IH}	Input High Voltage	2		1.7			1.4	V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9	0.8	V	Guaranteed input low threshold for ell inputs
I_F	Input Load Current T105 (non exp. section)and T115 T105 (exp. section) T106 and T108		-1.6 -2.4		-1.1 -1.5	-1.6 -2.4	-1.6 -2.4	mA	V_{CC} = 5.5 V V_F = 0.4V 5.5 V on other inputs
I_R	Input Leakage Current T105 (non exp. section) and T115 T105 (exp. section) T106 and T108				5 7.5	60 90	60 90	µA	V_R = 4.5 V V_{CC} = 5.5 V Gnd on all other inputs
I_{PD}	Power Dissipation Current T105 T115 T108		17.8 13 12.5		12.1 9.5 9.3	17.8 13 12.5	17.8 13 12.5	mA	V_{CC} = 5 V All inputs open
ΔI_{PD}	Extra Current Drain when one T106 expander is attached to a T105 "ON"		1.61		1.08	1.61	1.61	mA	V_{CC} = 5V all inputs high
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30 -100	mA	V_{CC} = 5.5 V Inputs and output grounded
t_{pd+}	Turn off delay			4		12		nsec	T105 (non expandable section) and T115 V_{CC} = 5 V C_L = 15 pF See test circuit
t_{pd-}	Turn on delay			3		14		nsec	
t_{pd+}	Turn off delay			3		15		nsec	T105 (exp. section) and T108 V_{CC} = 5V C_L = 15 pF See test circuit
t_{pd-}	Turn on delay			3		12		nsec	
Δt_{pd+}	Turn off delay			-1		4		nsec	T106 only - the T106 is tested by measuring its t_{pd} through the T105 - see test circuit
Δt_{pd-}	Turn on delay			-1		4		nsec	

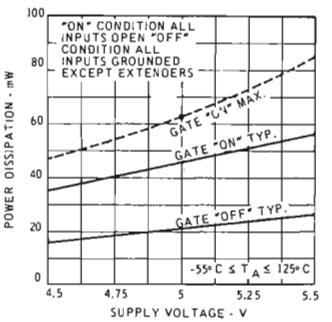
Note : 1) Output characteristics above apply to T105 - T115 and T108

2) Input characteristics above apply to T105, T115 and T108 using either the internal gates or an external T106 extender

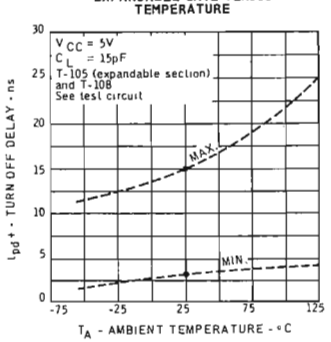
WORST CASE POWER DISSIPATION OF T 105 VERSUS SUPPLY VOLTAGE (per gate)



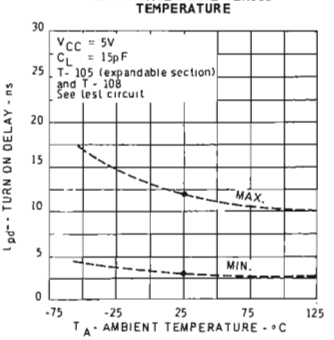
WORST CASE POWER DISSIPATION OF T 108 VERSUS SUPPLY VOLTAGE



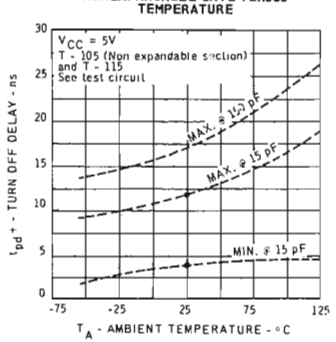
WORST CASE TURN OFF DELAY OF EXPANDABLE GATE VERSUS TEMPERATURE



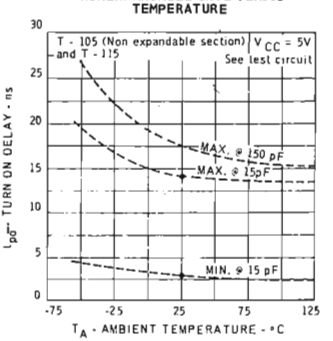
WORST CASE TURN ON DELAY OF EXPANDABLE GATE VERSUS TEMPERATURE



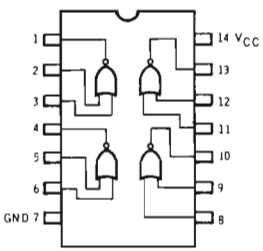
WORST CASE TURN OFF DELAY OF NONEXPANDABLE GATE VERSUS TEMPERATURE



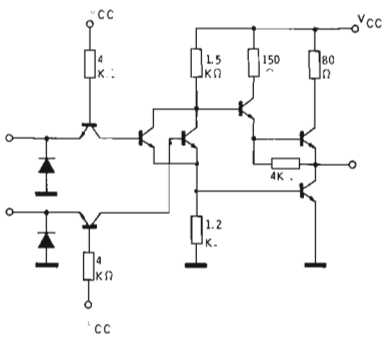
WORST CASE TURN ON DELAY OF NONEXPANDABLE GATE VERSUS TEMPERATURE



CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM
(one gate only)



ELECTRICAL CHARACTERISTICS (T_A = - 55°C to 125°C, V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		- 55°		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.5 V I_{OH} = - 1.32 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC} = 5.5 V I_{OL} = 17.6 mA V_{CC} = 4.5 V I_{OL} = 13.6 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6			-1.6		-1.6	mA	V_{CC} = 5.5 V V_F = 0.4 V 5.5 V on other input
I_R	Input Leakage Current				10	60		60	µA	V_{CC} = 5.5 V V_R = 4.5 V
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC} = 5.5 V inputs and output grounded
I_{PD}	Power Dissipation Current (each gate)		5.5		3.5	5.5		5.5	mA	V_{CC} = 5 V inputs open
t_{pd+}	Turn-Off Delay					10			nsec	V_{CC} = 5 V C_L = 15 pF see test circuit
t_{pd-}	Turn-On Delay					12				

GENERAL DESCRIPTION

The TTL family includes the T100 and T101 flip-flops to satisfy the storage element needs of a logic system. Each is a master-slave JK flip-flop with the same multi-emitter inputs and low impedance active pull-up outputs common to the gate elements.

The internal JK connections assure the user of non-ambiguous operation for all input states. The master-slave design with buffered clock input offers high noise immunity, low clock loading and eliminates the need for careful control of clock pulse rise or fall times. Data is accepted by the master when the clock is in the low logic state. Transfer from master to slave occurs when the clock goes from the low to the high logic level. When the clock is in the high logic level both J and K inputs are inhibited. For this reason it is desirable to maintain the clock pulse in the high level most of the duty cycle. Direct set and reset inputs provide true asynchronous control of both master and slave flip-flops independent of logic and clock input levels.

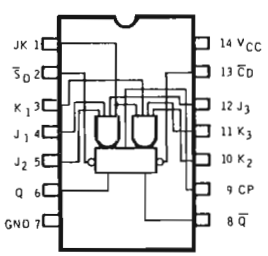
A common J-K input is provided which is useful in the physical layout of most logic configurations.

The two circuits are almost identical. The T100 has capacitors at the outputs of the J and Kdata input gates in the master flip-flop. The capacitors serve to lengthen the time requirements between J or K data and the low to-high clock transition. This feature makes the T100 particularly attractive for applications where clock shew is an important consideration.

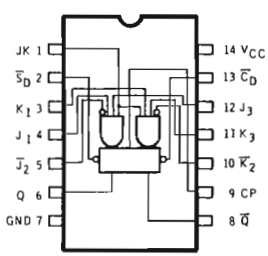
The T101 provides one $\overline{J}$ and one $\overline{K}$ input for additional logic flexibility. It has no master flip-flop capacitors to extend the set-up time and therefore has a higher toggling rate.

The important characteristics of the two flip-flops are illustrated in the following curves and specifications. Noise immunity and operating level curves shown in the gate section of the data sheet are applicable to the flip-flops as well.

CONNECTION DIAGRAMS
(top view)



T 100



T 101

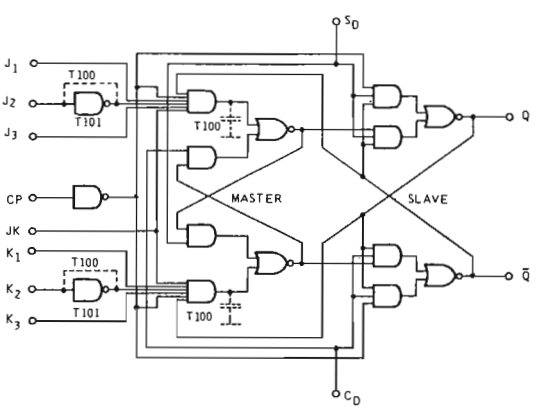
TRUTH TABLES

SYNCHRONOUS ENTRY J - K MODE OPERATION									ASYNCHRONOUS ENTRY Independent of Clock and Synchronous Input			
INPUTS @ t_n							OUTPUTS @ t_{n+1}		INPUTS		OUTPUTS	
		(5)			(5)							
JK	J_1	J_2	J_3	K_1	K_2	K_3	Q	$\bar{Q}$	S_D	C_D	Q	$\bar{Q}$
1	4	5	12	3	10	11	6	8	2	13	6	8
L		X			X		No Change (4)					
H		L			L		No Change (4)		L	L	H	H
H		L			H		L	H	L	H	H	L
H		H			L		H	L	H	L	L	H
H		H			H		Toggles		H	H	No Change	

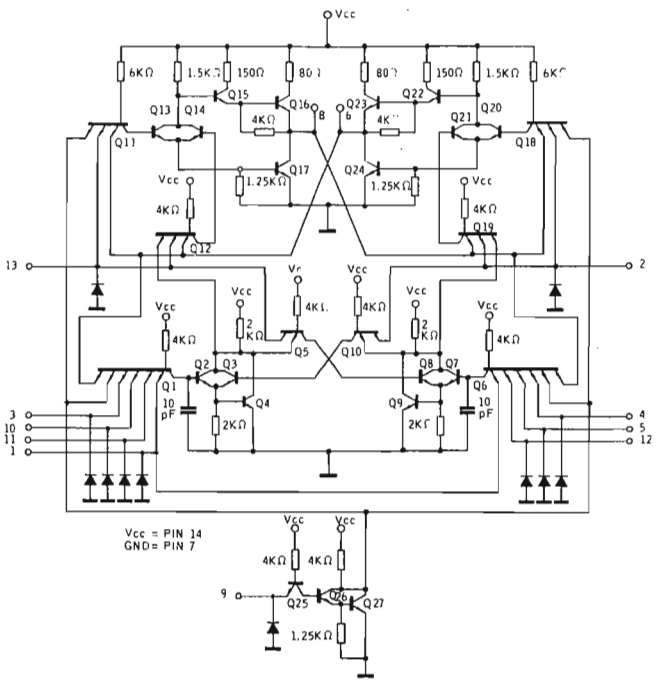
NOTES :

1) H = Most positive logic level.
2) L = Most negative voltage level.
3) X = Could be high or low.
4) For no change of outputs, the J and K inputs of the common JK input must remain low from the time the clock goes low to the time the clock goes high again.
5) The T101 has inverted J_2 (Pin 5) and K_2 (Pin 10) inputs. When not in use, they must be grounded.
6) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is low. The H symbol in the J and K input column is defined as meaning that the input has been high at same time while the clock was low.

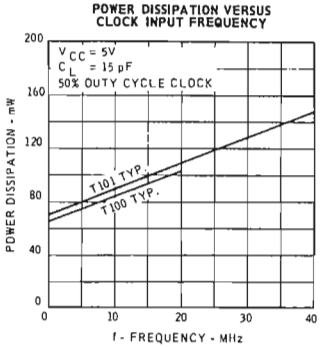
T100 AND T101 FUNCTIONAL LOGIC DIAGRAM



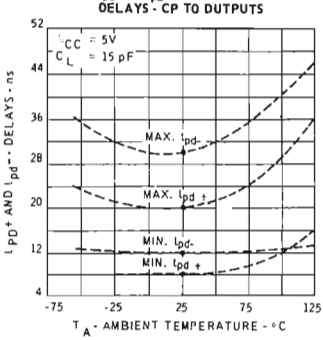
T 100 SCHEMATIC DIAGRAM



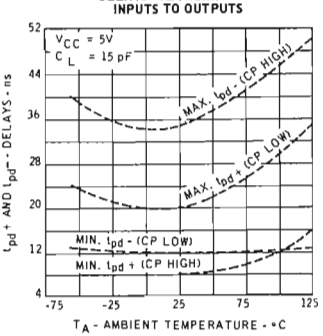
POWER DISSIPATION VERSUS CLOCK INPUT FREQUENCY



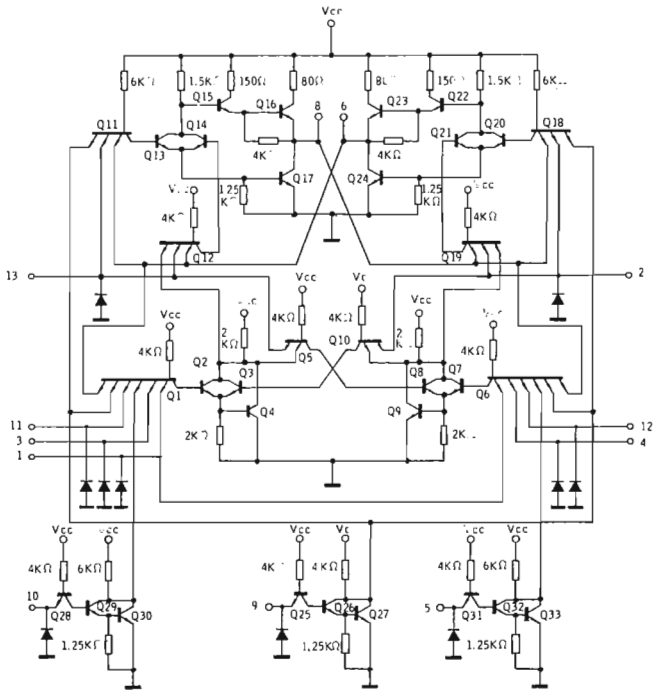
WORST CASE MAX. & MIN. $t_{pd}+$ & $t_{pd}-$ PROPAGATION DELAYS - CP TO OUTPUTS

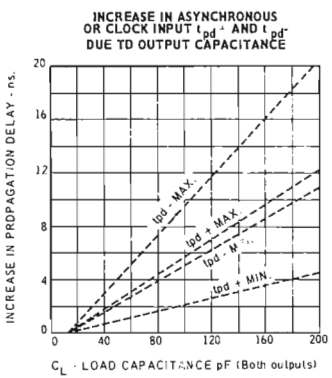


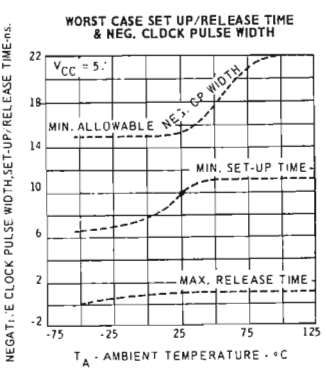
WORST CASE MAX. & MIN. $t_{pd}+$ & $t_{pd}-$ PROPAGATION DELAYS - ASYNCHRONOUS INPUTS TO OUTPUTS



T 101 SCHEMATIC DIAGRAM



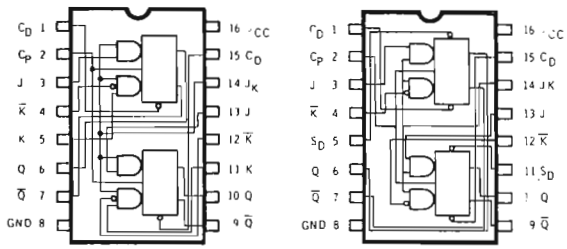




ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.5 V, I_{OH} = -1.2 mA V_{IL} on asynchronous input
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 12.4 mA V_{IH} on asynchronous input V_{CC} = 5.5 V I_{OL} = 16 mA V_{IH} = 5.5 V on asynchronous input
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_R	Input Leakage Current									
	J, K, $\overline{J}$, $\overline{K}$ & Clock Inputs				5	60		60	µA	V_{CC} = 5.5 V V_R = 4.5 V
	J - K Input				10	120		120		Gnd on other inputs
	Asynchronous input				14	162		162		
I_F	Input Load Current									
	J, K, $\overline{J}$, $\overline{K}$ & Clock inputs		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.5V V_F = 0.4V
	J - K Inputs		-3.2		-2	-3.2		-3.2		5.5 V on other
	Asynchronous input		-4.32		-2.7	-4.32		-4.32		inputs
I_{PD}	Power Dissipation Current (each flip-flop)									
	T100		23		13	23		23	mA	V_{CC} = 5 V S_D at ground
	T101		28		14	28		28		
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC} = 5.5 V ground on output and asynchronous input
t_{pd+}	Turn-off delay			8	12	20			nsec	
t_{pd-}	Turn-on delay			12	20	30			nsec	
$t_{release}$	T100			10	18				nsec	
	T101			1	7					V_{CC} = 5 V
t set-up	T100				22	30			nsec	C_L = 15 pF
	T101				8	10				see test circuits and curves
	Negative clock pulse width									
	T100				25				nsec	
	T101				10					
	Toggle frequency									
	T100				20				MHz	
	T101				50					

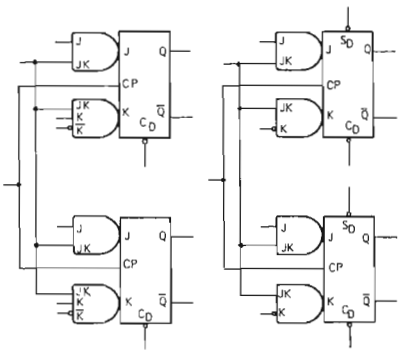
CONNECTION DIAGRAMS
(top view)



T 120 T 121

Available in Dip only

FUNCTIONAL LOGIC DIAGRAMS



T 120 T 121

TRUTH TABLE

SYNCHRONOUS ENTRY J-K MODE OPERATION

T120 INPUTS t_n			T121 INPUTS t_n			OUTPUTS $t_n + 1$	
JK	J	K · $\overline{K}$	JK	J	$\overline{K}$	Q	$\overline{Q}$
14	3(13)	5(11)·4(12)	14	3(13)	4(12)	6(10)	7(9)
L	X	X	L	X	X	No Change	(1)
H	L	L	H	L	H	No Change	(1)
H	L	H	H	L	L	L	H
H	H	L	H	H	H	H	L
H	H	H	H	H	L	Toggles	

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

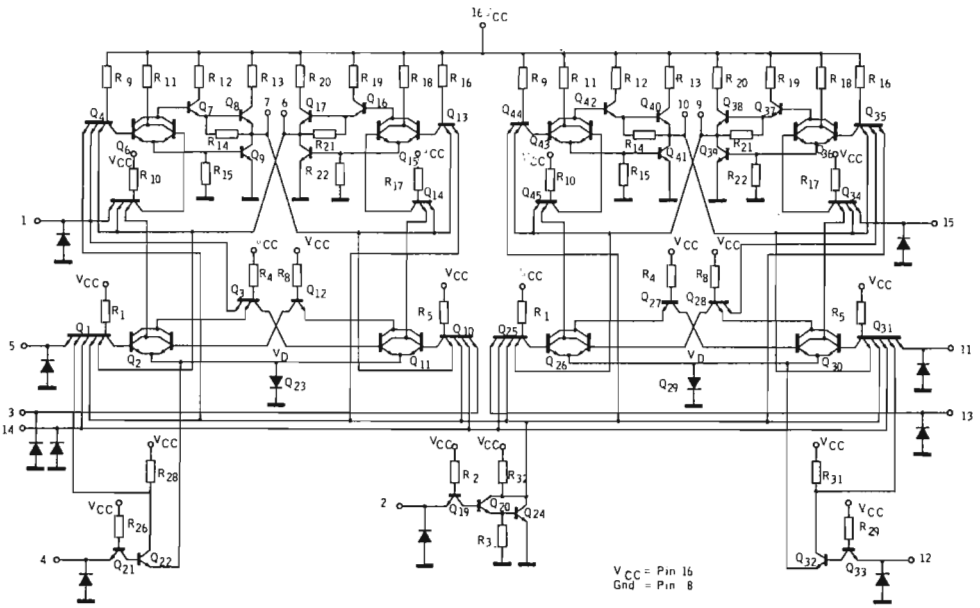
T120 INPUTS	T121 INPUTS		OUTPUTS	
C_D	S_D	C_D	Q	$\overline{Q}$
1(15)	5(11)	1(15)	6(10)	7 (9)
L	H	L	L	H
H	H	H	No Change	
	L	L	H	H
	L	H	H	L

H = Most positive logic level
L = Most negative logic level
X = Could be high or low

NOTES :

1) $\overline{K}$ inputs should be grounded when not in use.
2) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is low. The H symbol in the J and K input column is defined as meaning that the input has been high at same time while the clock was low.

T 120 SCHEMATIC DIAGRAM



NOMINAL COMPONENT VALUES

$R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29}$ = 4 KΩ

R_2, R_3, R_6, R_7 = 2 KΩ

$R_9, R_{16}, R_{28}, R_{31}$ = 6 KΩ

R_{11}, R_{18} = 1.5 KΩ

R_{12}, R_{19} = 150Ω

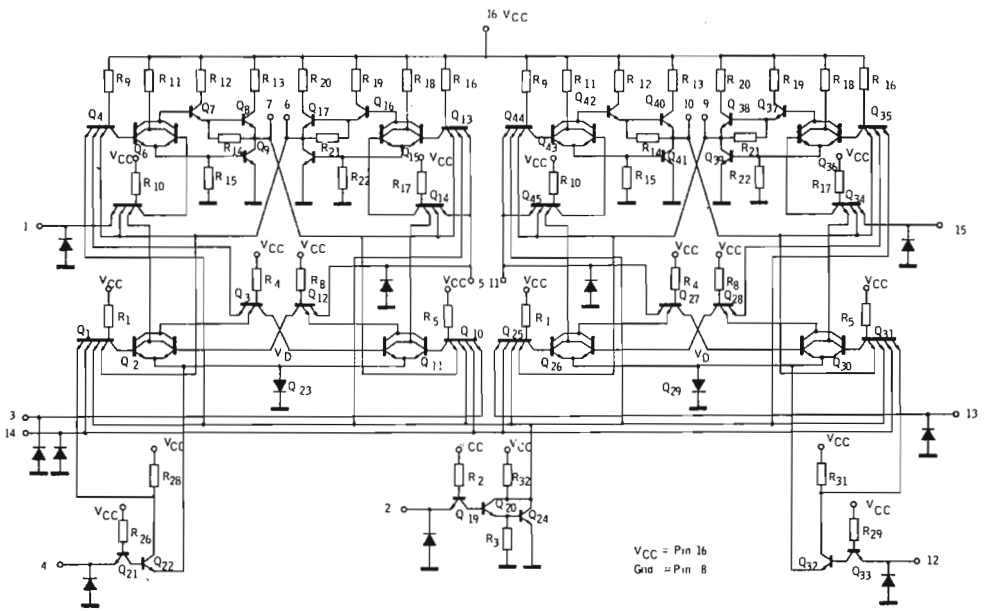
R_{13}, R_{20} = 80Ω

$R_{15}, R_{22}, R_{25}, R_{27}, R_{30}$ = 1.25 KΩ

R_{32} = 1 KΩ

C_1, C_2 = 10 pF

T 121 SCHEMATIC DIAGRAM



NOMINAL COMPONENT VALUES

R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4 KΩ

R_2, R_3, R_6, R_7 = 2 KΩ

R_9, R_{16}, R_{28}, R_{31} = 6 KΩ

R_{11}, R_{18} = 1.5 KΩ

R_{12}, R_{19} = 150Ω

R_{13}, R_{20} = 80Ω

R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25 KΩ

R_{32} = 1 KΩ

C_1, C_2 = 10 pF

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%)

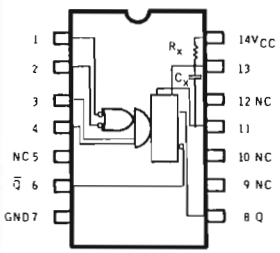
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min. Max.		
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4	V	V_{CC} = 4.5 V I_{OH} = - 1.2 mA V_{IL} on asynchronous input
V_{OL}	Output Low Voltage		0.4		0.21	0.4	0.4	V	V_{CC} = 4.5 V I_{OL} = 12.4 mA V_{IH} on asynchronous input V_{CC} = 5.5 V I_{OL} = 16 mA V_{IH} = 5.5 V on asynchronous input
V_{IH}	Input High Voltage	2		1.7			1.4	V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9	0.8	V	Guaranteed input low threshold for all inputs
I_R	Input Leakage Current								
	J, K and $\overline{K}$ inputs				5	60	60	µA	V_{CC} = 5.5 V
	Clock input				10	120	120		V_R = 4.5 V
	JK input				20	240	240		Ground on other inputs
	Asynchronous inputs				14	160	160		
I_F	Input Load Current								
	J, K and $\overline{K}$ inputs		-1.6		-1.1	-1.6	-1.6	mA	V_{CC} = 5.5 V
	Clock input		-3.2		-2.2	-3.2	-3.2		V_F = 0.4 V
	JK input		-6.4		-4.4	-6.4	-6.4		5.5 V on other inputs
	Asynchronous inputs		-4.32		-3	-4.32	-4.32		
I_{PD}	Power Dissipation Current (each flip-flop)		27		14	27	27	mA	V_{CC} = 5 V C_D at ground
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30 -100	mA	V_{CC} = 5.5 V ground on output and asynchronous input
t_{pd+}	Turn-off delay				8	13	22	nsec	V_{CC} = 5 V C_L = 15 pF see test circuits
t_{pd-}	Turn-on delay				12	21	32	nsec	
t release					1	7		nsec	
t set- up						8	16	nsec	
	Negative Clock Pulse Width					10		nsec	
	Toggle frequency					50		MHz	

EXTENDED TEMPERATURE RANGE

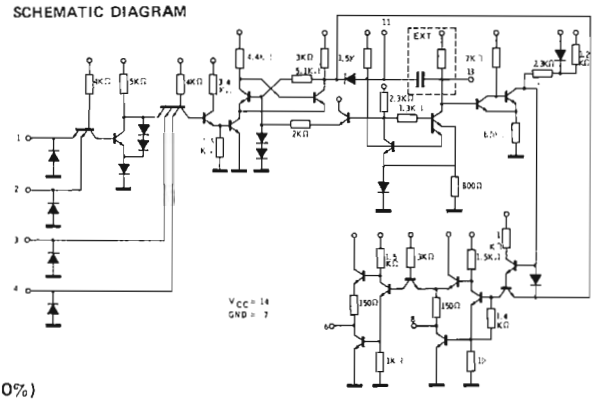
GENERAL DESCRIPTION

This retriggerable monostable multivibrator (or one-shot) provides an output pulse with high accuracy and a very wide duration range (50 nsec to ∞). The T118 will respond to trigger inputs even when already in its active timing state, and will time itself out from the last input pulse received.

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



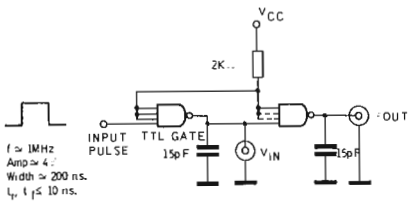
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

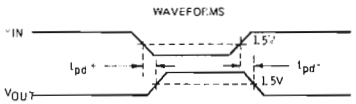
SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		V	V_{CC} = 4.5 V I_{OH} = -1 mA for pin 6 open pin 11 for pin 8 ground pin 11
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 10 mA for pin 6 open pin 11 for pin 8 ground pin 11
V_{IH}	Input High Voltage	2		2	1.7				V	V_{CC} = 4.5 V minimum pulse width 40 nsec
V_{IL}	Input Low Voltage				1.4	0.85		0.85	V	V_{CC} = 5.5 V minimum pulse width 40 nsec
I_F	Input Load Current		-1.6		-1.1	-1.6		-1.6	mA	V_{CC} = 5.5 V V_F = 0.4 V 4.5V on other input
I_R	Input Leakage Current				15	60		60	µA	V_{CC} = 5.5 V V_R = 4.5 V ground on other input
I_{PD}	Power Dissipation Current		25			25		25	mA	V_{CC} = 5.5 V ground on true inputs and 4.5V on complemented inputs
t_{pd+}	Negative trigger input to Q output				25	50			nsec	V_{CC} = 5V R_X = 5 KΩ C_X = 0 C_L = 15 pF see test circuit
t_{pd-}	Negative trigger input to $\bar{Q}$ output				25	50			nsec	
t_{pw}	Min Q output pulse width (1)				45	65			nsec	
C_{stray}	Max. allowable Wiring Cap (pin 13)		50			50		50	pF	Gnd on pin 13 This capacitance, if present, will add to C_X in determining output pulse width
R_X	Timing Resistor (2)	5	20	5		20	5	20	KΩ	

Notes : 1) Pulse width calculation : $T_{pw} = 0.36\ R_X\ C_X$.
2) Unless otherwise noted, 10 KΩ resistor (R_X) is placed between Pin 13 and V_{CC} for all tests.

SWITCHING TIME TEST CIRCUITS

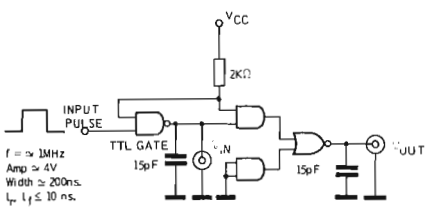
T102 - T103 - T104 - T107 - T109 - T116 t_{pd} TEST CIRCUIT

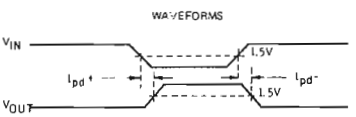




NOTE Capacitance includes probe and jig capacity

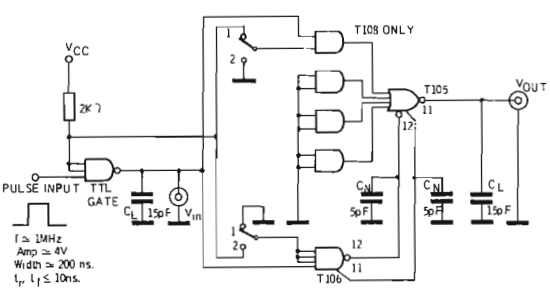
t_{pd} TEST CIRCUIT T105-T115 NONEXPANDABLE SECTION ONLY





NOTE Capacitance includes probe and jig capacity

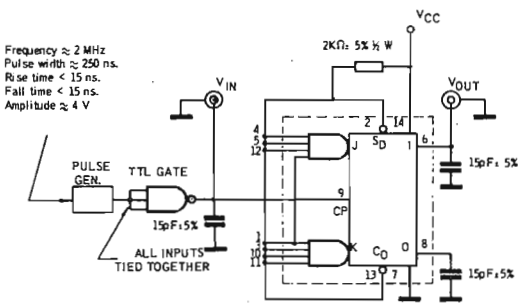
t_{pd} TEST CIRCUIT T105-T108 EXPANDABLE GATE AND T106 EXPANDER

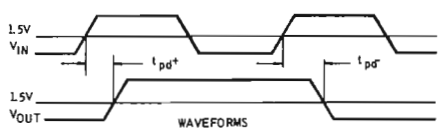


NOTE
With switch in position 1 measure t_{pd} of T105 · With switch in position 2 measure t_{pd} (T105 · T108) + Δt_{pd} (T10[illegible] · Capacitance includes probe and jig capacitances.

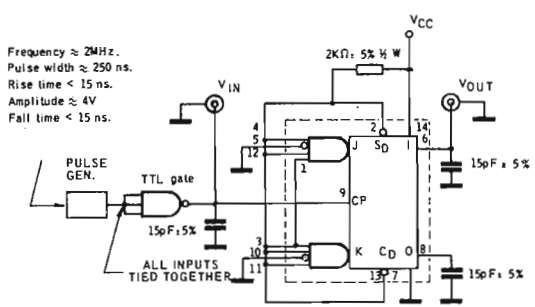
SWITCHING TIME TEST CIRCUITS

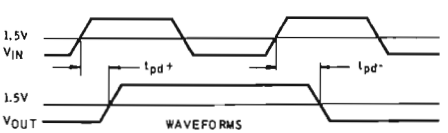
T100 t_{pd} TEST CIRCUIT





T101 t_{pd} TEST CIRCUIT





SWITCHING NOTES

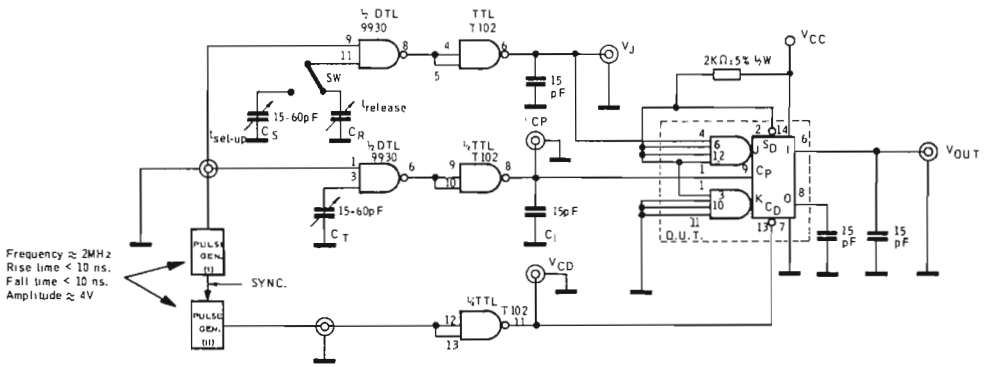
1) The load capacitance indicated in test circuits includes the capacitance of probe and jig.

2) Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and D.C. loading is very small.

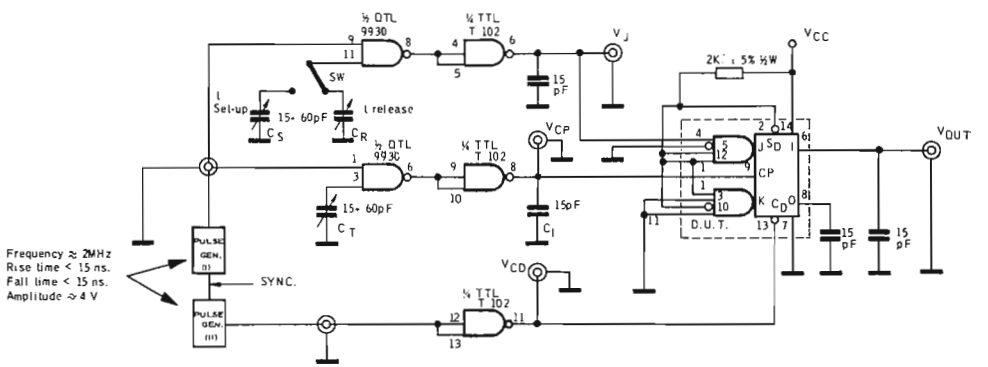
3) Allowable clock skew ≤ t_{pd} + (max) + $t_{release}$ (min.).

SWITCHING TIME TEST CIRCUITS

T100 t_{set-up} and $t_{release}$ TEST CIRCUIT



T101 t_{set-up} and $t_{release}$ TEST CIRCUIT

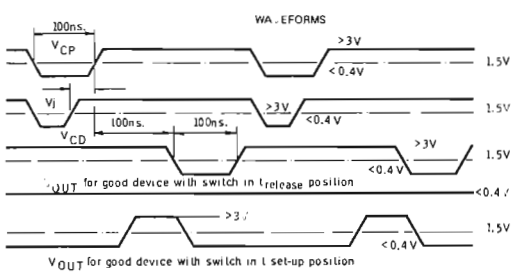


INITIAL ADJUSTMENT

1. With switch in t release position adjust pulse generators, C_T & C_R for proper V_{CP}, V_J & V_D waveforms and t release limit value.
2. With switch in t set-up position adjust C_S for t set-up limit value.

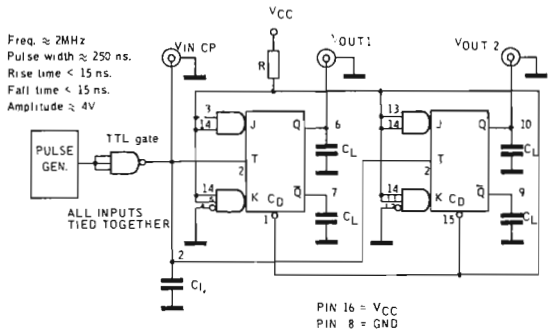
t set-up is defined as the minimum time required for a High to be present at a synchronous logic input at any time during the low state of the clock in order for the flip-flop to respond to the data.

t release is defined as the maximum time allowed for a High to be present at a synchronous logic input at any time during the low state of the clock and not be recognized.

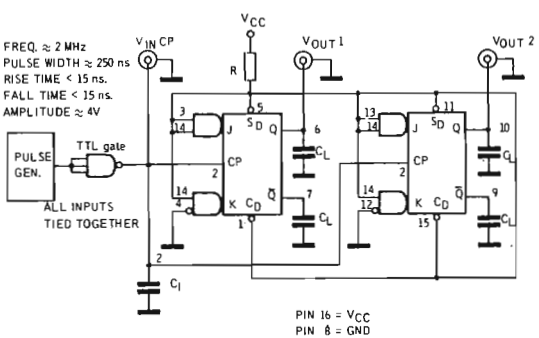


SWITCHING TIME TEST CIRCUITS

T120 t_{pd} TEST CIRCUIT



T121 t_{pd} TEST CIRCUIT

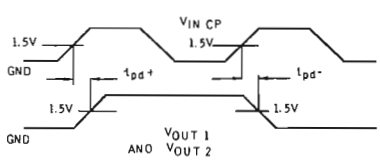


R = 2KΩ, ± 5%, 1/2W
C_I = 15 pF ± 5%
C_L = 15 pF ± 5%

C_I & C_L include all probe and jig capacity. Very short stranded or printed wire should be used for all interconnections.
Probes should be connected directly to the input & output pins.

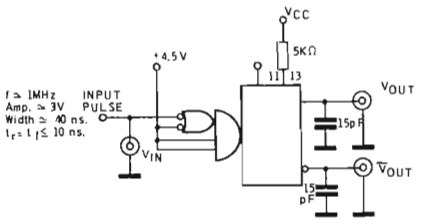
NOTE :
For $t_{set\text{-}up}$ and $t_{release}$ see T 100 and T 101 test circuits.

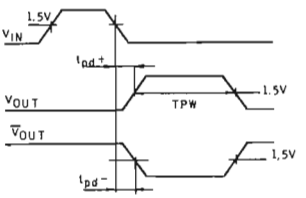
WAVEFORMS



SWITCHING TIME TEST CIRCUITS

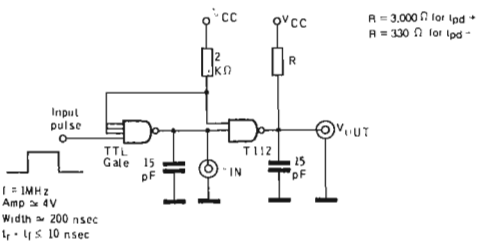
T118 t_{pd} TEST CIRCUIT

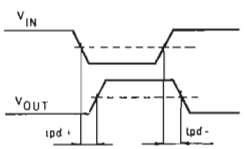




Note: Capacitance includes jig and probe capacity.

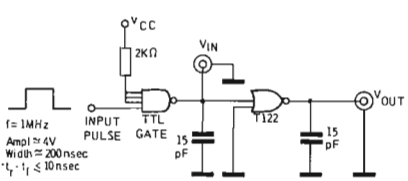
T112 t_{pd} TEST CIRCUIT

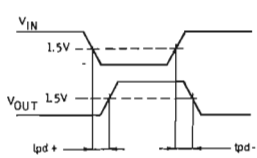




Note : capacitance includes probe and jig capacity.

T122 t_{pd} TEST CIRCUIT





NOTE: Capacitance includes probe and jig capacity.

Transistor-transistor logic

STANDARD TEMPERATURE RANGE, 0°C to 75°C

- COMPATIBLE WITH DTL AND LPDTL PRODUCTS
- INPUT DIODE CLAMPING
- NOISE IMMUNITY, 1 V
- WORST CASE NOISE IMMUNITY, 0.4 V
- OUTPUT DRIVE CAPABILITY OF 10
- POWER DISSIPATION, 11 mW PER GATE
- GATE PROPAGATION DELAY OF 6 nsec
- ACTIVE PULL-UP OUTPUT CIRCUIT
- SAME PIN CONFIGURATION AS THE CORRESPONDING DTL AND LPDTL PRODUCTS

The Transistor - Transistor Logic integrated circuit family (TTL) combines a high fan-out, high noise immunity, low power dissipation and good capacitive load driving capability with low propagation delay times.
The circuits are fabricated within a silicon monolithic substrate using planar epitaxial processes.
These devices are available in the following packages: ceramic DIP (14 or 16 leads), plastic DIP (14 or 16 leads), flat ceramic package.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

V_{CC} Pin Potential to Ground	-0.5V to 8V
Input Voltage (see note 1)	-0.5V to 5.5V
Gate Output Voltage, Inputs Low	-0.5V to V_{CC}
Gate Current into Output Terminal, Inputs High (except T109)	50 mA
Gate Current into Output Terminal, Inputs High T109	100 mA
Flip-Flop Output Voltage when Output is normally High	-0.5V to V_{CC}
Flip-Flop Current into Output Terminal when Output is normally Low	50 mA
Storage Temperature, Plastic	-55°C to 125°C
Storage Temperature, Ceramic	-65°C to 150°C
Temperature (Amb.) Under Bias, Ceramic	-55°C to 125°C

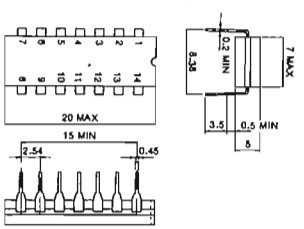
ORDERING NUMBERS

T1XXD1 for ceramic DIP
T1XXB1 for plastic DIP
T1XXF1 for flat package

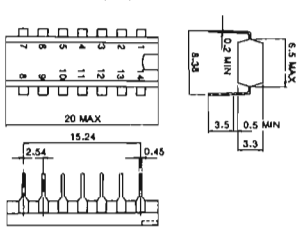
OPERATING CONDITIONS

Temperature Range	0°C to 75°C
Supply Voltage	5V ± 5%

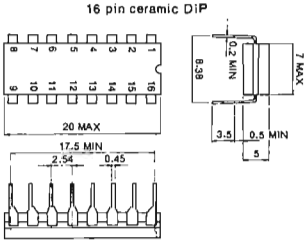
PHYSICAL DIMENSIONS
14 pin ceramic DIP



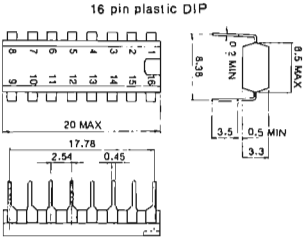
PHYSICAL DIMENSIONS
14 pin plastic DIP



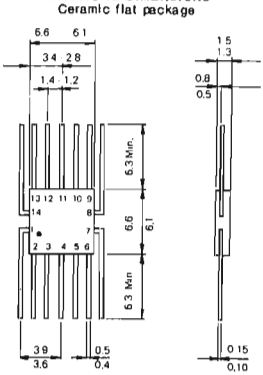
PHYSICAL DIMENSIONS
16 pin ceramic DIP



PHYSICAL DIMENSIONS
16 pin plastic DIP

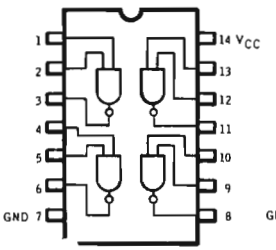


PHYSICAL DIMENSIONS
Ceramic flat package

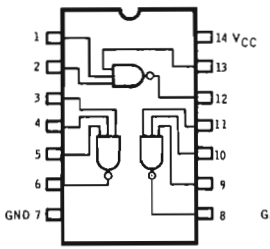


NOTE: all dimensions in mm.

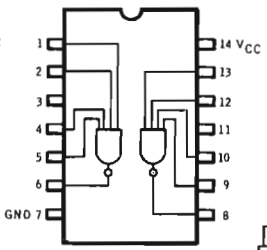
CONNECTION DIAGRAMS (top view)



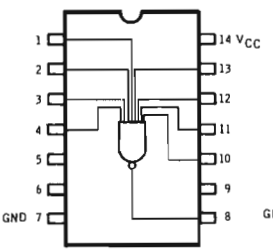
T 102



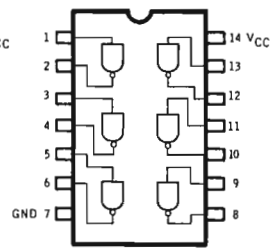
T 103



T 104

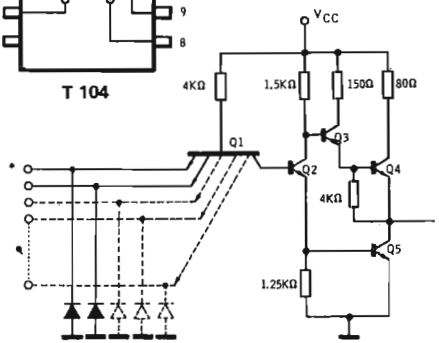


T 107



T 116

EQUIVALENT CIRCUI
(one gate only)

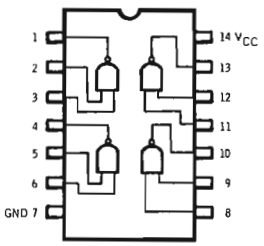


* Number of inputs depends on the gat

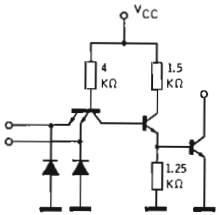
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.1		2.4		V	V_{CC} = 4.75V I_{OH} = -1.2 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 5.25 V I_{OL} = 16 mA V_{CC} = 4.75 V I_{OL} = 14.1 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.25 V V_F = 0.45 V V_R = 5.25 V on other inputs
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25 V V_R = 4.5 V Gnd on other inputs.
I_{PD}	Power Dissipation Current (each gate)		6.1		3.6	6.1		6.1	mA	V_{CC} = 5 V inputs open
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25 V inputs and output grounded
t_{pd+}	Turn-off Delay			3		13			nsec	V_{CC} = 5 V C_L = 15 pF See test circuit
t_{pd-}	Turn-on Delay			3		15			nsec	

CONNECTION DIAGRAM
(top view)



EQUIVALENT CIRCUIT
(one gate only)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 5.25V I_{OL} = 16 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.25V V_F = 0.45V V_R = 5.25V on other input
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25V V_R = 4.5V ground on other input
I_{CEX}	Output Leakage Current					200		200	μA	V_{CC} = 4.75V inputs guaranteed 4.5V applied to output
I_{PD}	Power Dissipation Current (each gate)		6.1		3.6	6.1		6.1	mA	V_{CC} = 5V inputs open
t_{pd+}	Turn-off Delay					35			nsec	V_{CC} = 5V
t_{pd-}	Turn-on Delay					15			nsec	C_L = 15 pF see test circuit

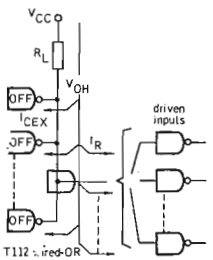
WIRED-OR APPLICATIONS

The T112 allows wired-OR operation when a proper load resistor (R_L) is connected between V_{CC} and output pins. Ge
eral rules to calculate the allowed number of wired-OR gates with a requested drive factor are explained below.
For a given number (K) of wired-OR gates a given number (n) of driven gates, two equations can be written in order t
determine the value of the external resistor (R_L) that guarantees a correct operation with respect to the same nois
immunity levels as the TTL family.

High Level: if all the wired-OR gates outputs are at the high level, a total current flows from supply through the external resistor R_L, that is the sum of the output leakage current I_{CEX} of the output wired-OR transistor and the input leakage current I_R of the driven gates. This current takes the output voltage to a value that should not be less than the V_{OH} voltage that guarantees the high level noise immunity. Therefore, to limit this voltage drop, the following R_L limitation should be respected:

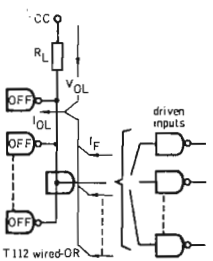
$$R_{Lmax} = \frac{V_{CC} - V_{OH}}{K I_{CEX} + n\, I_R}$$

note that the resulting R_L value is a worst case as I_{CEX} given in present data sheet is measured at 4.5V instead of 2.4V. Besides even I_R is measured at 4.5V.



Low Level: when almost one of the wired-OR gates is at the low level (ON), a current flow from supply, through R_L, to the output of the ON transistor. This current is the ratio of R_L and the allowed voltage drop, (the output leakage current of the OFF wired-OR gates is negligible). In addition, the output ON transistor sinks the output load current I_F of the driven inputs. The V_{OL} voltage guarantees the low level noise immunity, that is total sunk current should not overcome I_{OL} value; therefore, to limit the current through R_L, following limitation should be respected:

$$R_{Lmin} = \frac{V_{CC} - V_{OL}}{I_{OL} - n\, I_F}$$



If more than one gate is ON, allowed R_L value is higher.
The two combined equations give maximum and minimum values among which should range R_L value:

$$\frac{V_{CC}-V_{OL}}{I_{OL}-nI_F} \le R_L \le \frac{V_{CC}-V_{OH}}{K I_{CEX} + n\, I_R}$$

n = number of driven inputs

K = number of wired-OR T112 gates

DRIVING TTL LOADS

The adjoining table gives minimum and maximum resistance values to be used when one or more wired-OR T112s are driving TTL loads. When K (1 to 10) T112s are wired-OR and at the same time n TTL gates are driven, the resistance value to be externally connected to the output should be comprised between minimum and maximum given values. The table is calculated for the worst case of all the electrical parameters shown in the equations and the noise immunity of the TTL family is widely respected.

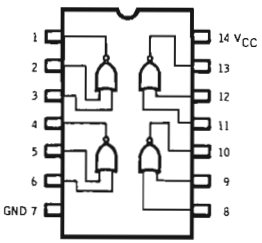
STANDARD TEMPERATURE RANGE (0°C to 75°C)

n	R_{min}	R_{max}									
		K=1	K=2	K=3	K=4	K=5	K=6	K=7	K=8	K=9	K=10
1	330	9040	5100	3560	2740	2220	1870	1610	1420	1260	1140
2	375	7340	4500	3260	2560	2100	1780	1500	1370	1220	1110
3	428	6180	4050	3010	2400	1990	1710	1490	1320	1190	1080
4	500	5340	3700	2800	2260	1900	1630	1430	1280	1150	1050
5	600	4700	3380	2610	2140	1810	1570	1380	1240	1120	1020
6	750	4200	3100	2450	2030	1730	1510	1340	1200	1090	995
7	1000	3790	2880	2300	1930	1650	1450	1290	1170	1060	X
8	1500	3460	2680	2180	1840	1590	X	X	X	X	X
9	3000	3180	X	X	X	X	X	X	X	X	X
10	∞	X	X	X	X	X	X	X	X	X	X

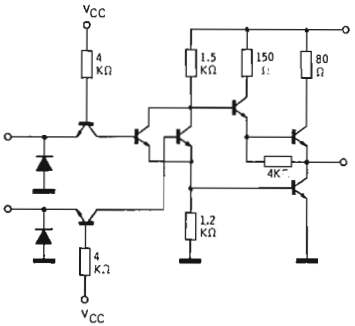
X means not allowed
n = number of driven TTL gates
K = number of T112s wired-OR

driven gate: I_F = 1.6 mA
I_R = 60 μA
V_{OH} = 2.4V

CONNECTION DIAGRAM
(top view)



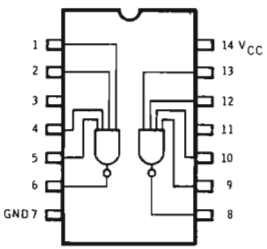
EQUIVALENT CIRCUIT
(one gate only)



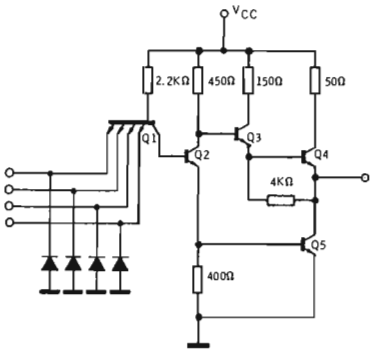
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.75V I_{OH} = -1.2 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 5.25V I_{OL} = 16 mA V_{CC} = 4.75V I_{OL} = 14.1 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.25V V_F = 0.45V 5.25V on other inputs
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25V V_R = 4.5V
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25V inputs and output grounded
I_{PD}	Power Dissipation Current (each gate)		6.1		3.6	6.1		6.1	mA	V_{CC} = 5V inputs open
t_{pd+}	Turn-off Time					13			nsec	V_{CC} = 5V C_L = 15 pF see test circuit
t_{pd-}	Turn-on Time					15			nsec	

CONNECTION DIAGRAM
(top view)



EQUIVALENT CIRCUIT
(one gate only)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%)

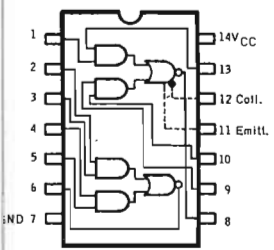
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.75V I_{OH} = -3.6 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 5.25V I_{OL} = 48 mA V_{CC} = 4.75V I_{OL} = 42.3 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-3.2		-2	-3.2		-3.2	mA	V_{CC} = 5.25V V_F = 0.45V V_R = 5.25V on other inputs
I_R	Input Leakage Current				25	120		120	μA	V_{CC} = 5.25V V_R = 4.5V Gnd on other inputs
I_{PD}	Power Dissipation Current (each gate)		14		8.6	14		14	mA	V_{CC} = 5V open
I_{SC}	Output Short-Circuit Current	-40	-150	-40		-150	-40	-150	mA	V_{CC} = 5.25V inputs and output grounded
t_{pd+}	Turn-off Delay			3		17			nsec	V_{CC} = 5V C_L = 15 pF See test circuit
t_{pd-}	Turn-on Delay			2		13			nsec	

AND-NOR gates **T105 - T108 - T115**, expander **T106**

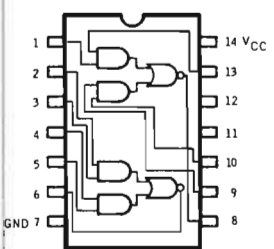
STANDARD TEMPERATURE RANGE

The TTL T105 and T108 are AND – NOR gates which may be NOR expanded with the use of the T106 element.

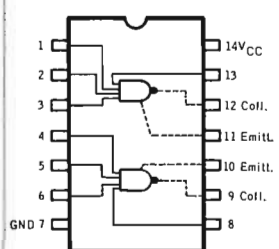
CONNECTION DIAGRAMS
(top view)



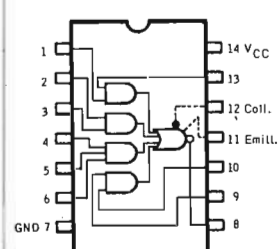
T 105



T 115

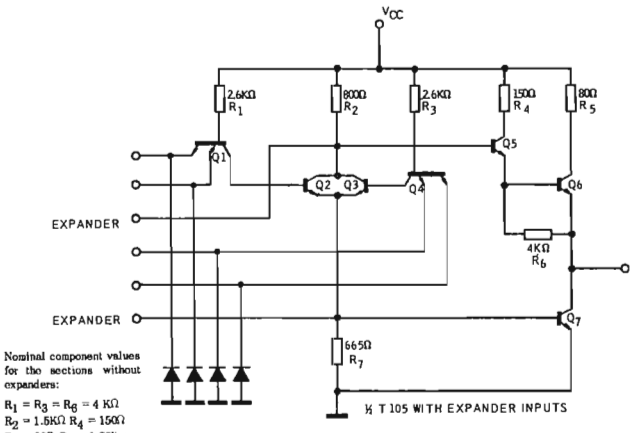


T 106



T 108

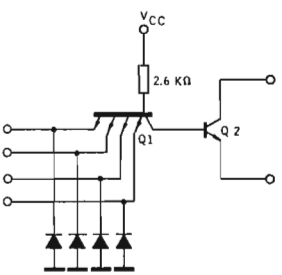
EQUIVALENT CIRCUITS



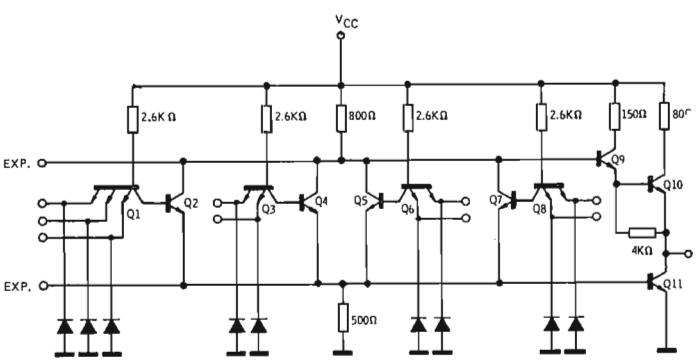
Nominal component values for the sections without expanders:

$R_1 = R_3 = R_6 = 4\ K\Omega$
$R_2 = 1.5K\Omega$ $R_4 = 150\Omega$
$R_5 = 80\Omega$ $R_7 = 1.25K..$

T 105 - T 115



T 106 (one gate)



T 108

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		V	V_{CC} = 4.75V I_{OH} = -1.2 mA V_{IL} see below
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC} = 5.25V I_{OL} = 16 mA V_{IH} = 5.25V V_{CC} = 4.75V I_{OL} = 14.1 mA V_{IH} see below
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current T105 (non exp.section) and T115 T105 (exp.section) T106 and T108		-1.6 -2.4		-1.04 -1.65	-1.6 -2.4		-1.6 -2.4	mA mA	V_{CC} = 5.25V V_F = 0.45V 5.25V on other inputs
I_R	Input Leakage Current T105 (non exp.section) and T115 T105 (exp.section) T106 and T108				5 15	60 90		60 90	μA μA	V_R = 4.5V V_{CC} = 5.25V Gnd on all other inputs
I_{PD}	Power Dissipation Current T105 T115 T108		21.3 15.4 17.7		12.1 9 9.3	21.3 15.4 17.7		21.3 15.4 17.7	mA mA mA	V_{CC} = 5V All inputs open
ΔI_{PD}	Extra Current Drain when one T106 expander is attached to a T105 "on"		2.05		1.08	2.05		2.05	mA	V_{CC} = 5V All inputs high
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25V inputs and output grounded
t_{pd+}	Turn-off Delay			3		15			nsec	T105 (non expandable section) and T115
t_{pd-}	Turn-on Delay			3		15			nsec	V_{CC} = 5V C_L = 15pF see test circuit
t_{pd+}	Turn-off Delay			3		18			nsec	T105 (expandable section) and T108
t_{pd-}	Turn-on Delay			3		13			nsec	V_{CC} = 5V C_L = 15pF see test circuit
Δt_{pd+}	Turn-off Delay			-2		5			nsec	T106 only - The T106 is tested by measuring its t_{pd} through the T105 - see test circuit.
Δt_{pd-}	Turn-on Delay			-2		5			nsec	

GENERAL DESCRIPTION

The TTL family includes the T100 and T101 flip-flops to satisfy the storage element needs of a logic system. Each is a master-slave J-K flip-flop with the same multi-emitter inputs and low impedance active pull-up outputs common to the gate elements.

The internal J-K connections assure the user of non-ambiguous operation for all input states. The master-slave design with buffered clock input offers high noise immunity, low clock loading and eliminates the need for careful control of clock pulse rise or fall times. Data is accepted by the master when the clock is in the low logic state. Transfer from master to slave occurs when the clock goes from the low to the high logic level. When the clock is in the high logic level both J and K inputs are inhibited. For this reason it is desirable to maintain the clock pulse in the high level most of the duty cycle. Direct set and reset inputs provide true asynchronous control of both master and slave flip-flops independent of logic and clock input levels.

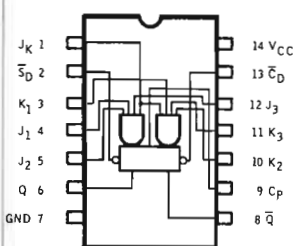
A common J-K input is provided which is useful in the physical layout of most logic configurations.

The two circuits are almost identical. The T100 has capacitors at the outputs of the J and K data input gates in the master flip-flop. The capacitors serve to lengthen the time requirements between J or K data and the low to high clock transition. This feature makes the T100 particularly attractive for applications where clock skew is an important consideration.

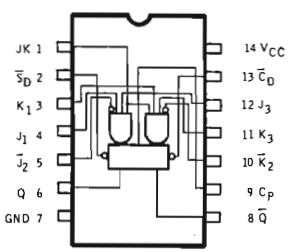
The T101 provides one $\overline{J}$ and one $\overline{K}$ input for additional logic flexibility. It has no master flip-flop capacitors to extend the set-up time and therefore has a higher toggling rate.

The important characteristics of the two flip-flops are illustrated in the following curves and specifications. Noise immunity and operating level curves shown in the gate section of the data sheet are applicable to the flip-flops as well.

CONNECTION DIAGRAMS
(top view)

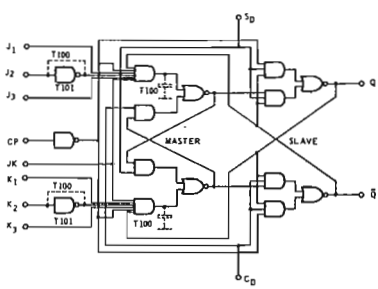


T 100



T 101

FUNCTIONAL LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS ENTRY
J-K MODE OPERATION

INPUTS @ t_n							OUTPUTS @ t_{n+1}	
JK 1	J_1 4	J_2 5	J_3 12	K_1 3	K_2 10	K_3 11	Q 6	$\overline{Q}$ 8
L		X			X		No Change (note 4)	
H		L			L		No Change (note 4)	
H		L			H		L	H
H		H			L		H	L
H		H			H		Toggles	

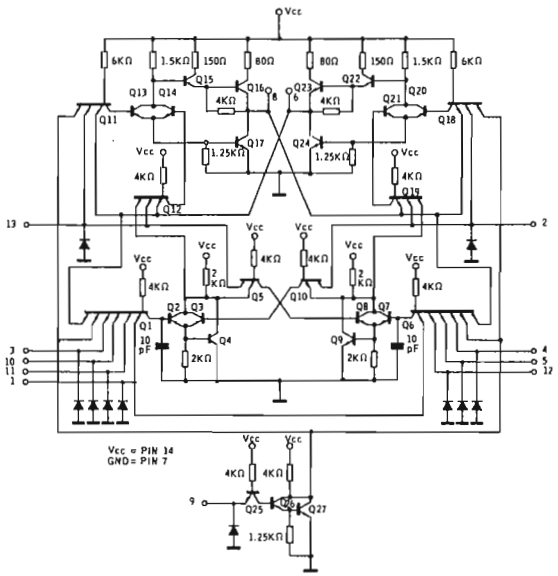
ASYNCHRONOUS ENTRY
Independent of Clock and Synchronous Input

INPUTS		OUTPUTS	
S_D 2	C_D 13	Q 6	$\overline{Q}$ 8
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

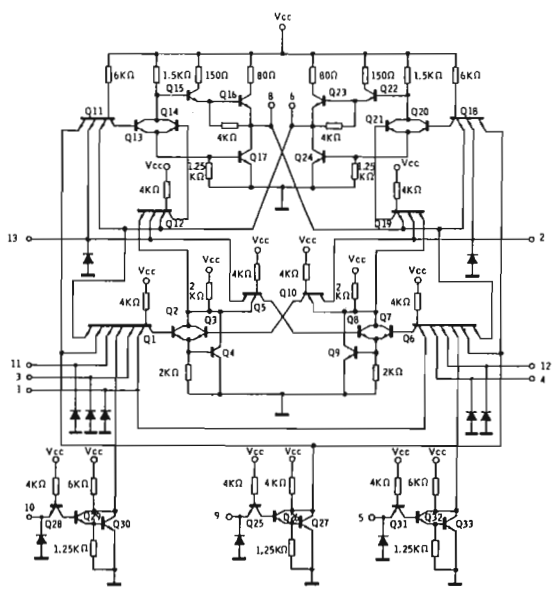
NOTES:

1) H = Most positive logic level.
2) L = Most negative voltage level.
3) X = Could be high or low.
4) For no change of outputs, the J and K inputs of the common J-K input must remain low from the time the clock goes low to the time the clock goes high again.
5) The T101 has inverted J_2 (Pin 5) and K_2 (Pin 10) inputs. When not in use, they must be grounded.
6) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is low. The H symbol in the J and K input column is defined as meaning that the input has been high at same time as the clock was low.

T100 EQUIVALENT CIRCUIT



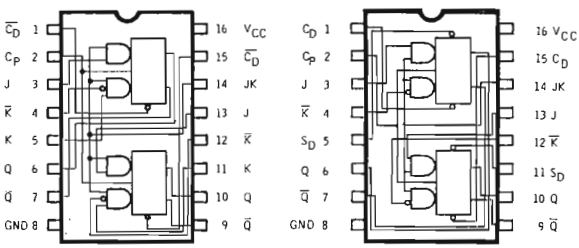
T101 EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC} = 4.75V I_{OH} = -1.2 mA V_{IL} on asynchronous input
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 4.75V I_{OL} = 14.1 mA V_{IH} on asynchronous input V_{CC} = 5.25V I_{OL} = 16 mA V_{IH} = 5.25V on asynchronous input
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_R	Input Leakage Current J, K, $\overline{J}$, $\overline{K}$ & Clock Inputs J - K input Asynchronous Input				5 10 14	60 120 162		60 120 162	μA	V_{CC} = 5.25V V_R = 4.5V Gnd on other inputs
I_F	Input Load Current J, K, $\overline{J}$, $\overline{K}$ & Clock Inputs J - K input Asynchronous Input		-1.6 -3.2 -4.32		-1 -2 -2.7	-1.6 -3.2 -4.32		-1.6 -3.2 -4.32	mA	V_{CC} = 5.25V V_F = 0.45V 5.25V on other inputs
I_{PD}	Power Dissipation Current (each flip-flop) T100 T101		28 33		14 16	28 33		28 33	mA	V_{CC} = 5V S_D at ground
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25V ground on output and asynchronous input
t_{pd+}	Turn-off Delay			8	12	20			nsec	V_{CC} = 5V C_L = 15 pF see test circuits
t_{pd-}	Turn-on Delay			12	20	30			nsec	
$t_{release}$	T100 T101			10 1	18 7				nsec	
t_{set-up}	T100 T101				22 8	35 15			nsec	
	Negative Clock Pulse Width T100 T101				25 10				nsec	
	Toggle Frequency T100 T101				20 50				MHz	

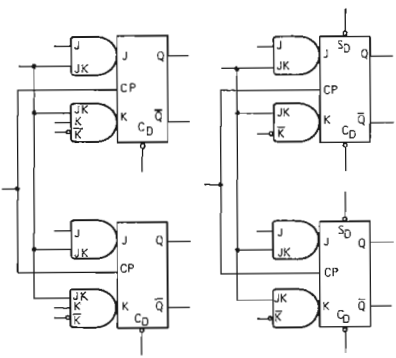
CONNECTION DIAGRAMS
(top view)



T 120 T 121

Available in DIP only

FUNCTIONAL LOGIC DIAGRAMS



T 120 T 121

TRUTH TABLES

SYNCHRONOUS ENTRY J-K MODE OPERATION

T120 INPUTS @ t_n			T121 INPUTS @ t_n			OUTPUTS @ t_{n+1}	
JK	J	K · $\overline{K}$	JK	J	$\overline{K}$	Q	$\overline{Q}$
14	3(13)	5(11)·4(12)	14	3(13)	4(12)	6(10)	7(9)
L	X	X	L	X	X	No Change (note 5)	
H	L	L	H	L	H	No Change (note 5)	
H	L	H	H	L	L	L	H
H	H	L	H	H	H	H	L
H	H	H	H	H	L	Toggles	

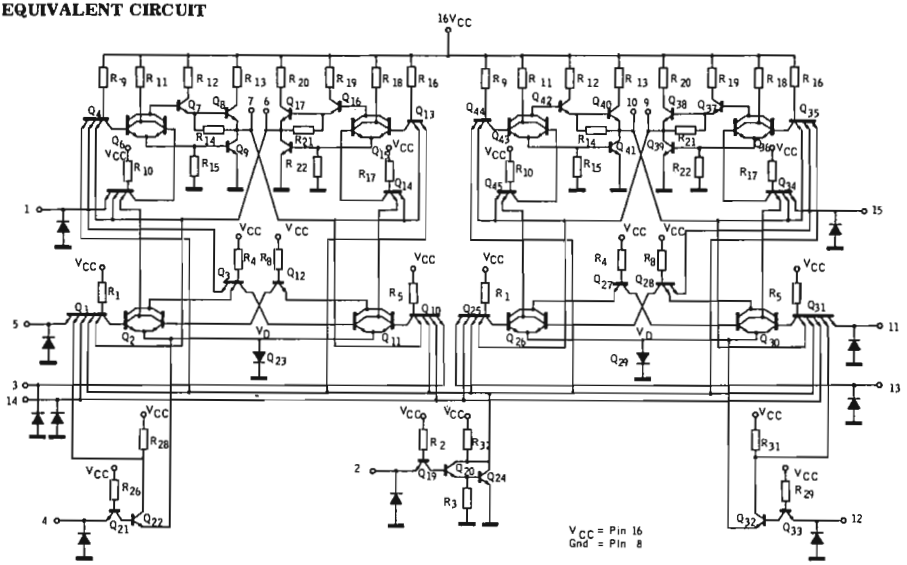
ASYNCHRONOUS ENTRY
Independent of Clock and Synchronous Input

T120 INPUTS	T121 INPUTS		OUTPUTS	
C_D	S_D	C_D	Q	$\overline{Q}$
1(15)	5(11)	1(15)	6(10)	7(9)
L	H	L	L	H
H	H	H	No Change	
	L	L	H	H
	L	H	H	L

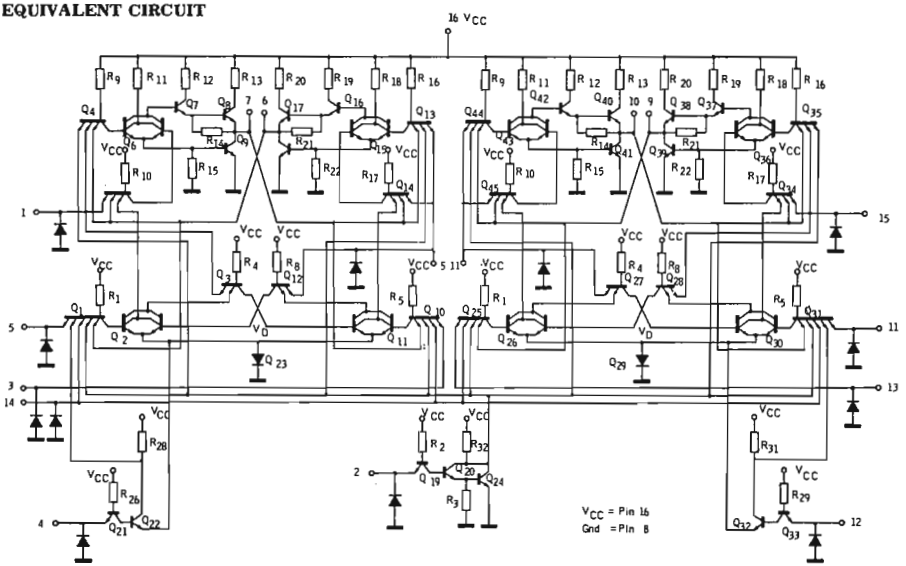
NOTES:

1) H = Most positive logic level
2) L = Most negative logic level
3) X = Could be high or low
4) $\overline{K}$ inputs should be grounded when not in use
5) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is low. The H symbol in the J and K input column is defined as meaning that the input has been high at same time as the clock was low.

T120 EQUIVALENT CIRCUIT



T121 EQUIVALENT CIRCUIT



NOMINAL COMPONENTS VALUES (Both diagrams)

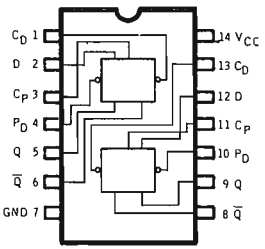
$R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4\,k\Omega$; $R_2, R_3, R_6, R_7 = 2\,k\Omega$; $R_9, R_{16}, R_{28}, R_{31} = 6\,k\Omega$

$R_{11}, R_{18} = 1.5\,k\Omega$; $R_{12}, R_{19} = 150\,\Omega$; $R_{13}, R_{20} = 80\,\Omega$; $R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25\,k\Omega$; $R_{32} = 1\,k\Omega$; $C_1, C_2 = 10\,pF$

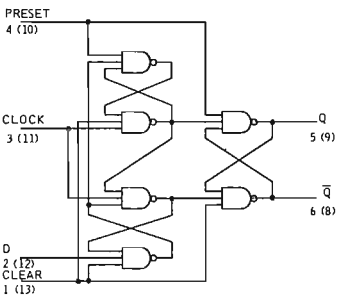
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS							UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C			
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC} = 4.75V I_{OH} = -1.2 mA V_{IL} on asynchronous input
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 4.75V I_{OL} = 14.1 mA V_{CC} = 5.25V I_{OL} = 16 mA V_{IH} on asynchronous input
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_R	Input Leakage Current									
	J, K and $\overline{K}$ Inputs				5	60		60	μA	V_{CC} = 5.25V
	Clock Input				10	120		120		V_R = 4.5V
	J-K Input				20	240		240		Ground on other inputs
	Asynchronous Input				14	160		160		
I_F	Input Load Current									
	J, K and $\overline{K}$ Inputs		-1.6		-1.1	-1.6		-1.6	mA	V_{CC} = 5.25V
	Clock Input		-3.2		-2.2	-3.2		-3.2		V_F = 0.45V
	J-K Input		-6.4		-4.4	-6.4		-6.4		5.25V on other inputs
	Asynchronous Input		-4.32		-3	-4.32		-4.32		
I_{PD}	Power Dissipation Current (each flip-flop)		30			30		30	mA	V_{CC} = 5V C_D at ground
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25V ground on output and asynchronous input
t_{pd+}	Turn-off Delay			8	13	22			nsec	V_{CC} = 5V C_L = 15 pF see test circuit
t_{pd-}	Turn-on Delay			12	21	32			nsec	
$t_{release}$				1	7				nsec	
$t_{set\text{-}up}$					8	16			nsec	
	Negative Clock Pulse Width				10				nsec	
	Toggle Frequency				50				MHz	

CONNECTION DIAGRAM
(top view)



FUNCTIONAL LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS ENTRY D MODE OPERATION

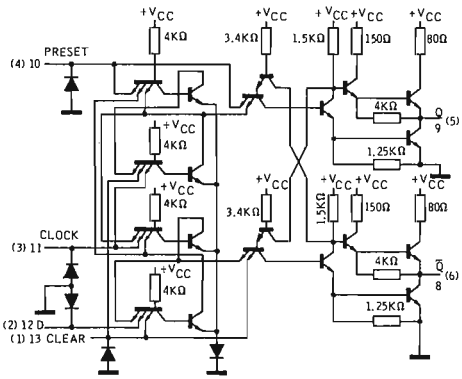
INPUTS @ t_n	OUTPUTS @ t_n+1	
D 2(12)	Q 5(9)	$\overline{Q}$ 6(8)
L	L	H
H	H	L

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
Clear 1(13)	Preset 4(10)	Q 5(9)	$\overline{Q}$ 6(8)
L	L	H	H
L	H	L	H
H	L	H	L
H	H	No Change	

H = Most positive logic level
L = Most negative logic level

EQUIVALENT CIRCUIT
(one side only)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%)

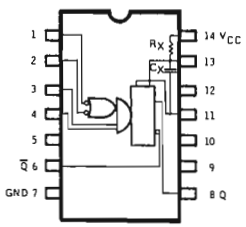
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC} = 4.75V I_{OH} = -0.6 mA V_{IL} on asynchronous input
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC} = 5.25V I_{OL} = 16 mA V_{IH} on asynchronous input
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current D and P_D Inputs C_P and C_D Inputs		-1.6 -3.2		-1	-1.6 -3.2		-1.6 -3.2	mA	V_{CC} = 5.25V V_F = 0.45V other inputs high
I_R	Input Leakage Current D Input C_P and P_D Inputs C_D Input		60 120 180			60 120 180		60 120 180	μA	V_{CC} = 5.25V V_R = 4.5V
I_{PD}	Power Dissipation Current (each flip-flop)		12			12		12	mA	Ground on C_D V_{CC} = 5V
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25V ground on output and synchronous input
t_{pd1+}	Turn-off Delay			10	20	35			nsec	D input
t_{pd1-}	Turn-on Delay			10	20	50			nsec	D input
t_{pd2+}	Turn-off Delay					25			nsec	C_D, S_D inputs
t_{pd2-}	Turn-on Delay					40			nsec	C_D, S_D inputs
t_{set-up}	Set-up Time					20			nsec	
$t_{release}$	Release Time			5					nsec	
	Clock Frequency			15					MHz	

V_{CC} = 5V, C_L = 15pF, see test circuits

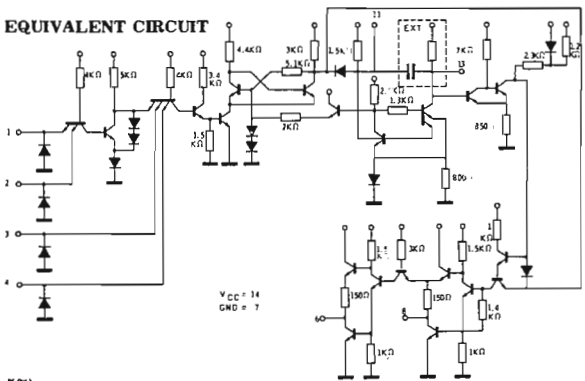
GENERAL DESCRIPTION

This retriggerable monostable multivibrator (or one-shot) provides an output pulse with high accuracy and a very wide duration range (50 nsec to ∞). The T118 will respond to trigger inputs even when already in its active timing state, and will time itself out from the last input pulse received.

CONNECTION DIAGRAM
(top view)



EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		V	V_{CC} = 4.75V I_{OH} = -0.72 mA for pin 6 open pin 11 for pin 8 ground pin 11
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC} = 4.75V I_{OL} = 13 mA for pin 6 ground pin 11 for pin 8 open pin 11
V_{IH}	Input High Voltage	2		2	1.7				V	V_{CC} = 4.75V minimum pulse width 40 nsec
V_{IL}	Input Low Voltage				1.4	0.8		0.8	V	V_{CC} = 5.25V minimum pulse width 40 nsec
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.25V V_F = 0.45V 4.5V on other input
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25V V_R = 4.5V ground on other input
I_{PD}	Power dissipation Current		25			25		25	mA	V_{CC} = 5.25V ground on true inputs and 4.5V on complemented inputs
t_{pd+}	Negative Trigger Input to Q Output				25	50			nsec	V_{CC} = 5V R_X = 5 KΩ C_X = 0 C_L = 15 pF see test circuit
t_{pd-}	Negative Trigger Input to Q̄ Output				25	50			nsec	
t_{pw}	Min Q Output Pulse Width (1)				45	65			nsec	
C_{stray}	Max. Allowable Wiring Cap (pin 13)		50			50		50	pF	Gnd on pin 13 This capacitance, if present, will add to C_X in determining output pulse width
R_X	Timing Resistor (2)	5	40	5		40	5	40	KΩ	

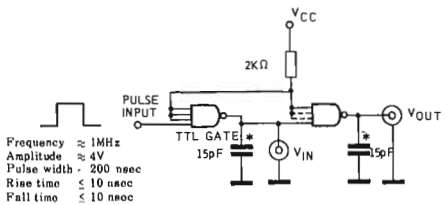
NOTES:

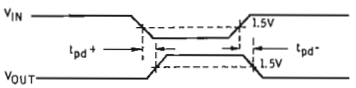
1) Pulse width calculation: $T_{pw} \simeq 0.36\ R_x\ C_x$.
2) Unless otherwise noted, 10 KΩ resistor (R_X) is placed between Pin 13 and V_{CC} for all tests.

SWITCHING TIME TEST CIRCUITS

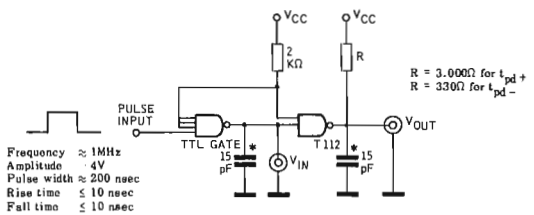
-Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and DC loading is very small.

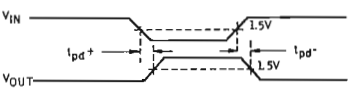
T102 - T103 - T104 - T107 - T109 - T116 t_{pd} TEST CIRCUIT AND WAVEFORMS



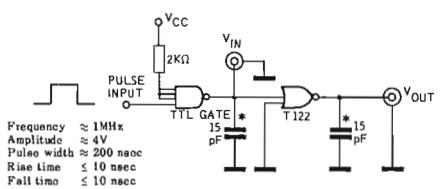


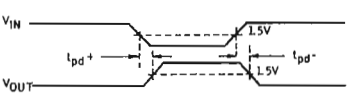
T112 t_{pd} TEST CIRCUIT AND WAVEFORMS



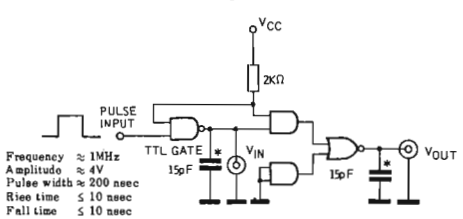


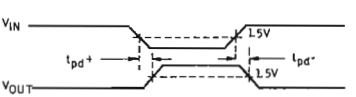
T122 t_{pd} TEST CIRCUIT AND WAVEFORMS





T105 and T115 t_{pd} TEST CIRCUIT (NON-EXPANDABLE SECTION ONLY) AND WAVEFORMS



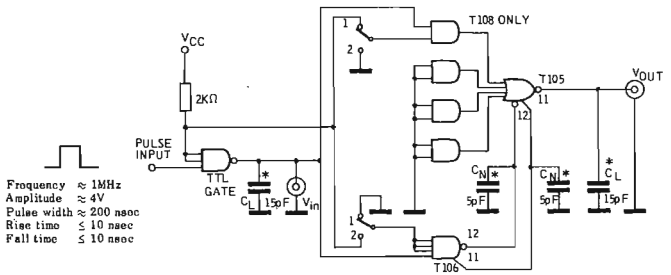


* Capacitance includes probe and Jig capacity.

SWITCHING TIME TEST CIRCUITS

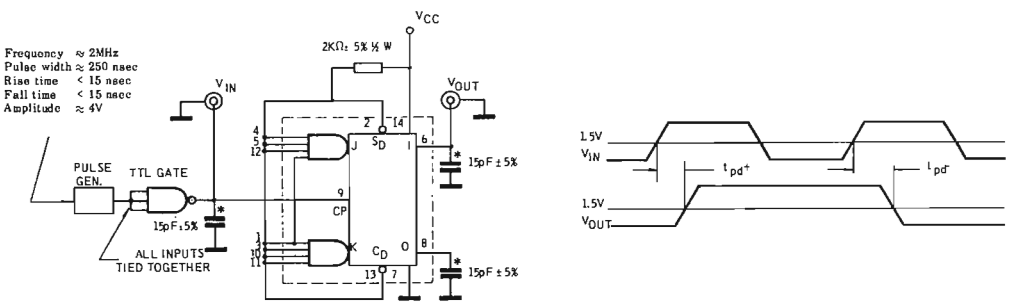
- Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and DC loading is very small.
- For Flip-Flops allowable clock skew ≤ t_{pd} (max) + $t_{release}$ (min).

T105-T108 EXPANDABLE GATE AND T106 EXPANDER t_{pd} TEST CIRCUIT

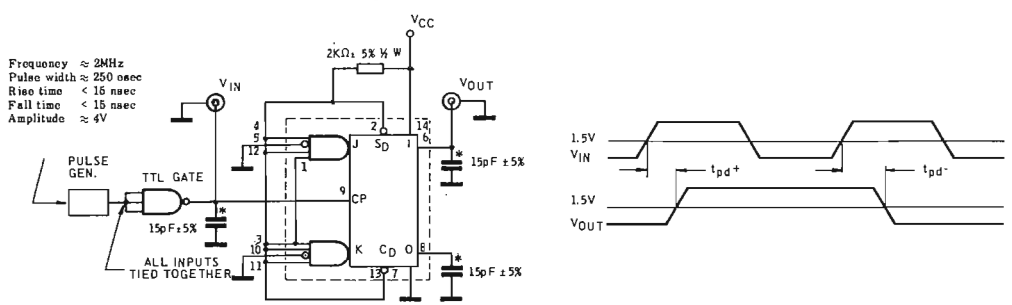


With switch in position 1 measure t_{pd} of T105 - With switch in position 2 measure t_{pd} (T105 - T108) + Δt_{pd} (T106).

T100 t_{pd} TEST CIRCUIT AND WAVEFORMS



T101 t_{pd} TEST CIRCUIT AND WAVEFORMS

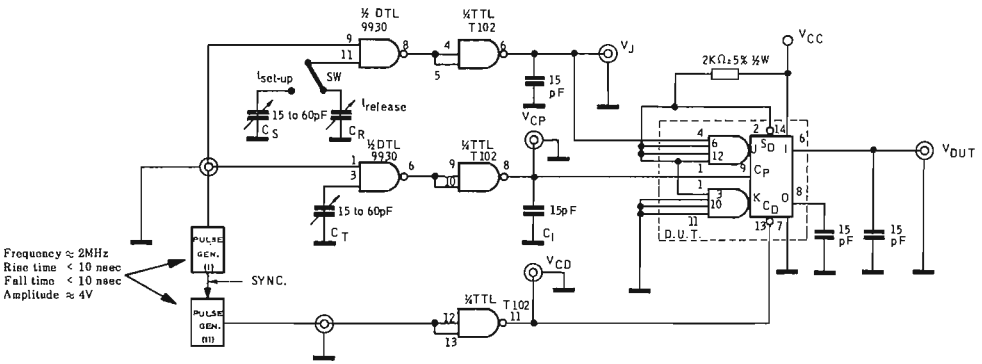


* Capacitance includes probe and Jig capacity.

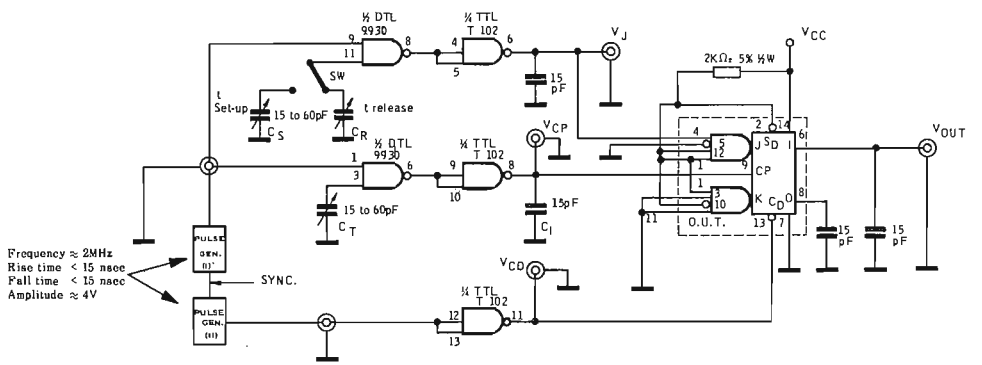
SWITCHING TIME TEST CIRCUITS

- Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and D C loading is very small.
- Allowable clock skew ≤ t_{pd} (max) + $t_{release}$ (min).

T100 $t_{set\text{-}up}$ and $t_{release}$ TEST CIRCUIT



T101 $t_{set\text{-}up}$ and $t_{release}$ TEST CIRCUIT

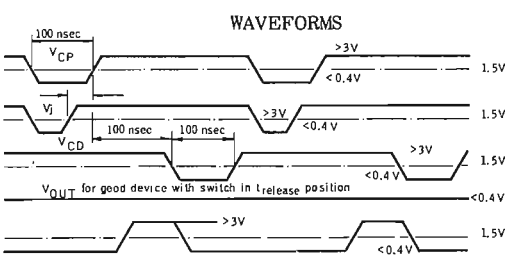


INITIAL ADJUSTMENT

1. With switch in $t_{release}$ position adjust C_T & C_R for proper V_{CP}, V_J & V_D waveforms and $t_{release}$ limit value.
2. With switch in $t_{set\text{-}up}$ position adjust C_S for $t_{set\text{-}up}$ limit value.

$t_{set\text{-}up}$ is defined as the minimum time required for a High to be present at a synchronous logic input at any time during the low state of the clock in order for the flip-flop to respond to the data. $t_{release}$ is defined as the maximum time allowed for a High to be present at a synchronous logic input at any time during the low state of the clock and not be recognized.

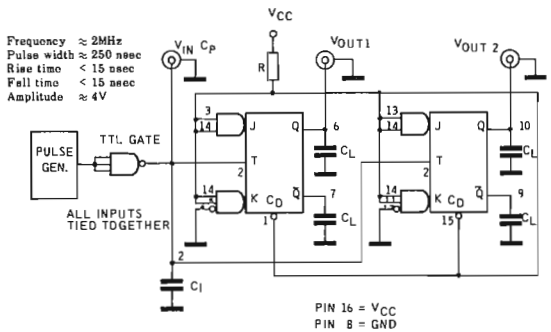
WAVEFORMS



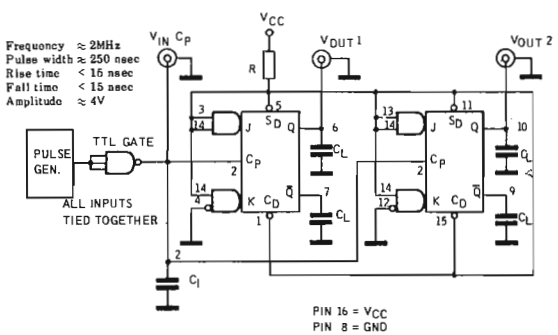
SWITCHING TIME TEST CIRCUITS

- Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and D C loading is very small.
- Allowable clock skew ≤ t_{pd} (max) + $t_{release}$ (min).

T120 t_{pd} TEST CIRCUIT



T121 t_{pd} TEST CIRCUIT



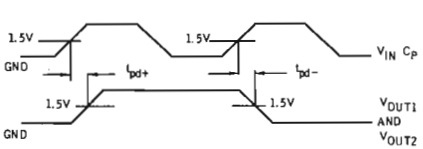
R = 2KΩ ± 5% 1/2W
C_I = 15 pF ± 5%
C_L = 15 pF ± 5%

C_I & C_L include all probe and jig capacity. Very short stranded or printed wire should be used for all interconnections. Probes should be connected directly to the input & output pins.

NOTE:

For $t_{set\text{-}up}$ and $t_{release}$ see T100 and T101 test circuits.

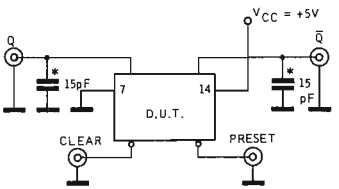
WAVEFORMS

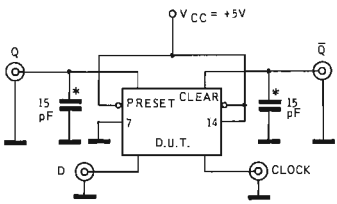


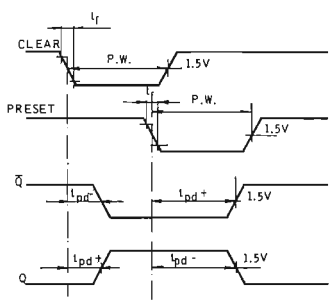
SWITCHING TIME TEST CIRCUITS

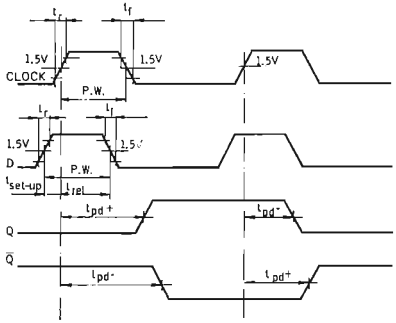
- Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and D C loading is very small.
- Allowable clock skew ≤ t_{pd} (max) + $t_{release}$ (min).

T110 t_{pd} TEST CIRCUIT AND WAVEFORMS









Clear: t_f =3 to 6 nsec P.W.=30 nsec f=1 MHz
Amplitude = 0.4 to 2.4 V.

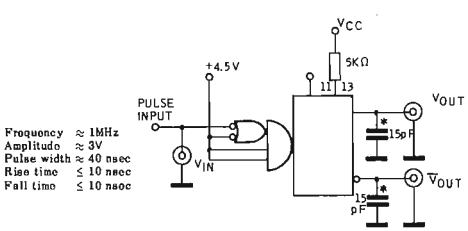
Preset: t_f=3 to 6 nsec P.W.=30 nsec f=1 MHz
Amplitude = 0.4 to 2.4 V.

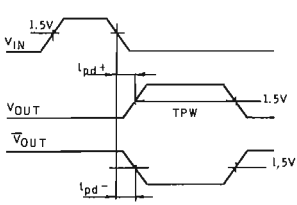
Clock: t_r=15 nsec t_f=15 nsec P.W.=30 nsec f=1 MHz
Amplitude = 0.4 to 2.4 V.

D: t_r=15 nsec t_f= 15 nsec P.W.=25 nsec $t_{set\text{-}up}$=20 nsec
$t_{rel.}$=5 nsec f = 500 kHz Amplitude = 0.4 to 2.4 V.

NOTE:
This Jig is used to test the minimum clock frequency.

T118 t_{pd} TEST CIRCUIT AND WAVEFORMS





* Capacitance includes probe and Jig capacity.

4-bit shift register

EXTENDED TEMPERATURE RANGE -55°C to 125°C
STANDARD TEMPERATURE RANGE 0°C to 75°C

- INPUT DIODE CLAMPING
- 20 MHz SHIFT FREQUENCY
- SYNCHRONOUS PARALLEL ENTRY
- J, $\overline{K}$ INPUTS TO FIRST STAGE
- ASYNCHRONOUS COMMON RESET
- POWER DISSIPATION OF 300 mW
- CERAMIC HERMETIC AND PLASTIC 16 PIN DUAL IN-LINE PACKAGE

The T 150 4-bit shift-register is constructed on a single silicon chip using the planar epitaxial process. The T 150 has serial and parallel entry, serial and parallel output and Master Reset (MR). Serial input is provided as a J and $\overline{K}$ input, which may be tied together externally to form a "D" input. The MR input clears all stages independent of clock pin level. A logic HIGH on the PE input ensures serial shift operation and a logic LOW enables parallel entry concurrent with low to high transition on the clock input. The J and $\overline{K}$ inputs make the circuit useful as a 4-bit modulo N counter ($N \leqslant 15$) needing only one additional gate element. The circuit utilizes TTL logic for high speed and high fan-out capability.

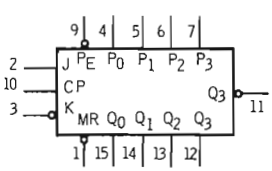
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage, Continuous	-0.5V to 7V
Input Voltage	-0.5V to 5.5V
Output Voltage	-0.5V to V_{CC}
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

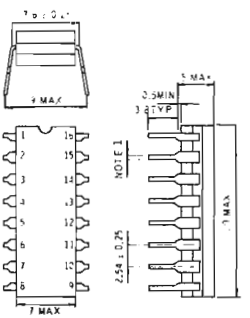
Extended	
Temperature Range	-55°C to 125°C
Supply Voltage	5V ± 10 %
Standard	
Temperature Range	0°C to 75°C
Supply Voltage	5V ± 5%

LOGIC DIAGRAM AND PIN CONNECTION



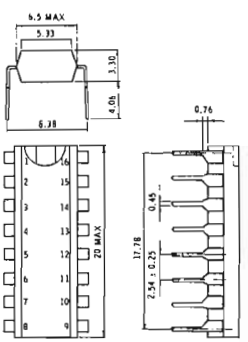
V_{CC} = PIN 16
GND = PIN 8

PHYSICAL DIMENSIONS
16 pin ceramic DIP



NOTES:
1) Board-drilling dimensions should equal your practice for a conventional 0,51 mm. diameter lead.
2) All dimensions in mm.

PHYSICAL DIMENSIONS
16 pin plastic DIP



NOTE: All dimensions in mm.

ORDERING NUMBERS

T 150 D1 (For Ceramic DIP and Standard Temperature Range)
T 150 D2 (For Ceramic DIP and Extended Temperature Range)
T 150 B1 (For Plastic DIP and Standard Temperature Range)

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						Unit	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V V_{CC}=4.75V I_{OH}= -0.36 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V V_{CC}=5.25V I_{OL}= 9.6 mA
									V_{CC}=4.75V I_{OL}= 8.5 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		V Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		- 1	-1.6		-1.6	mA V_{CC}=5.25V V_F = 0.45V other inputs high
I_F	Input Load Current (CP)		-6.4		- 4	-6.4		-6.4	mA V_{CC}=5.25V V_F = 0.45V other inputs high
I_F	Input Load Current (PE)		-3.7		-2.3	-3.7		-3.7	mA V_{CC}=5.25V V_F = 0.45V other inputs high
I_R	Input Leakage Current		60		15	60		60	µA V_{CC}=5.25V V_R = 4.5V
I_R	Input Leakage Current (CP)		240		45	240		240	µA V_{CC}=5.25V V_R = 4.5V
I_R	Input Leakage Current (PE)		140		35	140		140	µA V_{CC}=5.25V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-10	-70	-10		-70	-10	-70	mA V_{CC}= 7V 1.5V on output and 5.25V on P input
I_{PD}	Power Dissipation Current		85			85		85	mA V_{CC}= 5V

ELECTRICAL CHARACTERISTICS (T_A = -55°C to 125°C, V_{CC} = 5V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						Unit	CONDITIONS AND COMMENTS
		-55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V V_{CC}=4.5V I_{OH}= -0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	V V_{CC}=5.5V I_{OL}= 9.6 mA
									V_{CC}=4.5V I_{OL}= 7.5 mA
V_{IH}	Input High Voltage	2		1.7			1.4		V Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1.1	-1.6		-1.6	mA V_{CC}=5.5V V_F = 0.4V other inputs high
I_F	Input Load Current (CP)		-6.4		-4.2	-6.4		-6.4	mA V_{CC}=5.5V V_F = 0.4V other inputs high
I_F	Input Load Current (PE)		-3.7		-2.5	-3.7		-3.7	mA V_{CC}=5.5V V_F = 0.4V other inputs high
I_R	Input Leakage Current		60		15	60		60	µA V_{CC}=5.5V V_R = 4.5V
I_R	Input Leakage Current (CP)		240		45	240		240	µA V_{CC}=5.5V V_R = 4.5V
I_R	Input Leakage Current (PE)		140		35	140		140	µA V_{CC}=5.5V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-10	-70	-10		-70	-10	-70	mA V_{CC}= 7V 1.5V on output and 5.5V on P input
I_{PD}	Power Dissipation Current		85			85		85	mA V_{CC}= 5V

FUNCTIONAL DESCRIPTION

CP (common clock input) - shift or parallel entry operation occurs during low to high transition.
$\overline{PE}$ (parallel entry enable) - for parallel entry operation $\overline{PE}$ must be low; for shift operation it must be high.
$\overline{MR}$ (Master Reset) - when $\overline{MR}$ is low, all Q outputs are low independently of the condition of any other inputs.

J, $\overline{K}$ = serial inputs
P_0, P_1, P_2, P_3 = parallel inputs
Q_3, $\overline{Q}_3$ = serial outputs
Q_0, Q_1, Q_2, Q_3 = parallel outputs

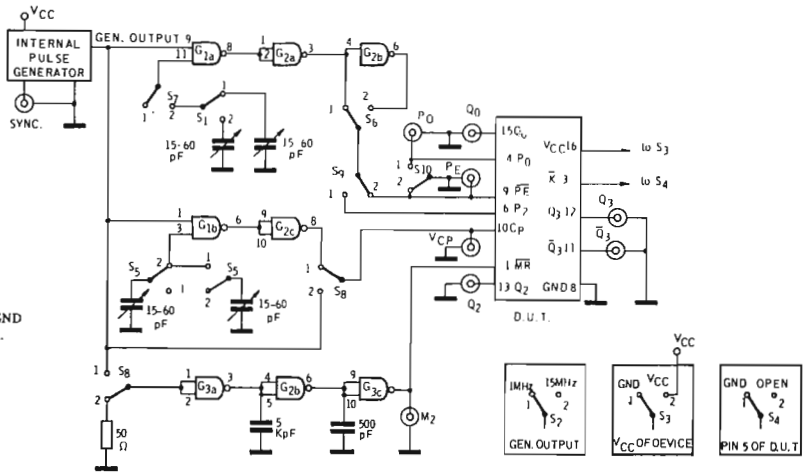
LOADING RULES (1 U.L. = 1 TTL Gate Input Unit Load)

INPUTS :	J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2, P_3	LOADING FACTOR :	1 U.L.
	$\overline{PE}$		2.3 U.L.
	CP		4 U.L.
OUTPUTS:	Q_0, Q_1, Q_2, Q_3, $\overline{Q}_3$	DRIVE FACTOR :	6 U.L.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	Min	Typ.	Max.	UNIT	CONDITIONS AND COMMENTS
t_{pd+}	Turn-Off Delay	10	20	35	ns	V_{CC} = 5V C_L = 15pF (see figures)
t_{pd-}	Turn-On Delay	10	25	45	ns	
CP_{pw}	Clock Pulse Width	35			ns	
t_s	Set-up Time		17		ns	
t_r	Release Time		17		ns	
$t_{s(\overline{PE})}$	Set-up Time for $\overline{PE}$		26		ns	
$t_{r(\overline{PE})}$	Release Time for $\overline{PE}$		26	10	ns	
$t_{pd-(\overline{MR})}$	Reset Time for $\overline{MR}$		35		ns	
$t_{rec(\overline{MR})}$	Recovery Time for $\overline{MR}$		20		ns	
$\overline{MR}_{pw}$	Min. Reset Pulse Width		15		ns	

T150 SWITCHING TEST JIG

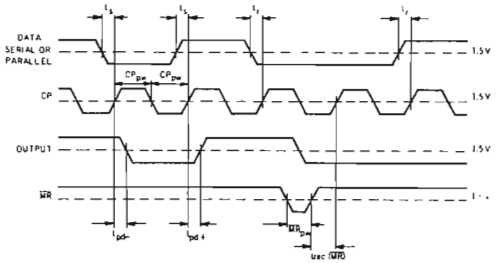


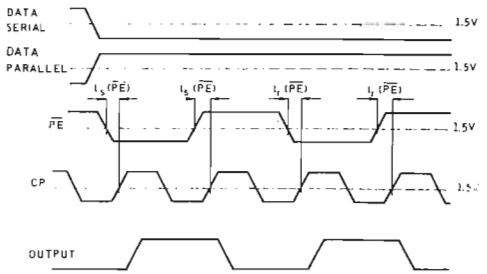
NOTES
G_1 = 9930
G_2 = T102
G_3 = T102
V_{CC} = 5V
S_3 is used for GND reference check.

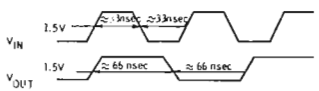
TABLE TO BE USED TO CHECK JIG FOR CALIBRATION

Test Type	Switch Numbers										Probe "A"	Probe "B"	TEST POINT LIMITATIONS V_{CC} = 5V Scope trigger connected to sync. Level check "S_3"
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10			
(PE) SET CHECK	1 or 2	1	2	2	1	1	1	1	2	1	VCP	PE	PE, VCP, 1.5V, 0V, 45 nsec
(PE) RELEASE CHECK	2	1	2	2	1	2	2	1	2	1	VCP	PE	VCP, 1.5V, 0V, PE, 10 nsec
(P2) SET CHECK	1 or 2	1	2	2	2	1	1	1	1	2	VCP	P2	VCP, P2, 1.5V, 0V, 35 nsec
(P2) RELEASE CHECK	1	1	2	2	2	2	2	1	1	2	VCP	P2	VCP, 1.5V, 0V, P2, 0 nsec
RESET CHECK	1 or 2	1	2	1	1	1	1	1	1	1 or 2	VCP	RESET	RESET, VCP
FREQ. CHECK	1 or 2	1 and 2	2	2	2	2	2	2	2	1 or 2	VCP	VCP	1000 nsec or 67.7 nsec

SWITCHING TIME AND SHIFT FREQUENCY WAVEFORMS



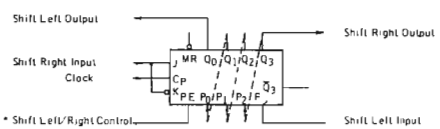




(PIN 12 or 11) V_{OUT} Frequency = ½ X V_{IN} Frequency

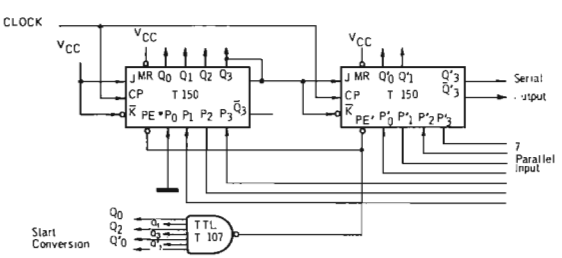
APPLICATIONS

A. 4-BIT LEFT/RIGHT SHIFT REGISTER



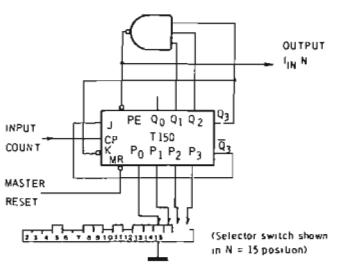
* To Shift Right-Input HIGH
To Shift Left-Input LOW

B. 7 - BIT PARALLEL - TO - SERIAL CONVERTER



* This circuit uses a marker bit to count the data bits shifted out so that a parallel load enable is generated to load the next parallel word for conversion at the correct time.

C. DIVIDE BY "N" COUNTER ("N" = 2 to 15)



One-of-ten decoder

EXTENDEND TEMPERATURE RANGE
-55°C to 125°C
STANDARD TEMPERATURE RANGE
0°C to 75°C

- INPUT DIODE CLAMPING
- TYPICAL INPUT/OUTPUT PROPAGATION DELAY 20 ns
- MULTI-FUNCTION CAPABILITY
- MUTUALLY EXCLUSIVE OUTPUTS
- DEMULTIPLEXING CAPABILITY
- TYPICAL POWER DISSIPATION OF 145 mW
- CERAMIC HERMETIC AND PLASTIC 16 PIN DUAL IN-LINE PACKAGE

The T 151 one-of-ten decoder is a circuit constructed on a single silicon chip by means of the planar epitaxial process. The T 151 is a multifunction decoder. Designed to accept four weighted inputs and provide ten mutually exclusive outputs, the circuit utilizes TTL logic for high speed and high fan-out capability. The unique logic of this device makes it very versatile in decoding and logic conversion applications.

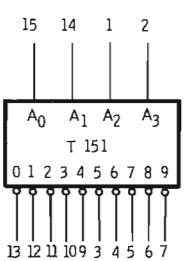
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage, Continuous	-0.5V to 7 V
Input Voltage	-0.5 V to 5.5 V
Output Voltage	-0.5 V to V_{CC}
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

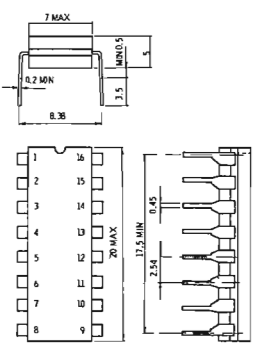
Extended	
Temperature Range	-55°C to 125°C
Supply Voltage	5 V ± 10%
Standard	
Temperature Range	0°C to 75°C
Supply Voltage	5 V ± 5%

LOGIC DIAGRAM AND PIN CONNECTION



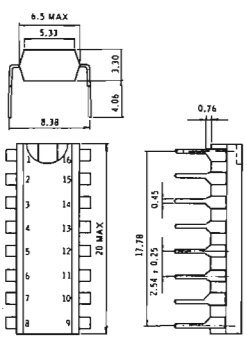
V_{CC} = PIN 16
GND = PIN 8

PHYSICAL DIMENSIONS
16-pin ceramic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
16 pin plastic DIP



NOTE: All dimensions in mm.

ORDERING NUMBERS

T 151 D1 (For Ceramic DIP and Standard Temperature Range)
T 151 D2 (For Ceramic DIP and Extended Temperature Range)
T 151 B1 (For Plastic DIP and Standard Temperature Range)

ELECTRICAL CHARACTERISTICS (0°C to 75°C, V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTIC	LIMITS						Unit	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC}=4.75V, I_{OH}= -0.6 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC}=4.75V, I_{OL}= 14.1 mA
										V_{CC}=5.25V, I_{OL}= 16 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC}=5.25V, V_F= 0.45 V
I_R	Input Leakage Current		60		15	60		60	µA	V_{CC}=5.25V, V_R= 4.5 V
I_{SC}	Output Short Circuit Current	-10	-70	-10		-70	-10	-70	mA	V_{CC}=5.25V, output grounded
I_{PD}	Power Dissipation Current		45			45		45	mA	V_{CC}= 5V, A_0, A_1, A_2, A_3 inputs grounded

ELECTRICAL CHARACTERISTICS (-55°C to 125°C, V_{CC} = 5V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						Unit	CONDITIONS AND COMMENTS
		-55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} =4.5V, I_{OH}= -0.6 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	V	V_{CC}=4.5V, I_{OL}= 12.4 mA
										V_{CC}=5.5V, I_{OL}= 16 mA
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1.1	-1.6		-1.6	mA	V_{CC}=5.5V, V_F = 0.4 V
I_R	Input Leakage Current		60		15	60		60	µA	V_{CC}=5.5V, V_R =4.5V
I_{SC}	Output Short Circuit Current	-10	-70	-10		-70	-10	-70	mA	V_{CC}=5.5V, output grounded
I_{PD}	Power Dissipation Current		45			45		45	mA	V_{CC}= 5V, A_0, A_1, A_2, A_3 inputs grounded

LOADING RULES (1 U.L. = 1 TTL Gate Input Unit Load)

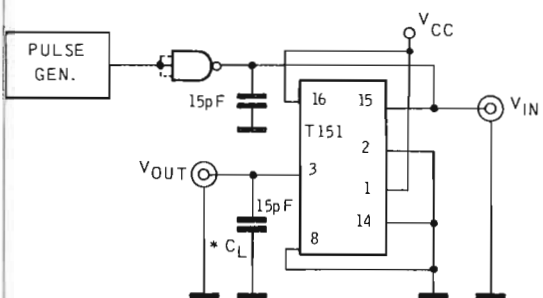
INPUTS : A_0, A_1, A_2, A_3 — LOADING FACTOR : 1 U.L.

OUTPUTS : 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 — DRIVE FACTOR : 10 U.L.

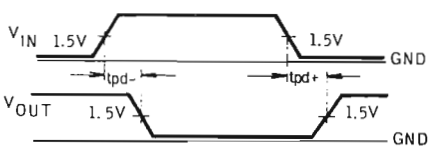
SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS AND COMMENTS
t_{pd+}	Turn-Off Delay	10	20	35	nsec	$V_{CC} = 5V$ $C_L = 15$ pF
t_{pd-}	Turn-On Delay	7	20	30	nsec	

TEST CIRCUIT



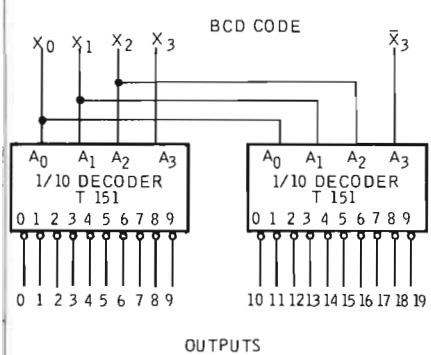
WAVEFORMS



* The capacitance shall be within ± 5% including jig, probe and wiring capacitance.

APPLICATIONS

A. DECODER FOR ANY BCD CODE

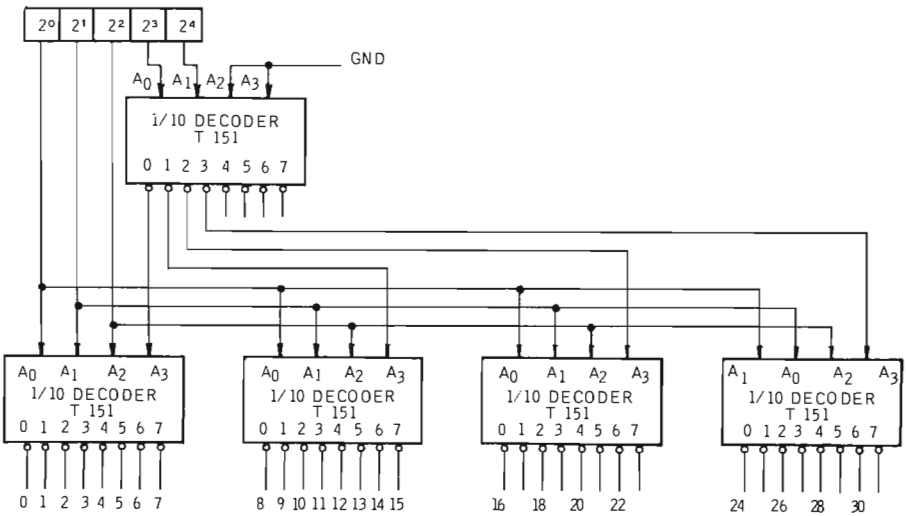


DECIMAL DIGIT	OUTPUT BCD CODE			
	8421	5421	Excess 3	4221
0	0.18	0.18	3	0.18
1	1.19	1.19	4	1.19
2	2	2	5	2
3	3	3	6	3
4	4	4	7	6
5	5	8.10	8.10	9.11
6	6	9.11	9.11	14
7	7	12	12	15
8	8.10	13	13	16
9	9.11	14	14	17

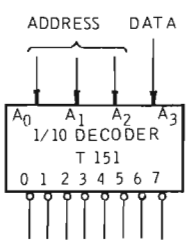
Decode any BCD code using two T 151 elements. Any 4 bit BCD code may be decoded by selecting outputs as shown in the table.

APPLICATIONS (contd)

B. ONE OF THIRTY-TWO DECODING



C. DIGITAL DEMULTIPLEXER



ADDRESS			OUTPUT LINE
A	B	C	
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

The single-line input data may be routed to any one of 8 outputs by addressing that output as shown. All non-addressed output remain high.

NOTE : Complements of output lines 0 and 1 are available on output lines 8 and 9 respectively.

EXTENDED TEMPERATURE RANGE,
-55°C to 125°C
STANDARD TEMPERATURE RANGE,
0°C to 75°C

- INPUT DIODE CLAMPING
- MULTI-FUNCTION CAPABILITY
- 8ns CARRY PROPAGATION DELAY
- COMPLEMENTARY INPUTS AND OUTPUTS
- TYPICAL POWER DISSIPATION OF 150 mW
- CERAMIC HERMETIC AND PLASTIC 16 PIN DUAL IN-LINE PACKAGE

Dual full adder

The T 152 dual full adder is a medium scale integrated circuit constructed on a single silicon chip using the planar epitaxial process. The T 152 consists of two independent, high-speed, binary full adders with complementary sum (S and $\overline{S}$) outputs. One adder features inverted carry ($\overline{C}_{OUT}$) output, while the second adder has complementary ($\overline{A}_2$ and $\overline{B}_2$) inputs and an inverted carry ($\overline{C}_{IN}$) input. By connecting the inverted carry output of the first adder to the inverted carry input of the second adder, the device performs the addition of two 2-bit binary numbers. Designed especially for multiple-bit, parallel-add/serial-carry applications, the circuit utilizes TTL logic for high-speed, high fan-out operation. The single inversion unique circuitry of the serial-carry outputs minimizes the necessity for complicated "look-ahead" and carry-cascading circuits.

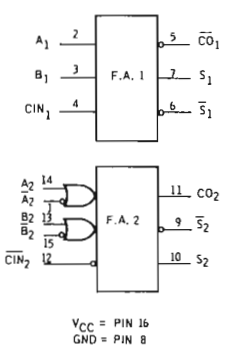
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage, Continuous	-0.5 V to 7 V
Input Voltage	-0.5 V to 5.5 V
Output Voltage	-0.5 V to V_{CC}
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

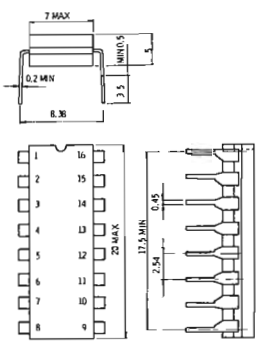
Extended	
Temperature Range	-55°C to 125°C
Supply Voltage	5 V ± 10%
Standard	
Temperature Range	0°C to 75°C
Supply Voltage	5 V ± 5 %

LOGIC DIAGRAM AND PIN CONNECTION



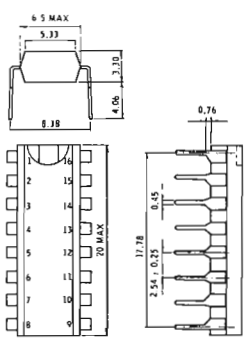
V_{CC} = PIN 16
GND = PIN 8

PHYSICAL DIMENSIONS
16 pin ceramic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
16 pin plastic DIP



NOTE: All dimensions in mm.

ORDERING NUMBER :

T 152 D1 (For Ceramic DIP and Standard Temperature Range)
T 152 D2 (For Ceramic DIP and Extended Temperature Range)
T 152 B1 (For Plastic DIP and Standard Temperature Range)

ELECTRICAL CHARACTERISTICS (0°C to 75°C, V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	Unit	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC}=4.75V I_{OH}=-0.6 mA $S_1, \overline{S}_2$ I_{OH}=-0.54mA $\overline{S}_1, S_2$ I_{OH}=-0.42mA $\overline{CO}_1, CO_2$
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC}=5.25V I_{OL}=16mA $S_1, \overline{S}_2$ I_{OL}=14.4mA $\overline{S}_1, S_2$ I_{OL}=11.2mA $\overline{CO}_1, CO_2$
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current A_2 and B_2 Inputs		-1.6		-1.1	-1.6		-1.6	mA	V_{CC}=5.25V V_F= 0.45V
	Other Inputs		-6.4		-4.4	-6.4		-6.4	mA	
I_R	Input Leakage Current A_2 and B_2 Inputs		60		15	60		60	µA	V_{CC}=5.25V V_R= 4.5V
	Other Inputs		240		60	240		240	µA	
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC}=5.75V output grounded
I_{PD}	Power Dissipation Current		55			55		55	mA	V_{CC}=5V A_2 and B_2 grounded

ELECTRICAL CHARACTERISTICS (-55°C to 125°C, V_{CC} = 5 V ± .10%)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	-55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	Unit	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC}=4.5V I_{OH}=-0.6mA $S_1, \overline{S}_2$ I_{OH}=-0.54mA $\overline{S}_1, S_2$ I_{OH}=-0.42mA $\overline{CO}_1, CO_2$
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC}=5.5V I_{OL}=16 mA $S_1, \overline{S}_2$ I_{OL}=14.4mA $\overline{S}_1, S_2$ I_{OL}=11.2mA $\overline{CO}_1, CO_2$
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current A_2 and B_2 Inputs		-1.6		-1.1	-1.6		-1.6	mA	V_{CC}=5.5V V_F=0.4V
	Other Inputs		-6.4		-4.4	-6.4		-6.4	mA	
I_R	Input Leakage Current A_2 and B_2 Inputs		60		15	60		60	µA	V_{CC}=5.5V V_R = 4.5V
	Other Inputs		240		60	240		240	µA	
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC}= 6V output grounded
I_{PD}	Power Dissipation Current		55			55		55	mA	V_{CC}= 5V A_2 and B_2 grounded

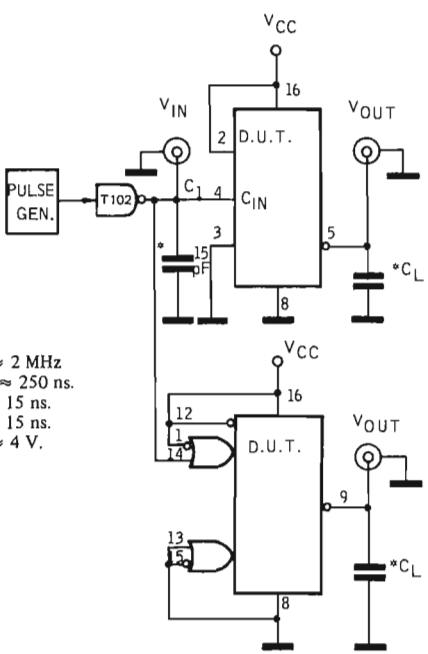
LOADING RULES (1 U.L. = 1 TTL gate input unit load)

INPUTS	A_1, B_1, C_{IN1}	LOADING FACTOR	:	4 U.L.
	$\bar{A}_2$, $\bar{B}_2$, $\bar{C}_{IN1}$			4 U.L.
	A_2, B_2,			1 U.L.
OUTPUTS	$\bar{C}_{01}$, C_{02}	DRIVE FACTOR	:	7 U.L.
	$\bar{S}_1$, S_2			9 U.L.
	S_1, $\bar{S}_2$			10 U.L.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

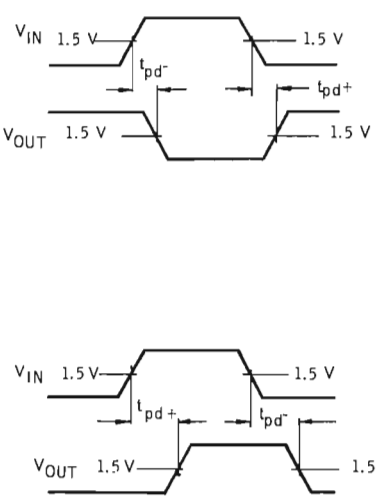
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.Ext.	Max.Std.	Unit	CONDITIONS AND COMMENTS
t_{pd^+}	C_{IN} to $\bar{C}_{OUT}$ and $\bar{C}_{IN}$ to C_{OUT}	2	8	13	15	nsec	V_{CC} = 5V C_L = 15 pF (see test circuit)
t_{pd^-}	C_{IN} to $\bar{C}_{OUT}$ and $\bar{C}_{IN}$ to C_{OUT}	2	8	13	15	nsec	
t_{pd^+}	A_2 to $\bar{S}_2$	8	25	40	45	nsec	
t_{pd^-}	A_2 to $\bar{S}_2$	8	20	35	40	nsec	

tpd TEST CIRCUIT



Frequency ≈ 2 MHz
Pulse Width ≈ 250 ns.
Rise Time < 15 ns.
Fall Time < 15 ns.
Amplitude ≈ 4 V.

WAVEFORMS



* The capacitance shall be within ± 5% including jig, probe and wiring capacitance.

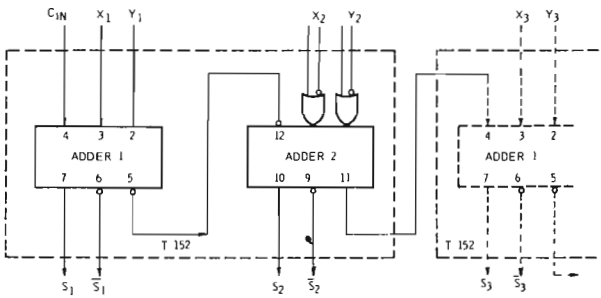
TRUTH TABLE

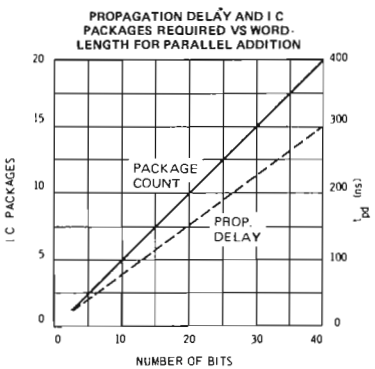
ADDER 1					
INPUTS			OUTPUTS		
C_{IN}	B	A	$\overline{C}_{OUT}$	$\overline{S}$	S
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

ADDER 2							
INPUTS					OUTPUTS		
$\overline{C}_{IN}$	B_2	A_2	$\overline{B}_2$	$\overline{A}_2$	C_{OUT}	S	$\overline{S}$
0	0	0	0	0	1	1	0
0	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	1	1	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	0	1
0	0	1	1	1	1	0	1
0	1	0	0	0	1	1	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	1	0
0	1	1	0	1	1	1	0
0	1	1	1	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	0	1	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	1	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	1
1	1	0	0	1	0	1	0
1	1	0	1	0	1	0	1
1	1	0	1	1	0	1	0
1	1	1	0	0	1	0	1
1	1	1	0	1	1	0	1
1	1	1	1	0	1	0	1
1	1	1	1	1	1	0	1

APPLICATIONS

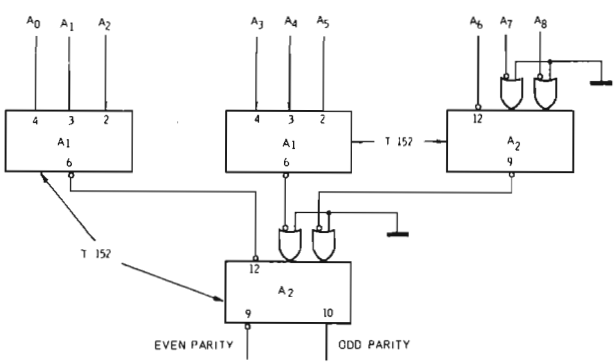
A. PARALLEL ADDITION - RIPPLE CARRY





The curve shows propagation delay of the ripple - carry adder shown in the above figure and also the low package count resulting from this-ripple-carry configuration.

B. PARITY - GENERATION OR CHECKING



The above configuration uses the T152 elements to generate parity for an 8 - bit byte or check parity over 9 - bits. Additional adder blocks can be used to generate or check parity over larger word lengths.

256-bit read only memory

STANDARD TEMPERATURE RANGE 0°C to 75°C

- COMPATIBLE WITH OTHER DTL OR TTL FAMILY PRODUCTS
- INPUT DIODE CLAMPING
- OPEN-COLLECTOR OUTPUTS PERMIT WIRED-OR CAPABILITY
- SINGLE TTL LOAD INPUTS
- ALL CERAMIC HERMETIC 16 PIN DUAL IN-LINE PACKAGE

ORDERING NUMBER

T154 D1XXXX, where XXXX are letters identifying the particular content.

The T 154 is a 256-bit bipolar transistor-transistor logic read only memory. The memory is organized as 32 words of 8 bits each. The words are selected through 5 address lines. The 8 outputs of the words are uncommitted collectors which may be wired-OR connected with the outputs of other ROM's. An Enable input is provided for additional decoding flexibility. A high Enable forces all outputs to be high. The contents of the memory are permanently programmed on customer request.

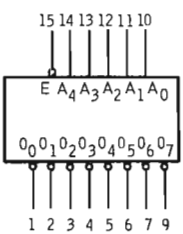
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

V_{CC} Pin Potential to Ground	- 0.5V to 8V
Input Voltage	- 0.5V to 5.5V
Current Into Output Terminal	100 mA
Output Voltages	- 0.5 to V_{CC} value
Storage Temperature Range	- 65°C to 150°C
Temperature (Ambient) Under Bias	- 55°C to 125°C

OPERATING CONDITIONS

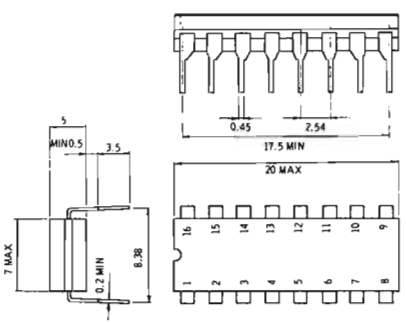
Temperature Range	0°C to 75°C
Supply Voltage	5V ± 5%

LOGIC DIAGRAM AND PIN CONNECTION



GND = 8
V_{CC} = 16

PHYSICAL DIMENSIONS
16-pin ceramic DIP



Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%)

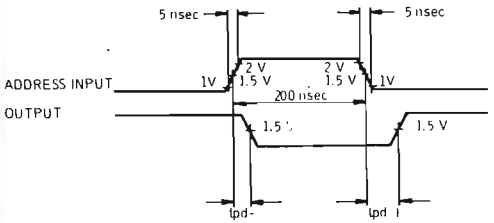
SYMBOL	CHARACTERISTICS	LIMITS			Unit	CONDITIONS AND COMMENTS
		Min.	Typ.	Max.		
V_{OL}	Output Low Voltage			0.45	V	V_{CC} = 4.75V I_{OL} = 10 mA Monitor appropriate output to perform this test.
V_{IL}	Input Low Voltage			0.85	V	V_{CC} = 5.25V Monitor appropriate output to perform this test.
V_{IH}	Input High Voltage	2			V	V_{CC} = 4.75V Monitor appropriate output to perform this test.
I_F	Input Load Current			- 1.6	mA	V_{CC} = 5.25V V_F = 0.45V
I_R	Input Leakage Current			100	µA	V_{CC} = 5.25V V_R = 4.5V
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 4.75V 5.25V on output.
I_{PD}	Power Dissipation Current		55	80	mA	V_{CC} = 5.25V Enable and Address inputs grounded.

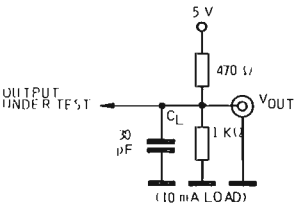
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	LIMITS			Unit	CONDITIONS AND COMMENTS
		Min.	Typ.	Max.		
t_{pd+}	Enable and Address to Output Delay		30	50	ns	10 mA load } Monitor appropriate outputs to perform these tests. (See fig. 1)
t_{pd-}	Enable and Address to Output Delay		30	50	ns	10 mA load

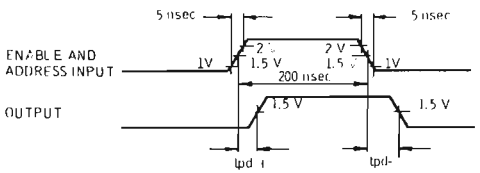
STANDARD TEMPERATURE RANGE

SWITCHING TIME TEST:OUTPUT LOAD AND WAVEFORMS (Fig. 1)





C_L includes probe and jig capacitance.



TRUTH TABLE

	WORD	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
INPUTS	ENABLE	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	ADDRESS 1	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
	ADDRESS 2	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
	ADDRESS 3	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
	ADDRESS 4	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	ADDRESS 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
OUTPUTS	OUTPUT 0_0																																
	OUTPUT 0_1																																
	OUTPUT 0_2																																
	OUTPUT 0_3																																
	OUTPUT 0_4																																
	OUTPUT 0_5																																
	OUTPUT 0_6																																
	OUTPUT 0_7																																

NOTES :

1) A high Enable forces all outputs to be high, irrespective of the selected word.
2) The output levels are not shown on the truth table since the customer specifies the output condition he desires at each of the eight outputs for each of the 32 words.
3) The output truth table has to be filled up with an X where a low level is required.
4) H = high level; L = low level.

HOW TO HAVE A CUSTOMIZED ROM

The SGS CAD facilities are used to customize the ROM. A large computer drives a photocomposition machine to make, from your content-punched cards, the test sequence, the truth table and the masks.
This unique system eliminates pattern conversion errors: upon request a computer generated truth table could be supplied for customer re-check purposes.

Punched card format

The punched cards suitable for SGS CAD are the 80 column type and one card per word is needed.

1st to 12th column - part number, alphanumeric. Each custom ROM is assigned its unique part number. First column shows the first character.

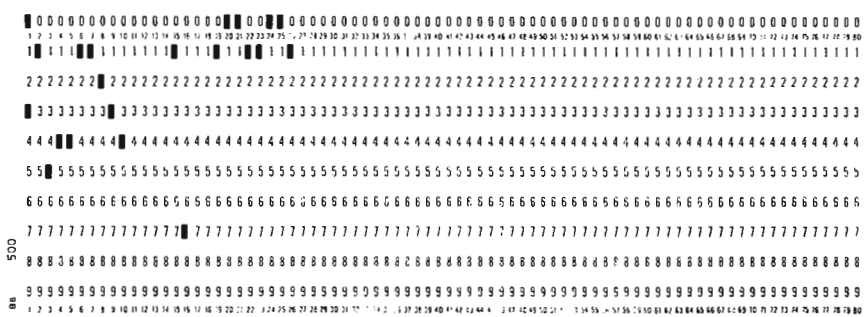
13th to 16th column - word number, numeric. First word is always called N° zero. Last column is the unit digit.

17th and 18th columns- blanks ♭.

19th to 26th column - word content expressed in one's and zero's. Column 19 corresponds to the output 0_0, the 20th to 0_1, etc.

EXAMPLE :

T154D1ABCD 17 10011001



8-input multiplexer

TTL family product

EXTENDED TEMPERATURE RANGE
-55°C ÷ 125°C
STANDARD TEMPERATURE RANGE
0°C ÷ 75°C

- COMPATIBLE WITH ALL OTHER DTL AND TTL FAMILY PRODUCTS
- INPUT DIODE CLAMPING
- TYPICAL DELAY-TIME 25 n SEC.
- TYPICAL POWER-DISSIPATION 135 mW
- MULTIFUNCTION CAPABILITY
- DATA INPUT ENABLE
- CERAMIC HERMETIC AND PLASTIC 16 PIN DUAL IN-LINE PACKAGE

The T 163 is a high speed eight input digital multiplexer circuit constructed on a single silicon chip using the planar epitaxial process. It provides, in one package, the ability to select one bit of data from up to eight sources. The T 163 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. The active pull-ups on the outputs provide high speed, high fan-out and the TTL circuitry makes the T 163 compatible with all other devices of the CCSL family.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage, Continuous	-0.5V to 7V
Input Voltage	-0.5V to 5.5V
Output Voltage	-0.5V to V_{CC}
Storage Temperature Range	-65°C to 150°C
Temperature (Ambient) Under Bias	-55°C to 125°C

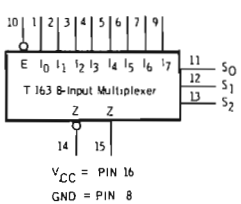
OPERATING CONDITIONS

Extended	
Temperature Range	-55°C to 125°C
Supply Voltage	5V ± 10%
Standard	
Temperature Range	0°C to 75°C
Supply Voltage	5V ± 5%

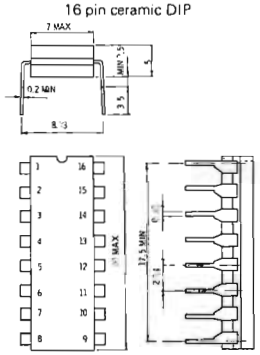
ORDERING NUMBERS

T 163 D1 (For Ceramic DIP and Standard Temperature Range)
T 163 D2 (For Ceramic DIP and Extended Temperature Range)
T 163 B1 (For Plastic DIP and Standard Temperature Range)

LOGIC DIAGRAM AND PIN CONNECTION

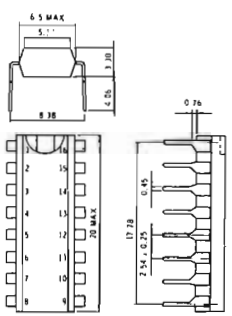


PHYSICAL DIMENSIONS
16 pin ceramic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
16 pin plastic DIP



NOTE: All dimensions in mm.

ELECTRICAL CHARACTERISTICS (0°C to 75°C, V_{CC} = 5V ± 5%)

Symbol	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC} = 4.75V I_{OH} = -0.6 mA
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 4.75V I_{OL}=14.1mA(Pin15) I_{OL}=12.95mA(Pin14)
										V_{CC} = 5.25V I_{OL}=16 mA (Pin15) I_{OL}=14.4mA(Pin14)
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed Input High Threshold for All Inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed Input Low Threshold for All Inputs
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.25V V_F = 0.45V
I_R	Input Leakage Current		60		15	60		60	µA	V_{CC} = 5.25V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-30	-100	-30		- 100	-30	-100	mA	V_{CC} = 5.25V Output Grounded
I_{PD}	Power Dissipation Current		43			43		43	mA	V_{CC} = 5V

ELECTRICAL CHARACTERISTICS (-55°C to 125°C, V_{CC} =5V ± 10%)

Symbol	CHARACTERISTICS	LIMITS -55°C Min.	-55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.5V I_{OH}=-0.6 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	V	V_{CC} = 4.5V I_{OL}=12.4mA (Pin 15) I_{OL}=11.2mA (Pin 14)
										V_{CC} = 5.5V I_{OL}=16 mA (Pin 15) I_{OL}=14.4mA (Pin 14)
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed Input High Threshold for All Inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed Input Low Threshold for All Inputs
I_F	Input Load Current		-1.6		-1.1	-1.6		-1.6	mA	V_{CC} = 5.5V V_F = 0.4V
I_R	Input Leakage Current		60		15	60		60	µA	V_{CC} = 5.5V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC} = 5.5V Output Grounded
I_{PD}	Power Dissipation Current		40			40		40	mA	V_{CC} = 5V

FUNCTIONAL DESCRIPTION

The T 163 is a logic implementation of a single pole - 8 position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs.
The logic function provided at the output is :

$$Z=E\cdot(I_0\cdot\bar{S}_0\cdot\bar{S}_1\cdot\bar{S}_2 + I_1\cdot S_0\cdot\bar{S}_1\cdot\bar{S}_2 + I_2\cdot\bar{S}_0\cdot S_1\cdot\bar{S}_2 + I_3\cdot S_0\cdot S_1\cdot\bar{S}_2 + I_4\cdot\bar{S}_0\cdot\bar{S}_1\cdot S_2 + I_5\cdot S_0\cdot\bar{S}_1\cdot S_2 + I_6\cdot\bar{S}_0\cdot S_1\cdot S_2 + I_7\cdot S_0\cdot S_1\cdot S_2).$$

The T 163 provides the ability, in one package, to select from eight sources of data or control information.
By proper manipulation of the inputs, the T 163 can provide any logic function of four variables and its negation.
Thus any number of random topic elements used to generate unusual truth tables can be replaced by one T 163.

E	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level L = Low voltage level
X = Level does not affect output

LOADING RULES

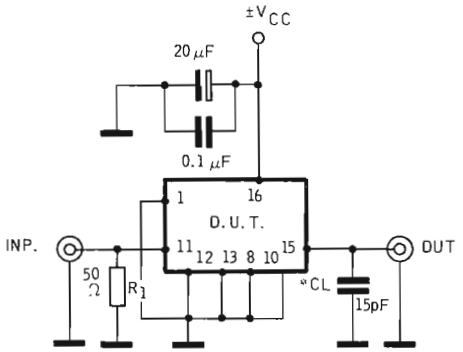
(1 U.L. = 1 TTL Gate Input Unit Load)

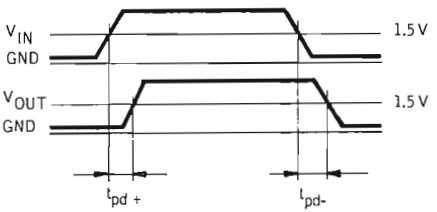
INPUTS : 1, 2, 3, 4, 5, 6, 7, 9, 10, 11, 12, 13 — LOADING FACTOR : 1 U.L.
OUTPUT: 15 — DRIVING FACTOR : 10 U.L.
OUTPUT: 14 — DRIVING FACTOR : 9 U.L.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	UNIT	CONDITIONS AND COMMENTS	
tpd+	Turn - Off Delay		23	34	nsec	V_{CC} = 5V	C_L = 15 pF
tpd−	Turn - On Delay		25	36	nsec	V_{CC} = 5V	C_L = 15 pF

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



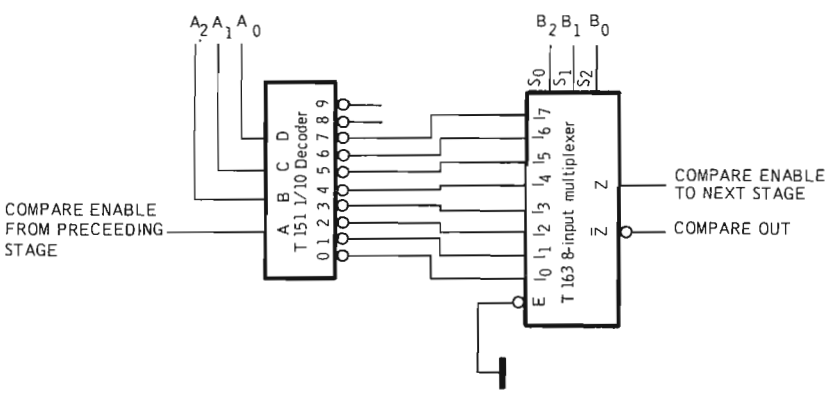


* The capacitance shall be within ± 5% including jig, probe and wiring capacitance.

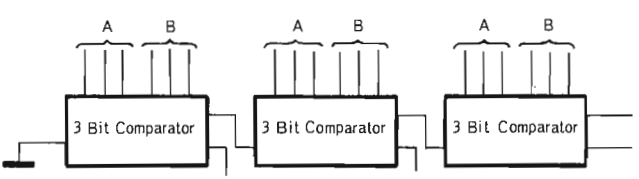
APPLICATIONS :

3 BIT COMPARATOR

Three bits of data to be compared are supplied to the address and select inputs of the T 151 and T 163 respectively.
If A_0, A_1, A_2 and B_0, B_1, B_2 compare, the mutually exclusive active low output of the T 151 1/10 decoder and the selected input of the T 163 multiplexer will be coincidental and COMPARE OUT will behigh. The COMPARE ENABLE must be low to permit compare operation.



INTERCONNECTION DIAGRAM FOR 9 BITS



Dual four-input multiplexer

EXTENDED TEMPERATURE RANGE
-55°C to 125°C
STANDARD TEMPERATURE RANGE
0°C to 75°C

- TYPICAL PROPAGATION DELAY 25 ns
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED COMPLEMENTARY OUTPUTS
- INPUT CLAMPING DIODES
- CERAMIC OR PLASTIC 16 PIN DUAL-IN-LINE PACKAGE
- COMPATIBLE WITH ALL DTL AND TTL FAMILY PRODUCTS

The T 164 is a monolithic, high speed dual four input digital multiplexer circuit. It consists of two multiplexing circuits with common input select logic, and each circuit contains four inputs and fully buffered complementary outputs. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding the T164 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output bus. The circuit utilizes TTL logic for high speed and high fanout capability, and is compatible with all DTL and TTL family products.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage, Continuous	-0.5V to 7V
Input Voltage	-0.5V to 5.5V
Output Voltage	-0.5V to V_{CC}
Storage Temperature Range (Ceramic DIP)	-65°C to 150°C
Storage Temperature Range (Plastic DIP)	-55°C to 125°C

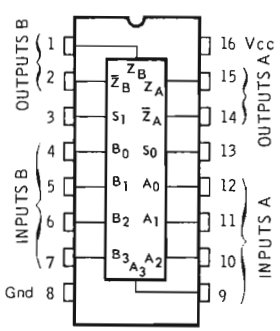
OPERATING CONDITIONS

Extended	
Temperature Range	-55°C to 125°C
Supply Voltage	5V ± 10%
Standard	
Temperature Range	0°C to 75°C
Supply Voltage	5V ± 5%

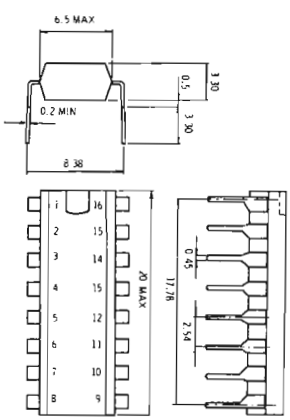
ORDERING NUMBERS

T 164 D1 (Ceramic DIP Standard Temperature Range)
T 164 D2 (Ceramic DIP Extended Temperature Range)
T 164 B1 (Plastic DIP Standard Temperature Range)

CONNECTION DIAGRAM
(Top view)

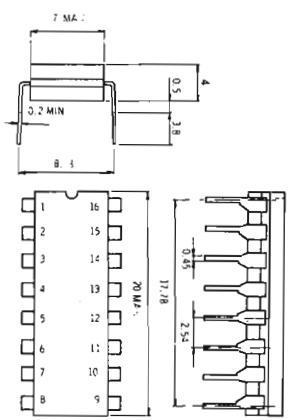


PHYSICAL DIMENSIONS
16 - pin plastic DIP



Note all dimensions in mm.

PHYSICAL DIMENSIONS
16 - pin ceramic DIP



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	2.4	3.0		V	V_{CC} = 4.75V I_{OH}= -1.2mA (Pins 1-15) V_{CC} = 4.75V I_{OH}=-1.08mA (Pins 2-14)
V_{OL}	Output Low Voltage		0.21	0.45	V	V_{CC} = 5.25V I_{OL}= 16mA (Pins 1-15) I_{OL}= 14.4mA (Pins 2-14) V_{CC} = 4.75V I_{OL}= 14.1mA (Pins 1-15) I_{OL}= 12.7mA (Pins 2-14)
V_{IH}	Input High Voltage	1.9			V	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage			0.85	V	Guaranteed input low threshold for all inputs.
I_F	Input Load Current		-1.1	-1.6	mA	V_{CC} = 5.25V V_F= 0.45V
I_R	Input Reverse Current		15	60	µA	V_{CC} = 5.25V V_R= 4.5
I_{PDH}	Power Dissipation Current		30	43	mA	V_{CC} = 5V All inputs high.

ELECTRICAL CHARACTERISTICS (T_A = -55°C to 125°C; V_{CC} = 5V ± 10%)

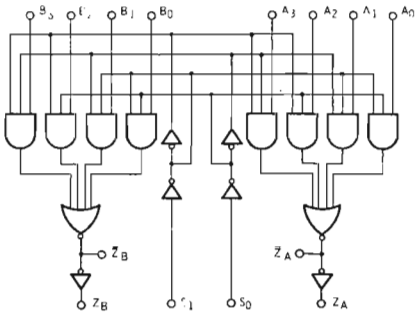
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	2.4	2.7		V	V_{CC} = 4.5V I_{OH}= -1.2mA (Pins 1-15) V_{CC} = 4.5V I_{OH}= -1.08mA (Pins 2-14)
V_{OL}	Output Low Voltage		0.21	0.4	V	V_{CC} = 5.5V I_{OL}= 16mA (Pins 1-15) I_{OL}= 14.4mA (Pins 2-14) V_{CC} = 4.5V I_{OL}= 12.4mA (Pins 1-15) I_{OL}= 11.2mA (Pins 2-14)
V_{IH}	Input High Voltage	2.0			V	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage			0.8	V	Guaranteed input low threshold for all inputs.
I_F	Input Load Current		-1.0	-1.6	mA	V_{CC} = 5.5V V_F= 0.4V
I_R	Input Reverse Current		10	60	µA	V_{CC} = 5.5V V_R= 4.5V
I_{PDH}	Power Dissipation Current		30	40	mA	V_{CC} = 5V All inputs high.

TRUTH TABLE

INPUTS						OUTPUTS	
S_0	S_1	A_0	A_1	A_2	A_3	Z_A	$\bar{Z}_A$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

INPUTS						OUTPUTS	
S_0	S_1	B_0	B_1	B_2	B_3	Z_B	$\bar{Z}_B$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

LOGIC DIAGRAM



L = LOW VOLTAGE LEVEL
H = HIGH VOLTAGE LEVEL
X = DON'T CARE

LOADING RULES (1 U.L. = 1 TTL GATE INPUT UNIT LOAD)

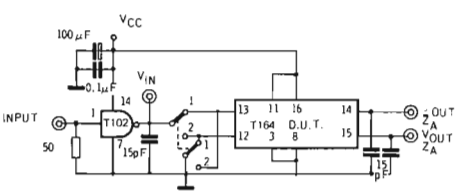
INPUTS : ALL
OUTPUTS: 1.15
OUTPUTS: 2.14

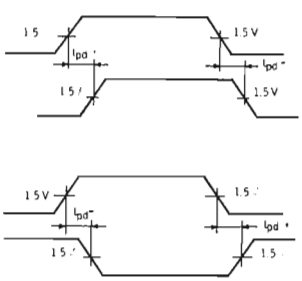
LOADING FACTOR : 1 U.L.
DRIVING FACTOR : 10 U.L.
DRIVING FACTOR : 9 U.L.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

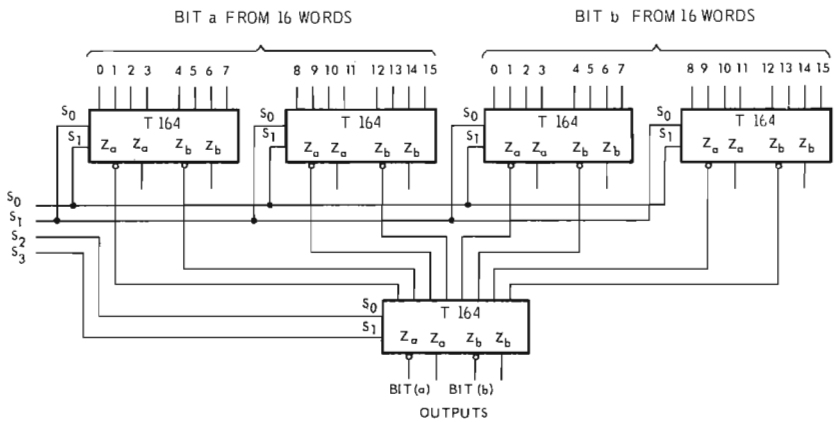
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS AND COMMENTS
t_{pd}	Turn-Off and On Delay S to Z		24	32	ns	See Test Circuit
t_{pd}	Turn-Off and On Delays S to $\bar{Z}$		18		ns	
t_{pd}	Turn-Off and On Delays A or B to $\bar{Z}$		14		ns	

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

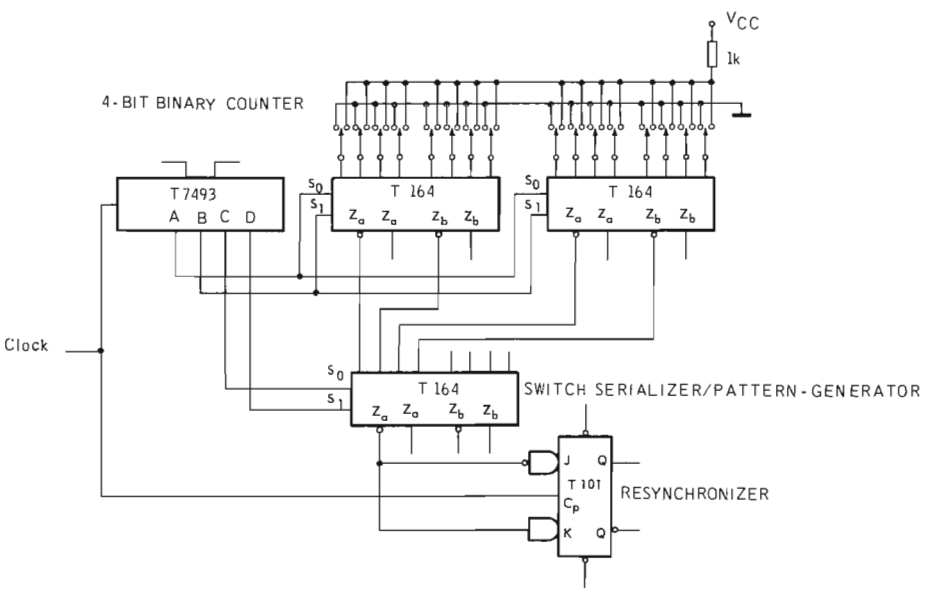




APPLICATIONS



A. Five T164's provide switching of data from sixteen two-bit words onto a two-bit output data bus. The selection of which bit to be transferred is made by the address inputs S_0, S_1, S_2 and S_3.



B. Sixteen-bit pattern generator

64-bit random access memory

STANDARD TEMPERATURE RANGE
0°C to 75°C

- FAST ACCESS TIME: 60nsec
- LOW POWER DISSIPATION: 6mW/BIT
- DTL AND TTL COMPATIBLE
- FULLY DECODED: ON CHIP ADDRESS, DECODE AND BUFFER
- CERAMIC 16-PIN DUAL IN-LINE PACKAGE
- OUTPUT OPEN COLLECTORS ALLOW WIRED-OR CAPABILITY FOR WORD EXPANSION
- SIMPLE MEMORY EXPANSION: CHIP SELECT INPUT LEAD
- MINIMUM LINE REFLECTION: LOW VOLTAGE INPUT CLAMP DIODES

The T 165 is a 64-bit random access memory. Its high speed makes it ideal in scratch pad applications. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than with a gold diffusion process. The T 165 is packaged in a hermetically sealed 16-pin dual in-line package, and its performance is specified over a temperature range from 0° to 85°C. The memory is organized as a 16-word by 4-bit array. The storage flip-flops are addressed through an on chip 1 out of 16 binary decoder using four input address leads. A separate Chip Select lead allows easy selection of an individual package when outputs are OR-tied. In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

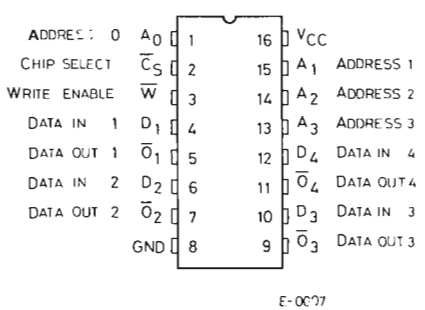
Supply Voltage (V_{CC}) Continuous	-0.5V to 7V
Input Voltage	5.25V
Storage Temperature Range	-65°C to 150°C
Temperature (Case) Under Bias	-55°C to 125°C

OPERATING CONDITIONS

Temperature Range	0°C to 75°C
Supply Voltage	5V ±5%

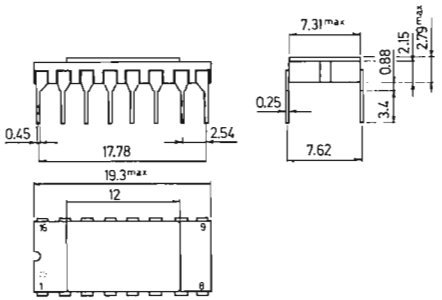
ORDERING NUMBER
T165 D1

CONNECTION DIAGRAM
(top view)



E-0007

PHYSICAL DIMENSIONS
16 - lead ceramic DIP



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS (0°C to 85°C, V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS
V_{OL}	Output Low Voltage			0.45	V	V_{CC} = 4.75V $V_W = V_{IL}$ $V_S = V_D$ = 2.5V I_{OL} = 15mA V_{CC} = 4.75V $V_S = V_W$=GND $V_D = V_{IH}$ I_{OL} = 15mA
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 5.25V V_{CEX} = 5.25V V_S = 2.5V $V_W = V_{IH}$ V_D = GND V_{CC} = 5.25V V_{CEX} = 5.25V $V_S = V_W$ = GND $V_D = V_{IL}$
V_{IH}	Input High Voltage	2			V	Guaranteed high threshold voltage
V_{IL}	Input Low Voltage			0.85	V	Guaranteed low threshold voltage
I_{FD}	Input Load Current Data			-1.6	mA	V_{CC} = 5.25V V_{IN} = 0.45V V_W = GND
I_F	Input Load Current A-W-C_S			-1.6	mA	V_{CC} = 5.25V V_{IN} = 0.45V
I_{RD}	Input Reverse Current Data			40	µA	V_{CC} = 5.25V V_{IN} = 5.25V V_W = 2.5V
I_R	Input Reverse Current A-W-C_S			40	µA	V_{CC} = 5.25V V_{IN} = 5.25V
V_{FC}	Input Clamp Voltage			-1	V	V_{CC} = 4.75V I_{IN} = -5mA
C_{IN}	Input Capacitance (All Pins)		6		pF	V_{IN} = 2V
C_{OUT}	Output Capacitance		8		pF	V_{OUT} = 2V
I_{PD}	Power Dissipation Current			110	mA	V_{CC} = 5.25V $V_A = V_S = V_D$=GND

SWITCHING CHARACTERISTICS (T_A = 0°C to 85°C, V_{CC} = 5V)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS
$T_{A(CS)}$	Read Access Time From Chip Select			60	ns	Figure 3
$T_{R(CS)}$	Recovery Time From Chip Select			60	ns	Figure 3
$T_{A(A)}$	Read Access Time From Address			60	ns	Figure 4
$T_{R(A)}$	Recovery Time From Address			60	ns	Figure 4
T_{WP}	Write Pulse Width	40			ns	Figure 2
T_{WR}	Write Recovery Time			50	ns	Figure 2
T_{DO}	Data To Output Delay			25	ns	V_W = GND Figure 5

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

Condition of test :

Input pulse amplitude 2.5V

Input pulse rise and fall time must be 5nsec between 1V and 2V

Speed measurements are made at 1.5V levels

FIG. 1

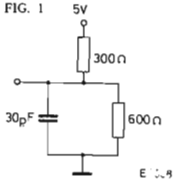
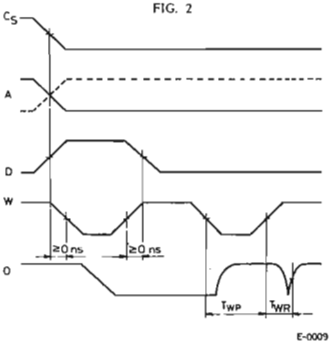


FIG. 2

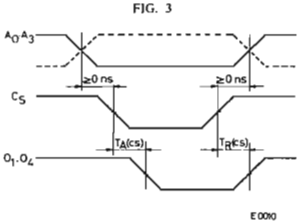


OPERATION

READ: The memory is addressed through A_0-A_3 which select one of the 16 words. The chip is enabled by placing chip select (C_S) to logic "0". If the write enable (W) is at a logic "1" the four stored bits are read out of 0_1-0_4 in parallel.

WRITE: The memory is addressed through A_0-A_3 which select one of the 16 words. The chip is enabled by placing C_S to logic "0". If the W is at a logic "0", the data on terminals D_1-D_4 is written into the addressed word in parallel and in complementary form. When W returns to logic "1", the information that was written in is now read out. However, each bit readout is the complement of what was written.

FIG. 3



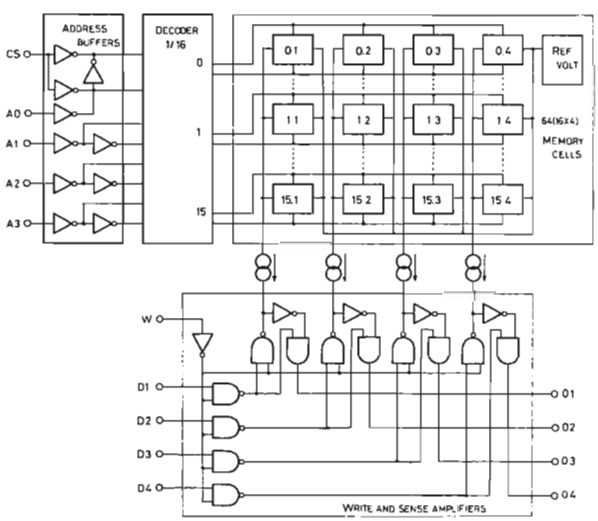


FIG. 6

FIG. 4

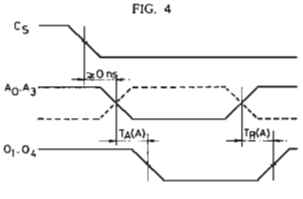
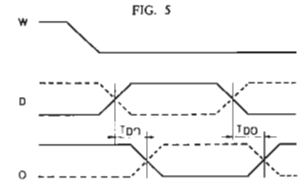
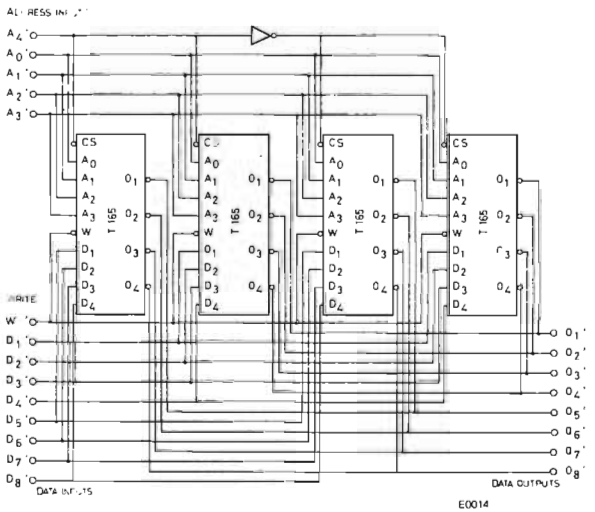


FIG. 5



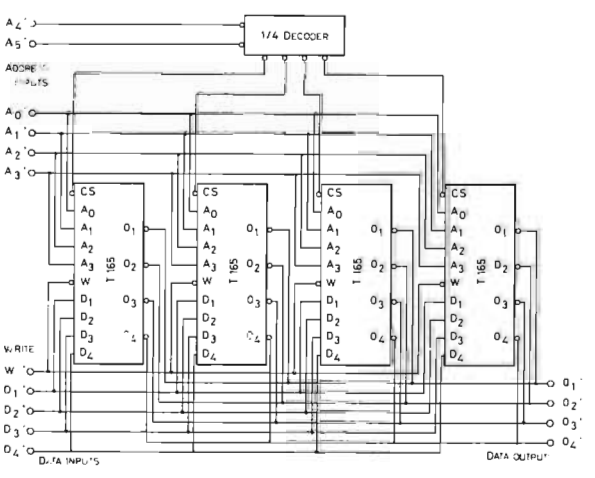
32 WORD x 8 BIT MEMORY

Two T 165 devices are used to increase the number of bits per word to 8. This is accomplished by connecting the Chip Select and Address inputs in parallel.To increase the number of words to 32, two of such parallel combinations are used.



64 WORD x 4 BIT MEMORY

The 64 word memory is made up of 4 T 165 memory devices. Word expansion is made possible by utilizing the Chip Select input as an additional address line. A 1 out of 4 decoder is used to drive the Chip Select input, and the outputs of each T 165 are OR-tied.



TTL INTEGRATED CIRCUIT

9 - BIT PARITY GENERATOR AND CHECKER

- BOTH EVEN AND ODD OUTPUT AVAILABLE
- HIGH VERSATILITY PROVIDED
- INPUT CLAMPING DIODES
- 14-PIN CERAMIC OR PLASTIC DUAL IN-LINE PACKAGE
- COMPATIBLE WITH ALL DTL AND TTL FAMILY PRODUCTS

The T 167, 9-input parity generator/parity checker, is a versatile MSI device commonly used to detect errors in data transmission or data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the T 167 (a logic 1 on the INHIBIT input forces both outputs to a logic 0).

When used as a parity generator, the T 167 supplies a parity bit which is transmitted together with the data word.

At the receiving end, the T 167 acts as a parity checker and indicates that data has been received correctly or that an error has been detected. Available in standard temperature range (0 to 75 °C), it comes in plastic and ceramic dual in-line package similar to Jedec TO-116.

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage, continuous	-0.5 to 7	V
V_i	Input voltage	-0.5 to 5.5	V
V_o	Output voltage	-0.5 to 5.5	V
T_{op}	Operating temperature	0 to 75	°C
T_{stg}	Storage temperature		
	for ceramic package	- 65 to 150	°C
	for plastic package	- 55 to 125	°C

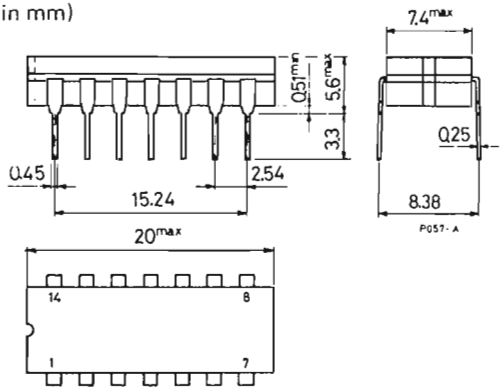
ORDERING NUMBERS

T 167 D1 (for ceramic dual in-line package and standard temperature range)
T 167 B1 (for plastic dual in-line package and standard temperature range)

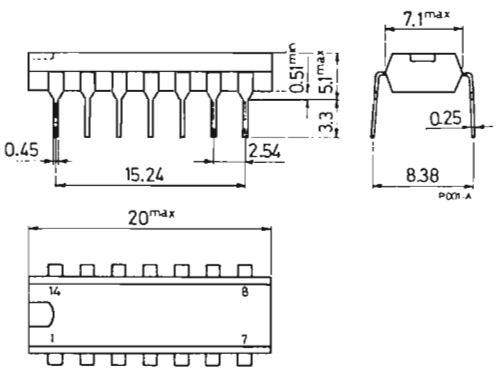
T 167

MECHANICAL DATA (Dimensions in mm)

Ceramic dual in-line package
(similar to TO-116)

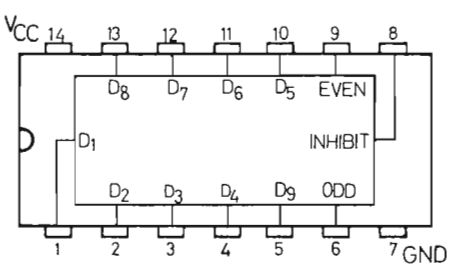


Plastic dual in-line package
(similar to TO-116)

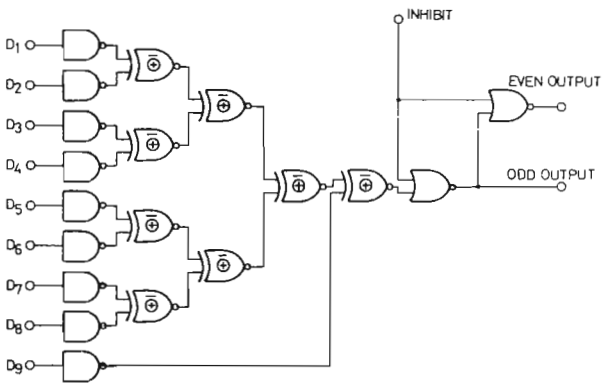


CONNECTION DIAGRAM

(top view)



FUNCTIONAL LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	
D_9	INHIBIT	Σ of 1's at D_1 thru D_8	EVEN	ODD
X	1	X	0	0
1	0	EVEN	0	1
1	0	ODD	1	0
0	0	EVEN	1	0
0	0	ODD	0	1

X : any level present at those inputs does not affect the output.

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
T_{op}	Operating temperature	0 to 75	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{IH}	Input high voltage		2			V	1
V_{IL}	Input low voltage				0.8	V	1
V_{OH}	Output high voltage	EVEN $V_{CC} = 4.75V$ $V_i = 0.8V$ $I_{OH} = -800\ \mu A$ $V_{INHIBIT} = 0.8V$ ODD $V_{CC} = 4.75V$ $V_i = 2V$ $I_{OH} = -800\ \mu A$ $V_{INHIBIT} = 0.8V$	2.6 2.6			V V	1
V_{OL}	Output low voltage	EVEN $V_{CC} = 4.75V$ $V_i = 2V$ $I_{OL} = 16\ mA$ $V_{INHIBIT} = 0.8V$ ODD $V_{CC} = 4.75V$ $V_i = 0.8V$ $I_{OL} = 16\ mA$ $V_{INHIBIT} = 0.8V$			0.4 0.4	V V	1
I_{IL}	Input low current at data inputs	$V_{CC} = 5.25V$ $V_i = 0.4V$			-1.6	mA	2
I_{IH}	Input high current at data inputs	$V_{CC} = 5.25V$ $V_i = 5.5V$ $V_{CC} = 5.25V$ $V_i = 2.4V$			1 40	mA µA	2
I_{IL}	Input low current at inhibit input	$V_{CC} = 5.25V$ $V_i = 0.4V$			-3.2	mA	2
I_{IH}	Input high current at inhibit input	$V_{CC} = 5.25V$ $V_i = 5.5V$ $V_{CC} = 5.25V$ $V_i = 2.4V$			1 80	mA µA	2
I_{SC}*	Short-circuit output current	$V_{CC} = 5.25V$ $V_{INHIBIT} = 0.8V$	-20		-70	mA	3
I_{CC}	Power supply current	$V_{CC} = 5.25V$			70	mA	3

* Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C, N = 10)

Parameter		Test Conditions **		Min.	Typ.	Max.	Unit
		from input	to output				
t_{pd1}	Propagation delay time to logical 1 level						
		Data 1-8	Even		38	55	ns
		Data 1-8	Odd		32	45	ns
		Data 9	Even		23	40	ns
		Data 9	Odd		20	35	ns
		Inhibit	Even or Odd		10	18	ns
t_{pd0}	Propagation delay time to logical 0 level						
		Data 1-8	Even		35	50	ns
		Data 1-8	Odd		30	45	ns
		Data 9	Even		20	35	ns
		Data 9	Odd		15	30	ns
		Inhibit	Even or Odd		8	15	ns

** See switching times test circuit, waveforms and truth table.

DC TEST CIRCUITS (arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{IH}, V_{IL}, V_{OH}, V_{OL}

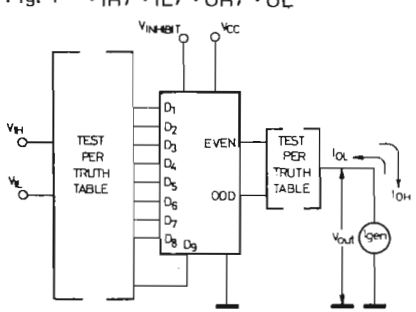
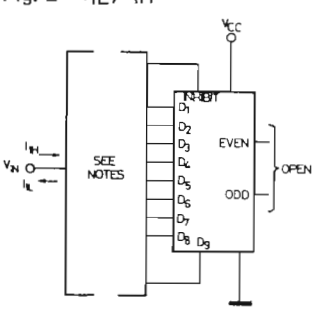


Fig. 2 - I_{IL}, I_{IH}

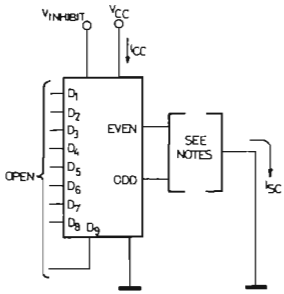


Each input is tested separately.

DC TEST CIRCUITS (continued)

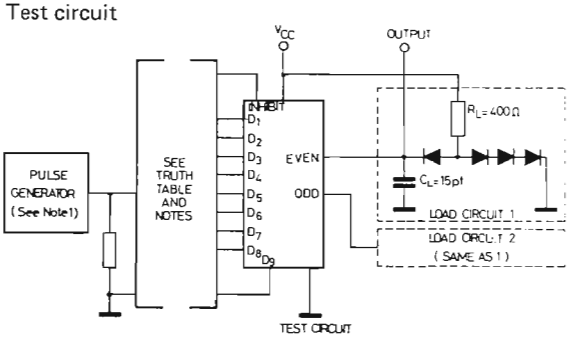
When testing I_{SC} each output is tested separately in accordance with the truth table. When testing I_{CC} both outputs are open.

Fig. 3 - I_{SC}, I_{CC}



SWITCHING TIMES

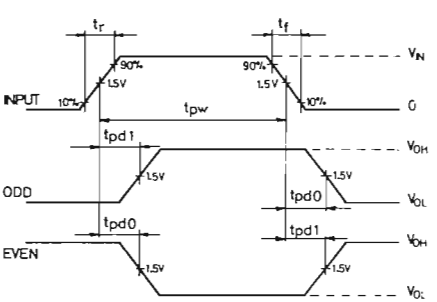
Test circuit



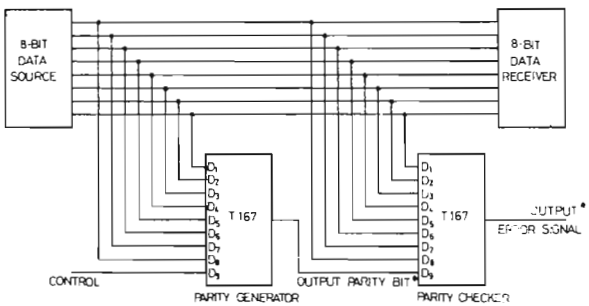
NOTES :

1. The pulse generator has the following characteristics : $V_i = 3V$, $t_r = t_f = 10$ ns, $t_{pw} = 500$ ns, PRR = 1 MHz and $Z_{out} \approx 50\Omega$.
2. C_L includes probe and jig capacitance.
3. All diodes are 1N3064.

Waveforms



TYPICAL APPLICATION



* Output can be conditioned for odd or even parity. An "even parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an even number.
An "odd parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an odd number.

TTL INTEGRATED CIRCUIT

T 168

QUAD 2 - INPUT MULTIPLEXER

- FULLY BUFFERED OUTPUTS
- ON-CHIP SELECT LOGIC DECODING
- MULTIFUNTION CAPABILITY
- INPUT CLAMPING DIODES
- TTL-DTL COMPATIBLE

The T 168 is a quad multiplexer of monolithic construction. Each multiplexer has common enable, select logic, two inputs and a single output. The device has an active level low enable input ($\overline{E}$), an output are active level high. This device is available in a 16-lead dual in-line plastic and ceramic package for a standard temperature range (0 to 75°C).

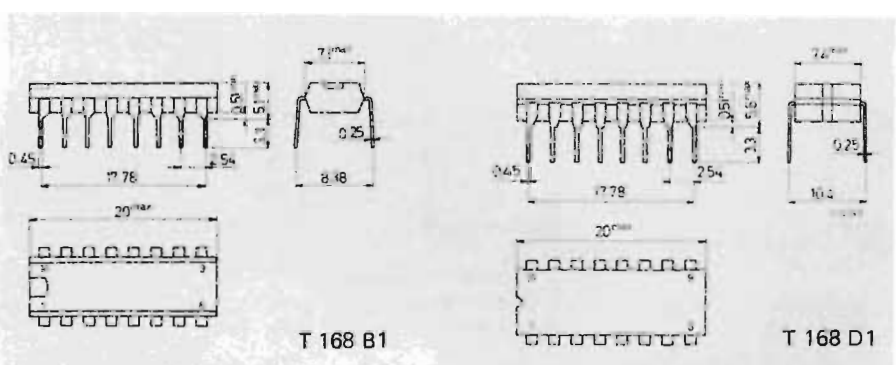
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage		7	V
V_i	Input voltage		5.5	V
T_{stg}	Storage temperature :	for plastic package	-55 to 125	°C
		for ceramic package	-65 to 150	°C
T_{op}	Operating temperature		0 to 75	°C

ORDERING NUMBER : T 168 B1 for dual in-line plastic package
T 168 D1 for dual in-line ceramic package

MECHANICAL DATA

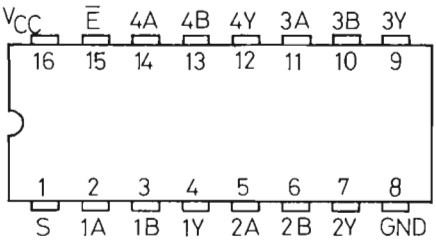
Dimensions in mm



T 168

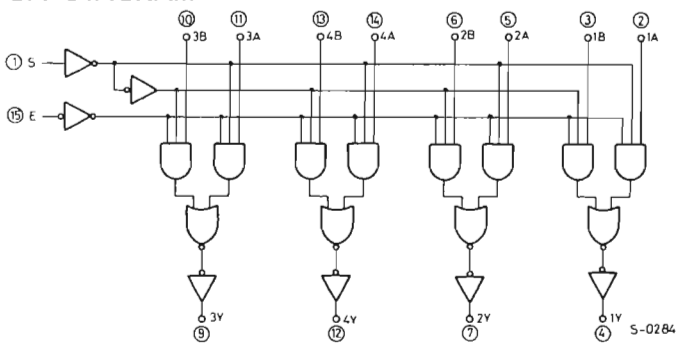
CONNECTION DIAGRAM

(top view)



S-0283

FUNCTIONAL LOGIC DIAGRAM



S-0284

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	B	A	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level.
L = LOW Voltage Level.
X = Either HIGH or LOW Logic Level.

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
N	Normalized fan-out (each output)	max 10	–
T_{op}	Operating temperature	0 to 75	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.*	Max.	Unit
V_{IH}	Input high voltage		2			V
V_{IL}	Input low voltage				0.8	V
V_C	Input clamp diode voltage	V_{CC}= 4.75V I_i= -12mA			-1.5	V
V_{OH}	Output high voltage	V_{CC}= 4.75V V_{IH}= 2V V_{IL}= 0.8V I_{OH}= -800μA	2.4	3.6		V
V_{OL}	Output low voltage	V_{CC}= 4.75V V_{IH}= 2V V_{IL}= 0.8V I_{OL}= 16mA			0.4	V
I_{IH}	Input high current	V_{CC}= 5.25V V_i= 2.4V V_{CC}= 5.25V V_i= 5V			40 1	μA mA
I_{IL}	Input low current	V_{CC}= 5.25V V_i= 0.4V		-0.96	-1.6	mA
I_{SC}**	Short-circuit output current	V_{CC}= 5.25V	-30		-100	mA
I_{CC}***	Supply current	V_{CC}= 5.25V		30	48	mA

* All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

** Not more than one output should be shorted at a time

*** It is measured with 4.5V applied to all inputs and all outputs open.

T 168

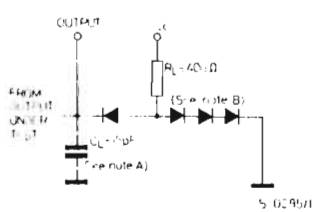
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C, N = 10)

Parameter		Test conditions*		Min.	Typ.	Max.	Unit
		From	To				
t_{pd1}	Propagation delay time to logical 1 level	Data	Output		11	22	ns
		Enable	Output		13	24	ns
		Select	Output		17	30	ns
t_{pd0}	Propagation delay time to logical 0 level	Data	Output		10	18	ns
		Enable	Output		19	26	ns
		Select	Output		20	31	ns

* See switching times load circuit and waveforms.

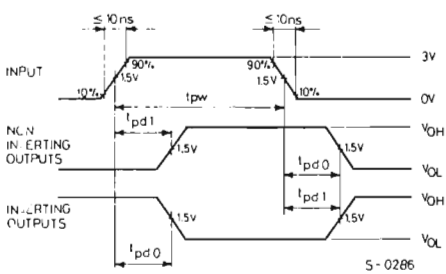
SWITCHING TIMES

Load circuit



NOTE: A. C_L includes probe and jig capacitance.
B. All diodes are 1N 3064.

Waveforms



NOTE: The input waveform is supplied by a generator with the following characteristics: PRR = 1 MHz, Z_o = 50Ω, t_{pw} = 100 ns.

TTL INTEGRATED CIRCUIT

T172

QUAD LINE RECEIVER

- INPUT CLAMP DIODES
- ACTIVE OUTPUT PULL-UP
- TYP. POWER DISSIPATION 150 mW
- 14-PIN DUAL IN-LINE PLASTIC PACKAGE

The T 172 is a quad two-input line receiver, constructed on a single silicon chip using the planar epitaxial process. Compatible with other TTL and DTL family products, it combines high noise immunity with high logic speed. The T 172, available in standard temperature range (0 to 75°C), comes in a dual in-line plastic package similar to Jedec TO-116.

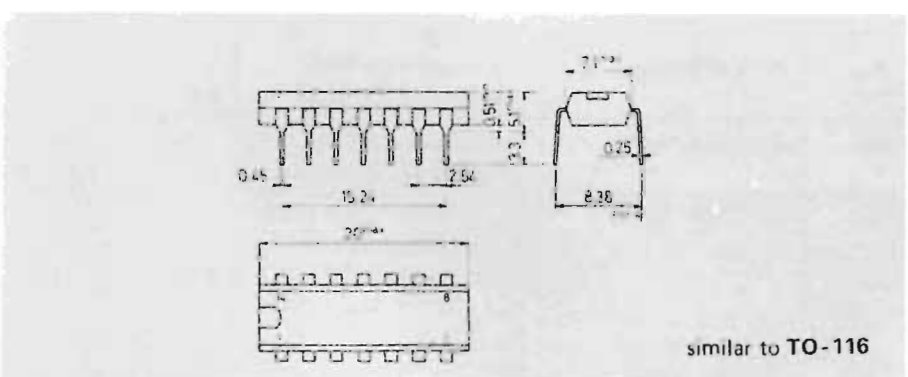
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage, continuous	-0.5 to 7	V
V_i	Input voltage	-0.5 to 5.5	V
V_o	Output voltage	-0.5 to 5.5	V
T_{op}	Operating temperature	0 to 75	°C
T_{stg}	Storage temperature	- 55 to 125	°C

ORDERING NUMBER : T 172 B1

MECHANICAL DATA

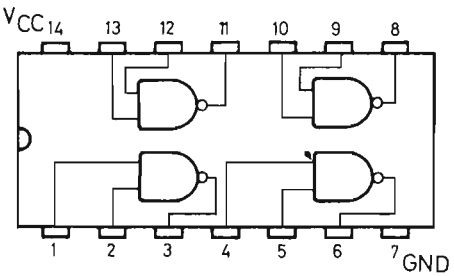
Dimensions in mm



similar to **TO-116**

T172

CONNECTION DIAGRAM (top view)



RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
T_{op}	Operating temperature	0 to 75	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	Guaranteed input high threshold for all inputs	2.6			V
V_{IL}	Input low voltage	Guaranteed input low threshold for all inputs			1.5	V
V_{OH}	Output high voltage	V_{CC} = 4.75V I_{OH} = -500µA V_{IL} = 1.5V Other input to V_{CC}	2.6			V
		V_{CC} = 4.75V I_{OH} = -500µA V_{IL} = 1.1V Other input to V_{CC}	2.8			V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Output low voltage	V_{CC} = 4.75V I_{OL} =20 mA V_{IH} = 2.6V			0.4	V
I_{IH}	Input high current	V_{CC} = 5.25V V_{IH} = 2.6V V_{CC} = 5.25V V_{IH} = 5.5V			50 1	µA mA
I_{IL}	Input low current	V_{CC} = 5.25V V_{IL} = 0.4V			-2.0	mA
I_{SC}*	Short-circuit output current	V_{CC} = 5.25V Output and inputs grounded	-40		-100	mA
I_{CCH}	High level power supply current	V_{CC} = 5.25V Inputs high			50	mA
I_{CCL}	Low level power supply current	V_{CC} = 5.25V Inputs low			20	mA
V_C	Input clamp diode voltage	V_{CC} = 4.75V I_i = -12mA			-1.5	V

* Only one gate shorted at a time

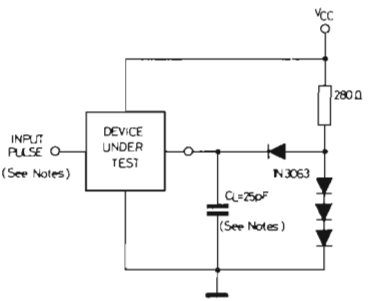
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
t_{pd1}	Propagation delay time to logical "1"	See switching time test circuit and waveforms			12	ns
t_{pd0}	Propagation delay time to logical "0"				12	ns

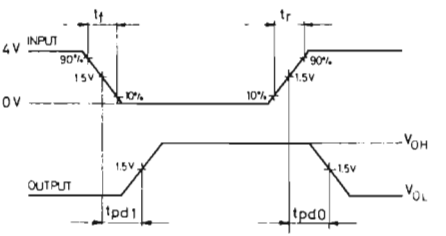
T172

SWITCHING TIMES

Test circuit



Waveforms



Notes :

- The input pulse has the following characteristics : P.R.R. 1MHz, duty cycle 50%, $t_f = t_r = 7$ ns
- C_L includes probe and jig capacitance.

TTL INTEGRATED CIRCUIT

T 173

QUAD BISTABLE LATCH

- INPUT CLAMP DIODES
- ACTIVE OUTPUT PULL-UP
- FAST LATCHING FUNCTION
- TYPICAL POWER DISSIPATION OF 300 mW
- 16-PIN DUAL IN-LINE PLASTIC PACKAGE

The T 173 is a quad D type flip-flop, constructed on a single silicon chip using the planar epitaxial process. It has common clock line, common strobe capability by means of a logical high level and, except the first stage, complementary output. The T 173 high speed makes this device ideally suited for use as temporary storage for binary information between processing units and indicator units. Available in standard temperature range (0 to 75 °C), it comes in 16-lead dual in-line plastic package.

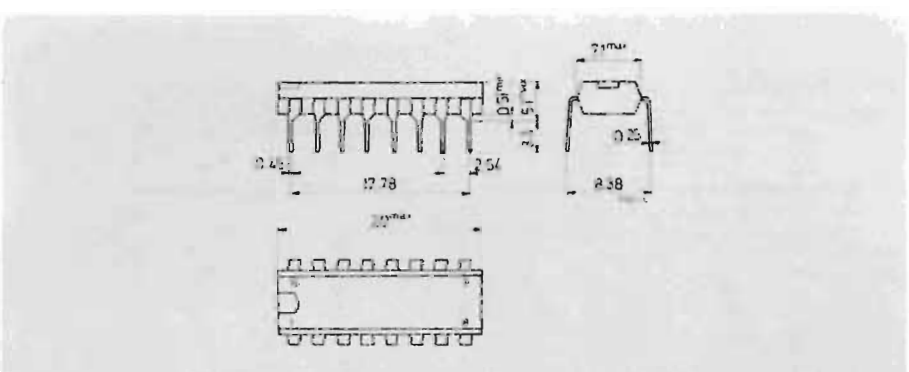
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
T_{op}	Operating temperature	0 to 75	°C
T_{stg}	Storage temperature	-55 to 125	°C

ORDERING NUMBER : T 173 B1

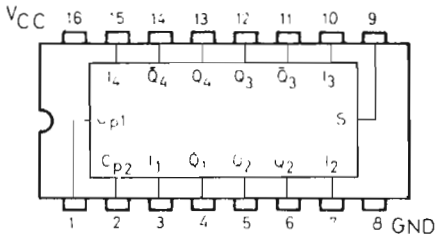
MECHANICAL DATA

Dimensions in mm

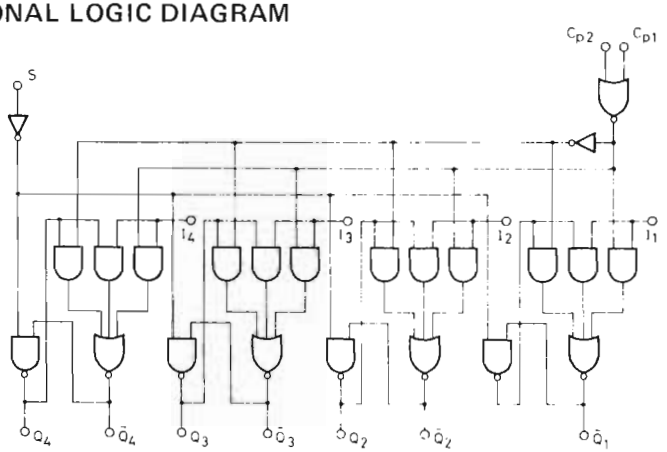


T 173

CONNECTION DIAGRAM (top view)



FUNCTIONAL LOGIC DIAGRAM



TRUTH TABLE

C_{p1}	C_{p2}	I	S	Q_{tn-1}
1	X	X	0	Q_{tn}
X	1	X	0	Q_{tn}
0	0	1	0	1
0	0	0	0	0
X	X	1	1	1

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
N	Normalized fan-out from each output	max 10	–
T_{op}	Operating temperature	0 to 75	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	Guaranteed input high threshold for all inputs	2			V
V_{IL}	Input low voltage	Guaranteed input low threshold for all inputs			0.8	V
V_{OH}	Output high voltage	V_{CC} = 4.75V I_{OH} = -500 µA V_i = 0.8V V_{CC} = 4.75V I_{OH} = -500 µA V_i = 0.4V	2.4 2.8			V V
V_{OL}	Output low voltage	V_{CC} = 4.75V I_{OL} = 20 mA V_i = 0.8V			0.4	V
I_{IH}	Input high current (clock strobe inputs)	V_{CC} = 5.25V V_i = 2.4V V_{CC} = 5.25V V_i = 5.5V			50 1	µA mA
I_{IH1}	Input high current (data input)	V_{CC} = 5.25V V_i = 2.4V V_{CC} = 5.25V V_i = 5.5V			100 1	µA mA
I_{SC}	Short-circuit output current ($\overline{Q}$)	V_{CC} = 5.25V input and output grounded	-40		-100	mA
I_{SC1}	Short-circuit output current (Q)	V_{CC} = 5.25V C_p = 4.5V output grounded	-40		-100	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CCL}	Supply current, low level output	V_{CC}= 5.25V I-C_p= Gnd S = 4.5V			72	mA
I_{CCH}	Supply current, high level output	V_{CC}= 5.25V I-S-C_p= 4.5V V_{CC}= 5.25V I-S-C_p= Gnd			88 88	mA mA

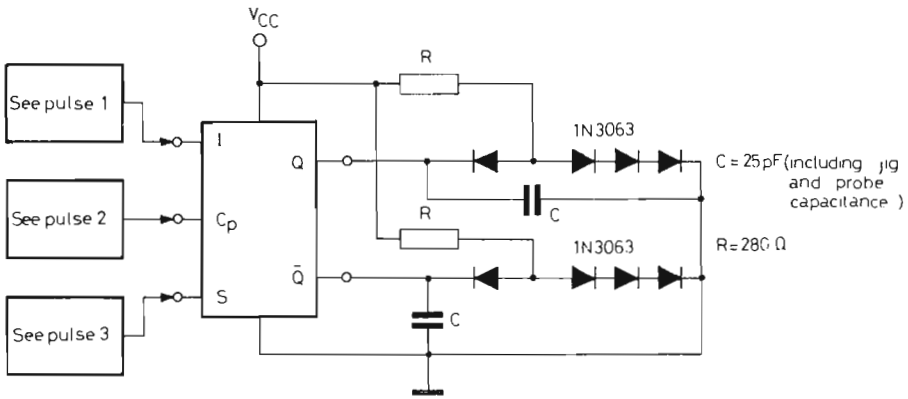
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_{amb}= 25°C)

Parameter		Test conditions*	Min.	Typ.	Max.	Unit
t_{pd0}	Propagation delay time to logical 0 level	C_p =S=0.4V Pulse 1				
		from I to $\overline{Q}$		7	11.5	ns
		from I to Q		15	22	ns
		C_{p2}=S=0.4V Pulse 1 and 2				
		from C_p to $\overline{Q}$		15	22	ns
		from C_p to Q		23	35	ns
		C_{p2}=I= 0.4V Pulse 2 and 3				
		from S to $\overline{Q}$		16	25	ns
t_{pd1}	Propagation delay time to logical 1 level	C_p =S=0.4V Pulse 1				
		from I to $\overline{Q}$		8	13	ns
		from I to Q		14	22	ns
		C_{p2}=S=0.4V Pulse 1 and 2				
		from C_p to $\overline{Q}$		18	26	ns
		from C_p to Q		20	29	ns
		C_{p2}=I= 0.4V Pulse 2 and 3				
		from S to Q		12	19	ns
t_S	Set-up time	C_{p2}=S=0.4V Pulse 1 and 3	15			ns
t_{rel}	Release time	C_{p2}=S=0.4V Pulse 1 and 3			15	ns

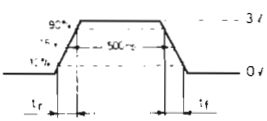
* See switching time test circuit, waveforms and truth table.

SWITCHING TIMES

Test circuit

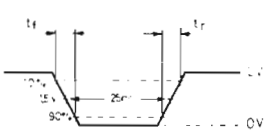


Pulse 1



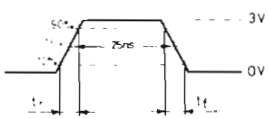
PRR = 1 MHz $t_r = t_f = 7$ ns

Pulse 2



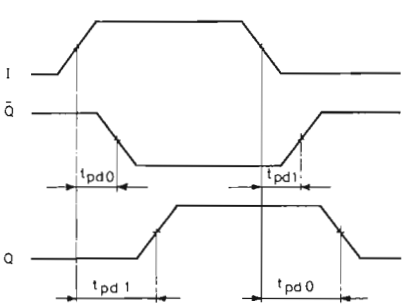
PRR = 2 MHz $t_r = t_f = 7$ ns

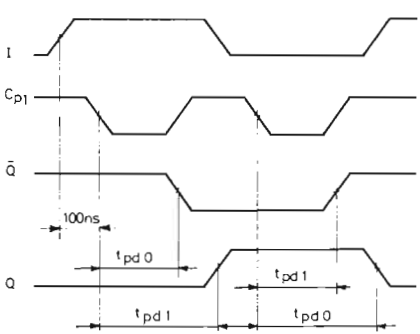
Pulse 3



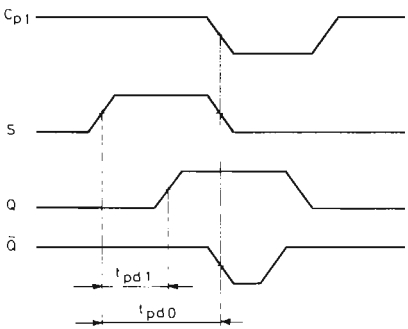
PRR = 2 MHz $t_r = t_f = 7$ ns

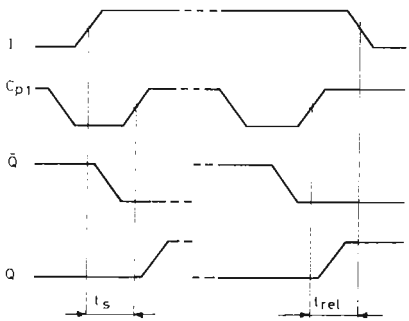
Waveforms





Waveforms (continued)





TTL INTEGRATED CIRCUIT

T 174

TRIPLE LINE RECEIVER

- HIGH SPEED
- FAN-OUT of TEN (10) with STANDARD TTL INTEGRATED CIRCUITS
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- INPUT SENSIBILITY of 200 mV
- SINGLE 5 V POWER SUPPLY

The T 174 is a triple line receiver constructed on a single silicon chip using the planar epitaxial process. Constructed with a common voltage supply and ground terminal, the T 174 has a TTL compatible active pull-up. The input sensitivity (200 mV) is particularly important when data have to be detected at the end of long transmission line.
The receiver high impedance input structure presents a minimal load to the driver and minimizes line reflections.
Available in the standard temperature range (0 to 75°C), it comes in 16-lead dual in-line plastic package.

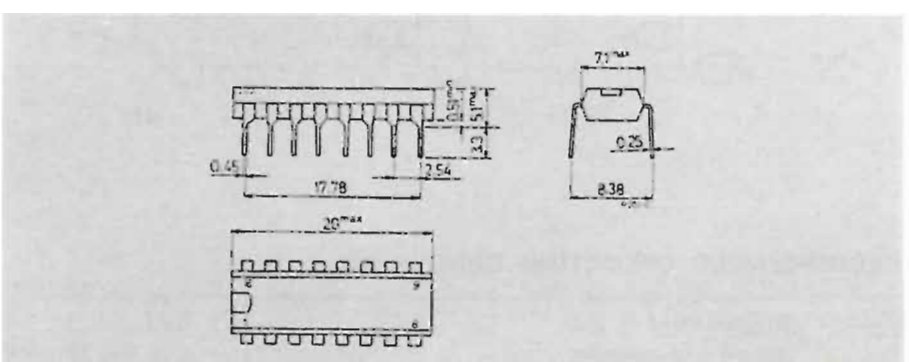
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
T_{stg}	Storage temperature	-55 to 125	°C
T_{op}	Operating temperature	0 to 75	°C

ORDERING NUMBER : T 174 B1

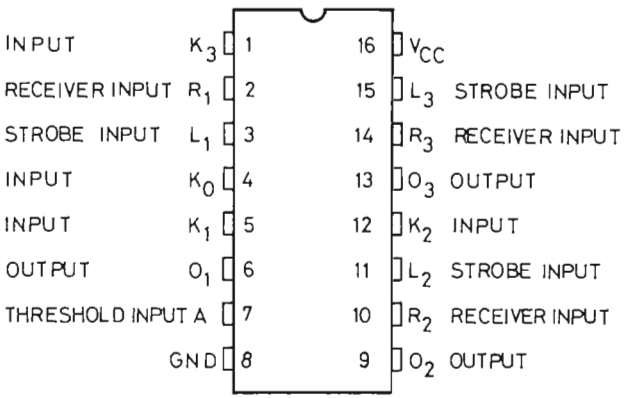
MECHANICAL DATA

Dimensions in mm



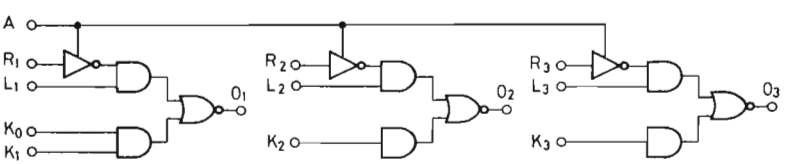
T 174

CONNECTION DIAGRAM
(top view)



S-0228

FUNCTIONAL LOGIC DIAGRAM



S-0229

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
T_{op}	Operating temperature	0 to 75	°C

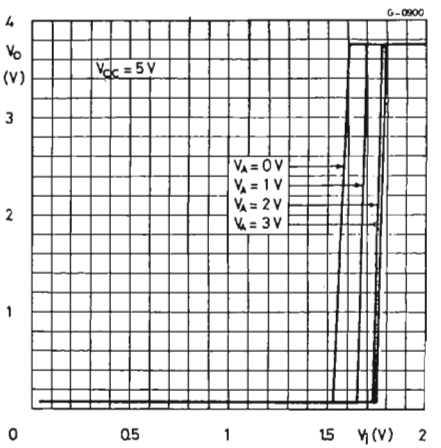
ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Output low voltage	V_{CC}= 4.75V I_{OL}= 16 mA V_R= 1.3V V_A= 0V V_L= 2V V_K= 0.8V			0.4	V
		V_{CC}= 4.75V I_{OL}= 16 mA V_R= 1.5V V_A= 5V V_L= 2V V_K= 0.8V			0.4	V
		V_{CC}= 4.75V I_{OL}= 16 mA V_L= 0.8V V_K= 2V			0.4	V
V_{OH}	Output high voltage	V_{CC}= 4.75V I_{OH}=-800µA V_R= 1.7V V_A= 0V V_L= 2V V_K= 0.8V	2.4			V
		V_{CC}= 4.75V I_{OH}=-800µA V_R= 1.9V V_A= 5V V_L= 2V V_K= 0.8V	2.4			V
		V_{CC}= 4.75V I_{OH}=-800µA V_L= V_K= 0.8V	2.4			V
I_{IL}	Input low current	V_{CC}= 5.25V V_i= 0.4V V_R= 0V			-1.6	mA
I_{IH}	Input high current	V_{CC}= 5.25V V_R= 4.5V V_i= 2.4V			40	µA
		V_{CC}= 5.25V V_R= 4.5V V_i= 5.5V			1	mA
I_{RH}	Receiver input high current	V_{CC}= 5.25V V_R= 3.8V			0.28	mA
I_{CC}	Power dissipation current	V_{CC}= 5.25V			72	mA
I_{SC} *	Output short circuit current	V_{CC}= 5.25V V_o= GND All inputs grounded	-50		-100	mA

* Only one output shorted at a time

Typical transfer characteristics

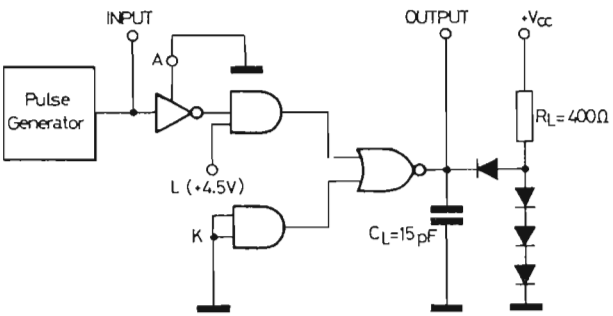


SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_{amb} 25°C

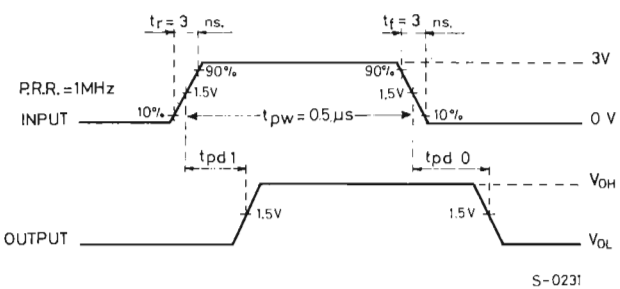
Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{pd1}	Propagation delay time to logical 1	See switching time test circuit and waveforms		18	30	ns
t_{pd0}	Propagation delay time to logical 0	See switching time test circuit and waveforms		15	25	ns

SWITCHING TIMES

Test circuit

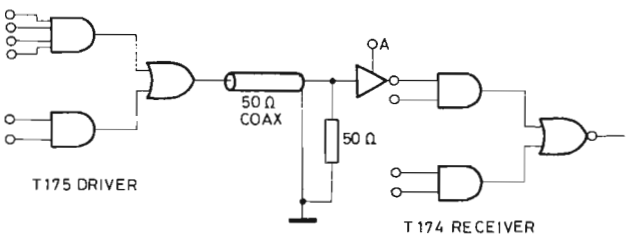


Waveforms

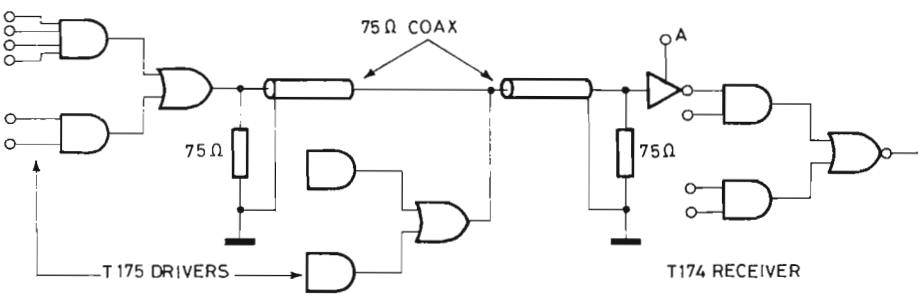


T 174

TYPICAL APPLICATIONS



S-0341



S-0342

If more than one driver/receiver is to be used for each transmission line, the line should be terminated at both ends as shown.

TTL INTEGRATED CIRCUIT

T 175

DUAL LINE DRIVER

- HIGH-POWER DRIVE CAPABILITY
- SHORT CIRCUIT PROTECTION
- TTL or DTL COMPATIBLE DIODE-CLAMPED INPUTS
- EMITTER-FOLLOWER OUTPUTS

The T 175 is a circuit constructed on a single silicon chip by means of the planar epitaxial process. It is designed to drive 50 Ω or 75 Ω coaxial transmission lines. TTL multiple emitter inputs allow this line driver to interface with standard TTL or DTL system. The outputs are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with impedances of 50 to 500 Ω .
The output stages have short circuit protection against overload on the line.
Available in standard temperature range (0 to 75°C), it comes in a 16-lead dual in-line ceramic package.

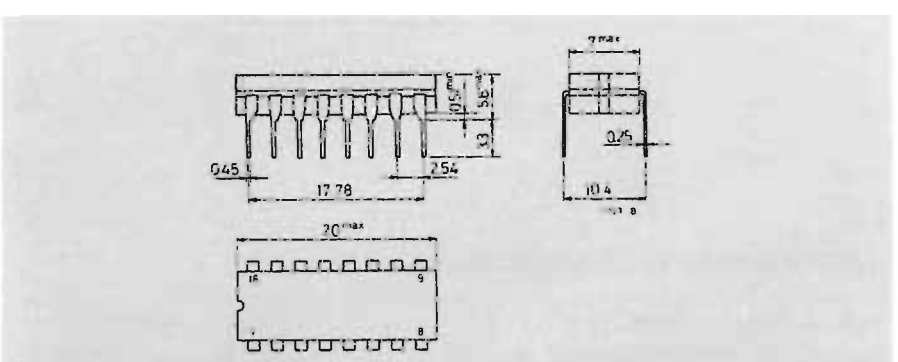
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
V_o	Output voltage	5.5	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 75	°C

ORDERING NUMBER: T 175 D1

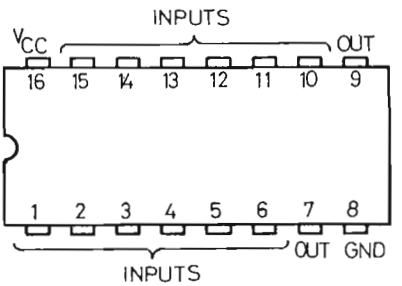
MECHANICAL DATA

Dimensions in mm



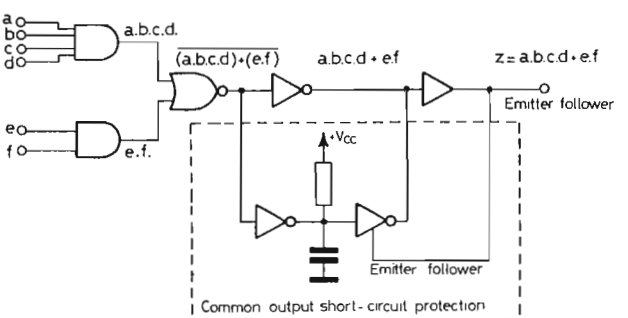
T 175

CONNECTION DIAGRAM
(top view)



S-0232

FUNCTIONAL LOGIC DIAGRAM
(half T 175)



S-0233

RECOMMENDED OPERATING CONDITIONS

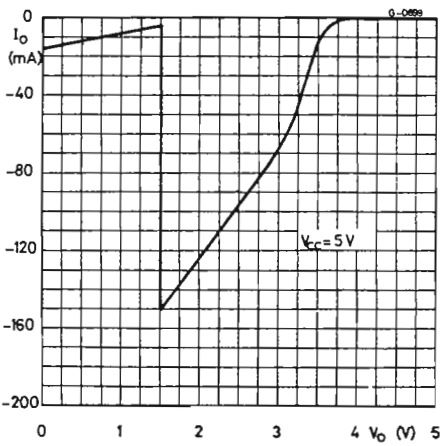
V_{CC}	Supply voltage	4.75 to 5.25	V
T_{op}	Operating temperature	0 to 75	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	V_{CC}= 4.75V	2			V
V_{IL}	Input low voltage	V_{CC}= 4.75V			0.8	V
V_{OH}	Output high voltage	V_{CC}= 4.75V V_i= 2V I_{OH}= -75 mA	2.4			V
I_{OL}	Output low current (each output)	V_{CC}= 5.25V V_i= 2V V_{OL}= 1.9V	-100		-230	mA
I_{OL1}	Output low current (each output)	V_{CC}= 5.25V V_i= 2V V_{OL}= 1.3V			-15	mA
I_{IL}	Input low current (each input)	V_{CC}= 5.25V V_i= 0.4V			-1.6	mA
I_{IH}	Input high current (each input)	V_{CC}= 5.25V V_i= 2.4V V_{CC}= 5.25V V_i= 5.5V			40 1	µA mA
I_{CEX}	Output leakage current	V_{CC}= 5.25V V_i= 0.8V V_{OL}= 0V			-1	mA
I_{OR}	Output reverse current	V_{CC}= 0V V_i= 0.8V V_{OH}= 3V			500	µA
I_{SC}	Short-circuit current (each output)	V_{CC}= 5.25V V_i= 2V V_{OL}= 0V			-30	mA
I_{CCH}	High power dissipation current (without loads)	V_{CC}= 5.25V V_i= 4.5V			28	mA
I_{CCL}	Low power dissipation current (without loads)	V_{CC}= 5.25V V_i= 0.4V			50	mA

Typical output current

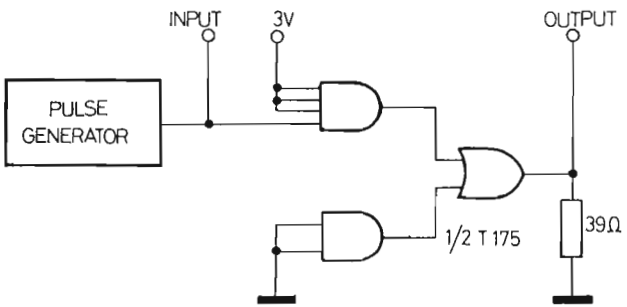


SWITCHING CHARACTERISTICS (V_{CC}= 5V, T_{amb} 25°C)

Parameter		Test conditions	Min. Typ. Max.	Unit
t_{pd1}	Propagation delay time to logical 1	See switching times test circuit and waveforms	20	ns
t_{pd0}	Propagation delay time to logical 0	See switching times test circuit and waveforms	20	ns

SWITCHING TIMES

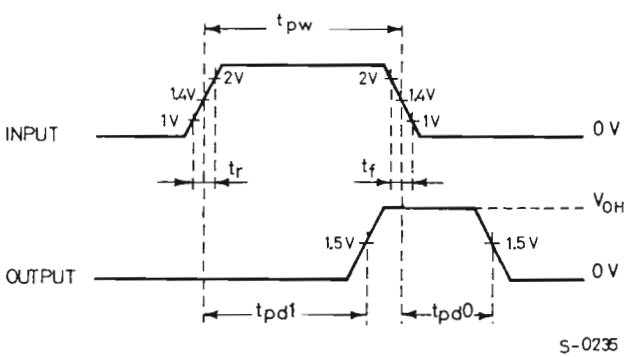
Test circuit



S-0237

INPUT PULSE : Amplitude = 3.0V
t_{pw} = 40 ns (50% Duty Cycle)
t_r = 3 ns t_f = 2 ns

Waveforms



S-0235

TYPICAL APPLICATIONS

A typical application for the T 175 is shown in Figure 1. If only one line driver is to be used for each transmission line, the line may be terminated with 50 ohms on the receiving end only. See Figure 2.

Figure 1

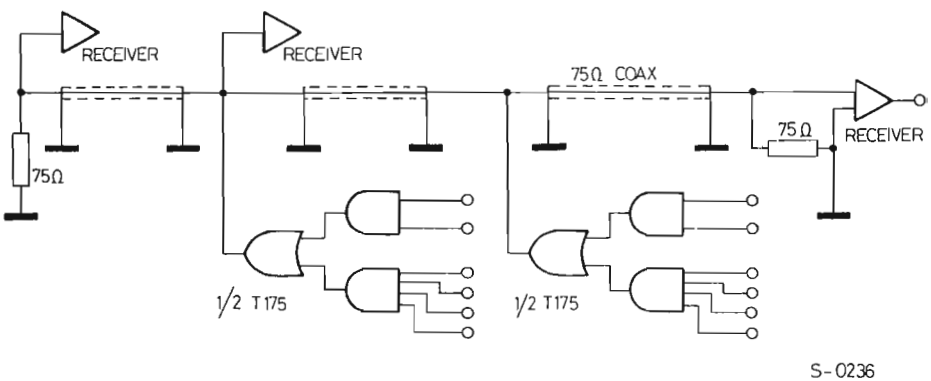
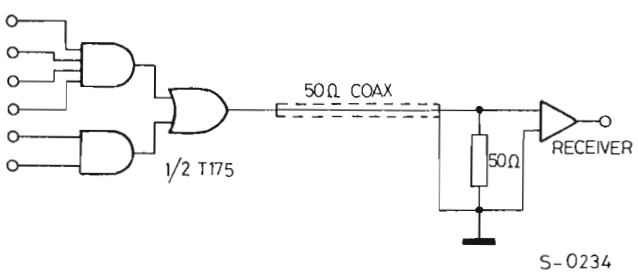


Figure 2



TTL INTEGRATED CIRCUIT

T 176

PRELIMINARY DATA

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

- ACTIVE PULL-UP OUTPUTS
- OUTPUT DRIVE CAPABILITY of 10
- NOISE IMMUNITY of 1V
- DTL-TTL COMPATIBILITY

The T 176 is a DC dual level sensitive retriggerable and resettable monostable multivibrator, which provides an output pulse whose duration is a function of external timing components only. The T 176 has two inputs, one of which is active level high and one of which is active level low; this allows a choice of leading edge or trailling edge triggering. The output pulse may be terminated at any time by taking reset pin to a low logic level. This device is available in 16-lead dual in-line plastic and ceramic package for a standard temperature range (0 to 75 °C).

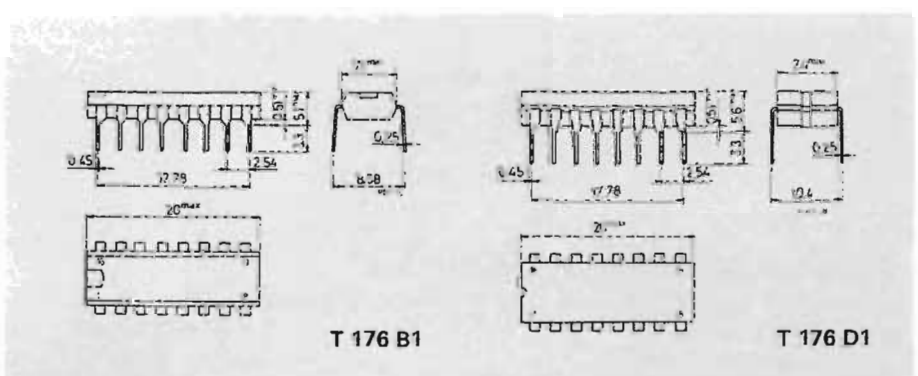
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	-0.5 to 8	V
V_i	Input voltage	5.5	V
T_{op}	Operating temperature	0 to 75	°C
T_{stg}	Storage temperature	-55 to 125	°C

ORDERING NUMBERS: T 176 B1 for dual in-line plastic package
T 176 D1 for dual in-line ceramic package

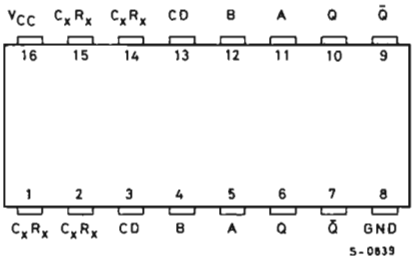
MECHANICAL DATA

Dimensions in mm

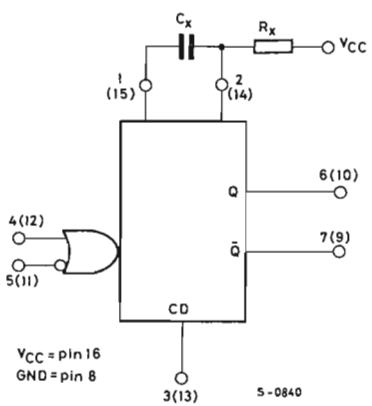


T 176

CONNECTION DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
T_{op}	Operating temperature	0 to 75	°C

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.*	Max.	Unit
V_{OH}	Output high voltage	V_{CC} = 4.75V I_{OH} = -0.96mA	2.4	3.4		V
V_{OL}	Output low voltage	V_{CC} = 4.75V I_{OL} = 11.3 mA V_{CC} = 5.25V I_{OL} = 12.8 mA		0.25 0.25	0.45 0.45	V V
V_{IH}	Input high voltage		1.8			V
V_{IL}	Input low voltage				0.85	V
I_{IL}	Input low current	V_{CC} = 5.25V V_{IL} = 0.45V		-1	-1.6	mA
I_{IR}	Input reverse current	V_{CC} = 5.25V V_{IR} = 4.5V		15	60	μA
I_{SC}**	Short-circuit output current	V_{CC} = 5.25V	-8		-50	mA
I_{PD}	Power dissipation current	V_{CC} = 5V GND pins 5 and 11		35		mA

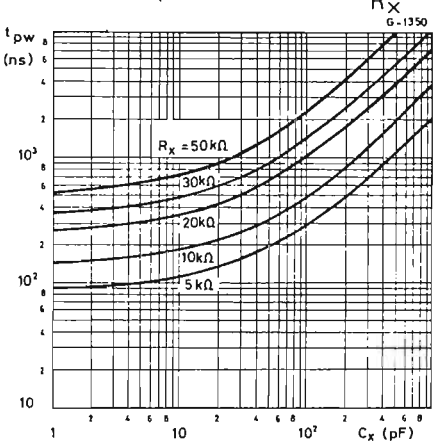
* All typical values are at V_{CC} = 5V, T_{amb} = 25 °C

** Not more than one output should be shorted at a time

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25 °C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$t_{pd\ 1}$	Propagation delay time to logical 1 level	C_L = 15 pF R_X = 5 kΩ C_X = 0		27		ns
$t_{pd\ 0}$	Propagation delay time to logical 0 level	C_L = 15 pF R_X = 5 kΩ C_X = 0		27		ns
t_{pw}	Minimum pulse width	C_L = 15 pF R_X = 5 kΩ C_X = 0		80		ns
t_{pw}	Pulse width	C_X = 1000 pF R_X = 10 kΩ		3.8		μs
R_X	External timing resistor		5		50	kΩ

Output pulse width vs. timing resistance and capacitance for $C_X < 10^3$ pF for $C_X \geq 10^3$ pF, $t_{pw} = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X})$



OPERATION RULES

a) An external resistor R_X and an external capacitor C_X are required. The values of R_X may vary from 5 kΩ to 50 kΩ, C_X may vary from 0 to any value necessary and obtainable.

b) Is recommended R_X = 30 kΩ if a fixed value of R_X is used.

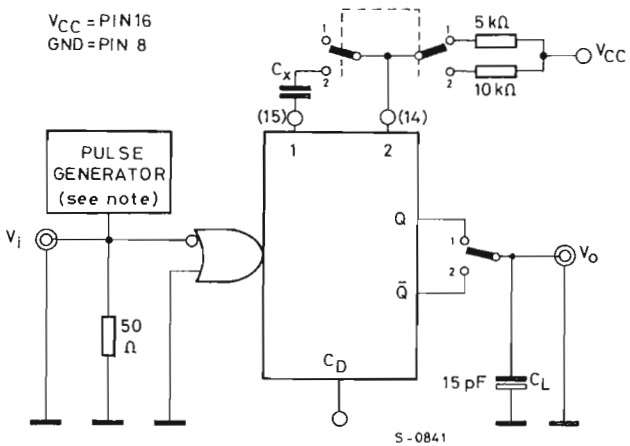
c) The output pulse width t is defined as follows:

$$t = 0.35\ R_X C_X\ [1 + \frac{0.85}{R_X}] \text{ for } C_X > 10^3 \text{ pF}$$

Where R_X is in kΩ
C_X is in pF
t is in ns

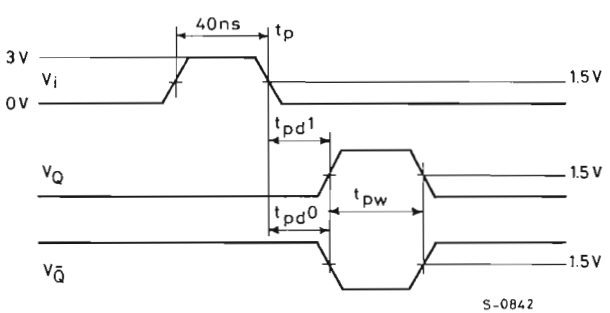
SWITCHING TIMES

Test circuit



NOTE: The pulse generator has the following characteristics; $V_i = 3V$, $t_r = t_f \leqslant 10$ ns, $t_p = 40$ ns PRR = 100 kHz.

Waveforms



TTL INTEGRATED CIRCUITS

TRANSISTOR-TRANSISTOR LOGIC

- COMPATIBLE WITH OTHER TTL or DTL FAMILY PRODUCTS
- NOISE IMMUNITY 1V
- WORST CASE NOISE IMMUNITY 0.4V
- OUTPUT DRIVE CAPABILITY of 10
- POWER DISSIPATION 10 mW per GATE
- GATE PROPAGATION DELAY 10 ns

The T 54/74 series of TTL integrated circuit combines high fanout, high noise immunity, low power dissipation and low propagation delay times and can therefore be used in any digital system.
Series T 54 are integrated circuits available in 14 or 16-lead dual in-line ceramic package.
Series T 74 are integrated circuits available in 14 or 16-lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS

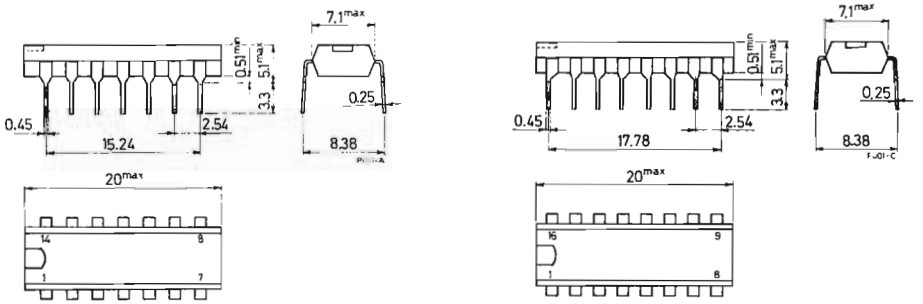
V_{CC}	Supply voltage		7	V
V_i	Input voltage		5.5	V
T_{stg}	Storage temperature		-65 to 150	°C
T_{op}	Operating temperature:	for T 54 type	-55 to 125	°C
		for T 74 types	0 to 70	°C

ORDERING NUMBERS:

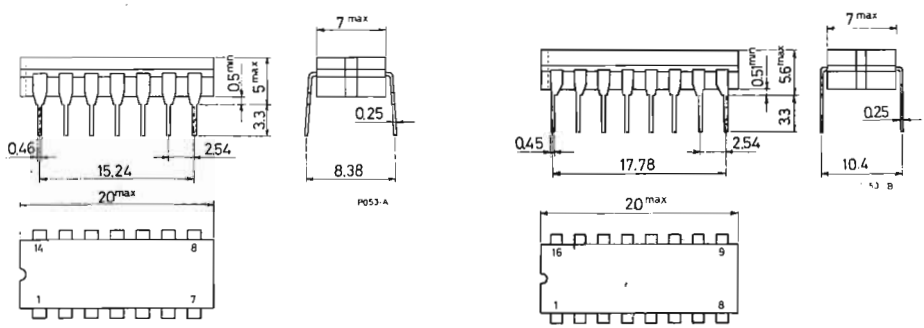
T 54 XX D2 for dual in-line ceramic package
T 74 XX B1 for dual in-line plastic package
T 74 XX D1 for dual in-line ceramic package

MECHANICAL DATA (dimensions in mm)

Dual in-line plastic packages: for T 74 XX B1



Dual in-line ceramic packages: for T 74 XX D1
for T 54 XX D2



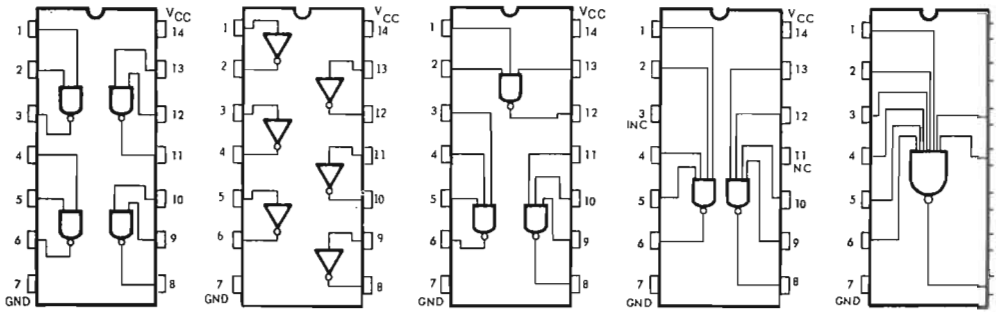
RECOMMENDED OPERATING CONDITIONS

V_{CC}*	Supply voltage:	for **T 54** type	4.5 to 5.5	V
		for T **74** types	4.75 to 5.25	V
N	Normalized fanout (each output)		max 10	
T_{op}	Temperature range:	for **T 54** type	-55 to 125	°C
		for T **74** types	0 to 70	°C

* These are measured with respect to the ground.

INDEX

CONNECTION DIAGRAMS (Top view)



T 7400 T 7404 T 7410 T 7420 T 7430

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

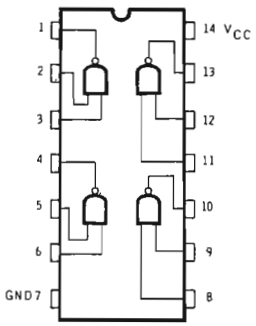
PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC}= MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC}= MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}= MIN V_{in}= 0.8 V I_{load} = -400 µA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC}= MIN V_{in}= 2 V I_{sink} = 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC}= MAX V_{in}= 0.4V			- 1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC}= MAX V_{in}= 2.4V V_{CC}= MAX V_{in}= 5.5V			40 1	µA mA
I_{OS}	Short circuit output current (***)	V_{CC}= MAX	- 18		- 55	mA
$I_{CC(0)}$	Logical 0 level supply current/gate	V_{CC}= MAX V_{in}= 5 V		3	5.5	mA
$I_{CC(1)}$	Logical 1 level supply current/gate	V_{CC}= MAX V_{in}= 0		1	2	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

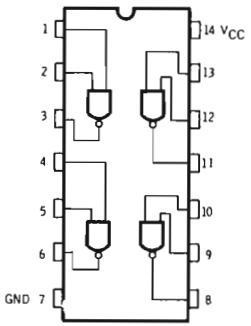
PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	26	C_L = 15pF R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	26	C_L = 15pF R_L = 400 Ω		12	22	ns

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be shorted at a time.

CONNECTION DIAGRAMS (Top view)



T 7401



T 7403

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on) level at output	V_{CC}= MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off) level at output	V_{CC}= MIN			0.8	V
$I_{out(1)}$	Output reverse current	V_{CC}= MIN V_{in} =0.8V $V_{out(1)}$ =5.5V			250	µA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC}= MIN V_{in}= 2 V I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC}= MAX V_{in} =0.4 V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC}= MAX V_{in} =2.4 V			40	µA
		V_{CC}= MAX V_{in} =5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current /gate	V_{CC}= MAX V_{in} = 5 V		3	5.5	mA
$I_{CC(1)}$	Logical 1 level supply current /gate	V_{CC}= MAX V_{in} = 0		1	2	mA

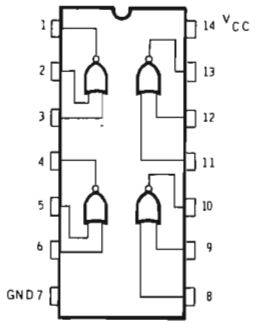
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	27	C_L=15pF R_L=400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	27	C_L=15pF R_L=4KΩ		35	45	ns

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions

(**) All typical values are at V_{CC} = 5V, T_A = 25°C.

CONNECTION DIAGRAM (Top view)



T 7402

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

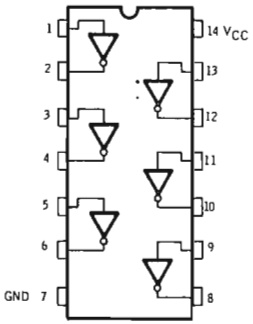
PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	V_{CC}= MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	V_{CC}= MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}=MIN V_{in}= 0.8V I_{load} = - 400 µA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} =MIN V_{in}= 2 V I_{sink}= 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC}= MAX V_{in}= 0.4 V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC}= MAX V_{in}= 2.4 V V_{CC}= MAX V_{in}= 5.5 V			40 1	µA mA
I_{OS}	Short-circuit output current (***)	V_{CC}= MAX	-18		- 55	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC}= MAX V_{in} = 5 V		14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC}= MAX V_{in} = 0		8	16	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	26	C_L=15pF R_L=400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	26	C_L=15pF R_L=400 Ω		12	22	ns

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions
(**) All typical values are at V_{CC} = 5 V, T_A = 25°C
(***) Not more than one output should be shorted at a time.

CONNECTION DIAGRAM (Top view)



T 7405 - T 7406 - T 7416

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

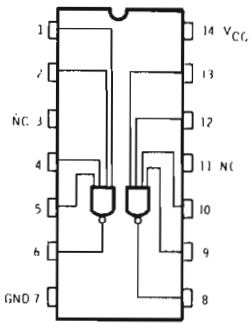
PARAMETER		TEST CONDITIONS (*)			Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	V_{CC} = MIN					0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, V_{in} = 0.8V	$V_{out(1)}$ = 5.5V	T7405			250	µA
			$V_{out(1)}$ = 30V	T7406				
			$V_{out(1)}$ = 15V	T7416				
$V_{out(0)}$	Logical 0 output voltage (on) level	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16mA					0.4	V
		V_{CC} = MIN, V_{in} = 2V, I_{sink} = 40 mA		T7406 T7416			0.7	
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX, V_{in} = 0.4V					- 1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX, V_{in} = 2.4V					40	µA
		V_{CC} = MAX, V_{in} = 5.5V					1	mA
$I_{CC(0)}$	Logical 0 level supply current/ gate	V_{CC} = 5V, V_{in} = 5V, T_A = 25°C		T7405		3	5.5	mA
				T7406 T7416		4.5	6.3	
$I_{CC(1)}$	Logical 1 level supply current/ gate	V_{CC} = 5V, V_{in} = 0, T_A = 25°C		T7405		1	2	mA
				T7406 T7416		5	7	

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER		Test Figure	TEST CONDITIONS		Min.	Typ.	Max.	Unit
t_{pd0}	Propagation delay time to logical 0 level	27	C_L = 15pF, R_L = 400Ω	T7405		8	15	ns
			C_L = 15pF, R_L = 110Ω	T7406 T7416		13	20	
t_{pd1}	Propagation delay time to logical 1 level	27	C_L = 15pF, R_L = 4KΩ	T7405		40	55	ns
			C_L = 15pF, R_L = 110Ω	T7406 T7416		17	26	

(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All Typical values are at V_{CC} = 5V, T_A = 25°C.

CONNECTION DIAGRAM (Top view)



T 7440

ELECTRICAL CHARACTERISTICS (over recommended free-air temperature range unless otherwise noted)

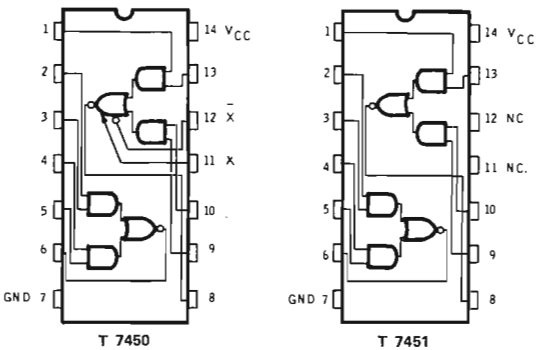
PARAMETER		TEST CONDITIONS (*)	Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN V_{in} = 0.8V I_{load} = - 1.2mA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN V_{in} = 2V I_{sink} = 48mA		0.28	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{in} = 2.4V			40	µA
		V_{CC} = MAX V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current (***)	V_{CC} = MAX	-18		-70	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX V_{in} = 5V		17	27	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX V_{in} = 0		4	8	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 30)

PARAMETER		TEST FIGURE	TEST CONDITIONS	Min.	Typ.	Max.	Unit
t_{pd0}	Propagation delay time to logical 0 level	26	C_L = 15pF R_L = 133 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	26	C_L = 15pF R_L = 133 Ω		13	22	ns

(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be shorted at a time.

CONNECTION DIAGRAMS (Top view)



ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	V_{CC}= MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC}= MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}= MIN V_{in}= 0.8 V I_{load} = - 400 µA	2.4	3.3		V
Vout(0)	Logical 0 output voltage	V_{CC}= MIN V_{in}= 2 V I_{sink} = 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC}= MAX V_{in}= 0.4 V			- 1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC}= MAX V_{in}= 2.4 V			40	µA
		V_{CC}= MAX V_{in}= 5.5 V			1	mA
IOS	Short-circuit output current (***)	V_{CC}= MAX	-18		- 55	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC}= MAX V_{in} = 5 V		7.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC}= MAX V_{in} = 0		4	8	mA

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions. Expander inputs X and $\overline{X}$ are open.

(**) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(***) Not more than one output should be shorted at a time.

ELECTRICAL CHARACTERISTICS (T 7450 circuit) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.(**)	MAX.	UNIT
I_X	Expander current	1	V_I = 0.4V I_{sink}=16 mA			3.1	mA
$V_{BE(Q)}$	Base emitter voltage of output transistor (Q)	2	I_{sink}=16 mA I_1=0.62 mA R_1=0			1	V
$V_{out(1)}$	Logical 1 output voltage	3	I_{load}=-400µA I_1 =-I_2 =270µA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	2	I_{sink}=16mA I_1= 0.43mA R_1 = 130 Ω		0.22	0.4	V

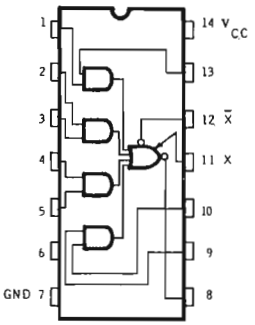
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25° C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS (*)	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	28	C_L=15 pF R_L=400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	28	C_L=15 pF R_L=400 Ω		13	22	ns

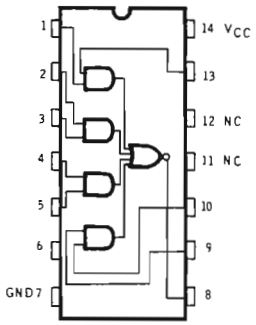
(*) Expander inputs X and $\overline{X}$ are open .

(**) All typical values are at V_{CC}=5 V, T_A=25°C .

CONNECTION DIAGRAMS (Top view)



T 7453



T 7454

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of one AND section to ensure logical 0 level at output	V_{CC}= MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 level at output	V_{CC}= MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}= MIN V_{in}= 0.8 V I_{load} = - 400 µA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN V_{in} = 2 V I_{sink} = 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX V_{in} =0.4 V			- 1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{in} =2.4 V			40	µA
		V_{CC} = MAX V_{in} =5.5 V			1	mA
I_{OS}	Short-circuit output current (***)	V_{CC} = MAX	- 18		- 55	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX V_{in} = 5 V		5.1	9.5	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX V_{in} = 0		4	8	mA

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions. Expander inputs X and $\overline{X}$ are open.

(**) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(***) Not more than one output should be shorted at a time.

ELECTRICAL CHARACTERISTICS (T7453 circuit) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.(**)	MAX.	UNIT
I_X	Expander current	1	V_I =0.4V I_{sink}=10 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	2	I_{sink}=16mA I_I=0.62 mA R_I = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	3	I_{load}=-400μA I_1=-I_2=270 μA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	2	I_{sink}=16 mA I_I=0.43 mA R_I= 130 Ω		0.22	0.4	V

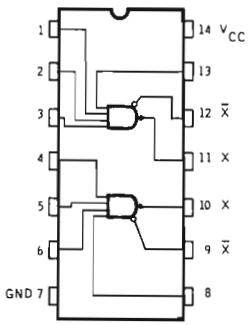
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS (*)	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	28	C_L=15pF R_L=400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	28	C_L=15pF R_L=400 Ω		13	22	ns

(*) Expander inputs X and $\overline{X}$ are open.

(**) All typical values, are at V_{CC} = 5V, T_A = 25°C.

CONNECTION DIAGRAM (Top view)



T 7460

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		Test Fig.	TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure that the output is in the on state	4	V_{CC}=MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure that the output is in the off state	5	V_{CC}=MIN			0.8	V
V_{on}	On-state output voltage	4	V_{CC}=MIN V_{in} = 2 V V_I=1V R=1.1K T_A=0°C			0.4	V
I_{off}	Off-state output current	5	V_{CC}=MIN, V_{in}=0.8V, T_A=0°C V_I=4.5V R=1.2 K			270	µA
I_{on}	On-state output current	6	V_{CC}=MIN, V_{in}=2V, V_I=1V	-0.43			mA
$I_{in(0)}$	Logical 0 level input current (each input)		V_{CC}=MAX, V_{in}=0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)		V_{CC}=MAX, V_{in}=2.4V V_{CC}=MAX, V_{in}=5.5V			40 1	uA mA
$I_{CC(on)}$	On-state supply current	7	V_{CC}=MAX, V_{in}=5 V, V_I = 0.85 V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	7	V_{CC}=MAX, V_{in}= 0, V_I= 0.85 V		2	4	mA

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	29	C_L=15pF R_L=400 Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level	29	C_L=15pF R_L=400 Ω		15	30	ns

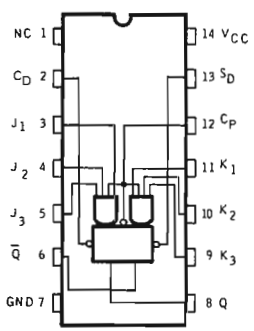
DESCRIPTION

This J-K flip-flop is based on the master-slave principle and has AND gate inputs for entry into the master section which is controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows :

1) Isolate slave from master.
2) Enter information from AND gate inputs to master.
3) Disable AND gate inputs.
4) Transfer information from master to slave.

CLOCK WAVEFORM

CONNECTION DIAGRAM (Top view)



T 7472

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES :
1) J = J1 · J2 · J3
2) K = K1 · K2 · K3
3) t_n = Bit time before clock pulse
4) t_{n+1} = Bit time after clock pulse
5) NC = No internal connection.

RECOMMENDED OPERATING CONDITIONS

– Width of clock pulse, t_p (clock)	20 ns (min)
– Width of preset pulse t_p (preset)	25 ns (min)
– Width of clear pulse, t_p (clear)	25 ns (min)
– Input setup time, t_{setup}	$\geq t_p$ (clock)
– Input hold time, t_{hold}	0 (min)

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC}=MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC}=MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}=MIN I_{load}=-400μA	2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC}=MIN I_{sink}= 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	V_{CC}=MAX V_{in} = 0.4 V			- 1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	V_{CC}=MAX V_{in} = 0.4 V			- 3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	V_{CC}=MAX V_{in} = 2.4 V V_{CC}=MAX V_{in} = 5.5 V			40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	V_{CC}=MAX V_{in} = 2.4 V V_{CC}=MAX V_{in} = 5.5 V			80 1	μA mA
I_{OS}	Short - circuit output current (***)	V_{CC}=MAX V_{in} = 0	- 18		- 57	mA
I_{CC}	Supply current	V_{CC}=MAX V_{in} = 5 V		10	20	mA

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(***) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	31	C_L=15pF R_L=400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	32	C_L=15pF R_L=400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	32	C_L=15pF R_L=400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	31	C_L=15pF R_L=400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	31	C_L=15pF R_L=400Ω	10	25	40	ns

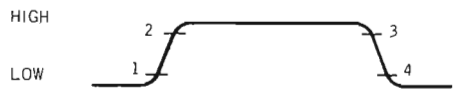
POSITIVE LOGIC

Low Input to Preset sets Q to Logical 1. Low Input to Clear sets Q to Logical 0. Preset and Clear are independent of clock.

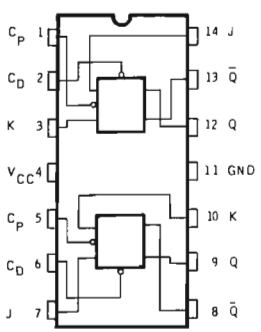
DESCRIPTION

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections.
The sequence of operation is as follows :
1) Isolate slave from master.
2) Enter information from J and K inputs to master.
3) Disable J and K inputs.
4) Transfer information from master to slave.

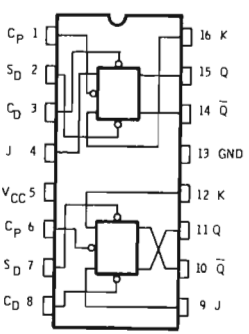
CLOCK WAVEFORM



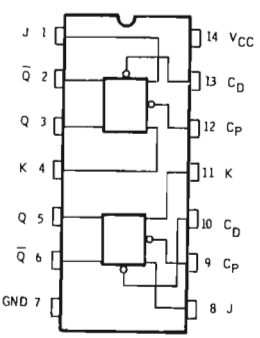
CONNECTION DIAGRAMS (Top view)



T 7473



T 7476



T 74107

TRUTH TABLE
(each flip-flop)

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES
1) t_n = Bit time before clock pulse.
2) t_{n+1} = Bit time after clock pulse.

RECOMMENDED OPERATING CONDITIONS

– Width of clock pulse, t_p (clock)	20 ns (min)
– Width of preset pulse (T7476 only), t_p (preset)	25 ns (min)
– Width of clear pulse, t_p (clear)	25 ns (min)
– Input setup time, t_{setup}	$\geq t_p$ (clock)
– Input hold time, t_{hold}	0 (min)

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC}=MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC}=MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}=MIN I_{load}=-400µA	2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC}=MIN I_{sink}= 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{CC}=MAX V_{in} = 0.4 V			- 1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear, preset (T7476 only), or clock	V_{CC}=MAX V_{in} = 0.4 V			- 3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC}=MAX V_{in} = 2.4 V V_{CC}=MAX V_{in} = 5.5 V			40 1	µA mA
$I_{in(1)}$	Logical 1 level input current at clear, preset (T7476 only), or clock	V_{CC}=MAX V_{in} = 2.4 V V_{CC}=MAX V_{in} = 5.5 V			80 1	µA mA
I_{OS}	Short circuit output current (***)	V_{CC}=MAX V_{in} = 0	-18		- 57	mA
I_{CC}	Supply current	V_{CC}=MAX V_{in} = 5 V		20	40	mA

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

(**) All typical values, are at V_{CC} = 5V, T_A = 25°C.

(***) Not more than one output should be shorted at a time; only for T7473 and T74107 when measuring Q, apply 2.4V to clear, ground $\bar{Q}$ and limit test time to 100 ms.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	31	C_L=15pF R_L=400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	32	C_L=15pF R_L=400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	32	C_L=15pF R_L=400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	31	C_L=15pF R_L=400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	31	C_L=15pF R_L=400Ω	10	25	40	ns

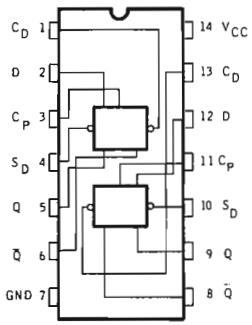
POSITIVE LOGIC:

Low Input to clear sets Q to logical 0. Clear is independent of clock.

DESCRIPTION

These monolithic, dual, D-type, edge-triggered flip-flops feature direct clear and preset inputs and complementary Q and $\bar{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.
Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.
This dual flip-flop is ideally suited for medium-to-high-speed applications. It can result in a significant saving in system power dissipation and package count in applications where input gating is not required.

CONNECTION DIAGRAM (Top view)



T 7474

TRUTH TABLE

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS t_n	OUTPUTS t_{n+1}	
D	Q	$\bar{Q}$
0	0	1
1	1	0

RECOMMENDED OPERATING CONDITIONS

Width of Clock Pulse $t_{p(clock)}$	30 ns
Width of Preset Pulse $t_{p(preset)}$	30 ns
Width of Clear Pulse $t_{p(clear)}$	30 ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC}=MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC}=MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}=MIN I_{load}= -400µA	2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC}=MIN I_{sink}= 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	V_{CC}=MAX V_{in} = 0.4 V			- 1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{CC}=MAX V_{in} = 0.4 V			- 3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC}=MAX V_{in} = 2.4 V			40	µA
		V_{CC}=MAX V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	V_{CC}=MAX V_{in} = 2.4 V			80	µA
		V_{CC}=MAX V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC}=MAX V_{in} = 2.4 V			120	µA
		V_{CC}=MAX V_{in} = 5.5 V			1	mA
I_{OS}	Short circuit output current (***)	V_{CC}=MAX V_{in} = 0	-18		- 57	mA
I_{CC}	Supply current	V_{CC}=MAX V_{in} = 5 V		17	30	mA

Notes: see the following page.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	33	C_L=15pF R_L=400 Ω	15	25		MHz
t_{setup}	Minimum input setup time	33	C_L=15pF R_L=400 Ω		15	20	ns
t_{hold}	Minimum input hold time	33	C_L=15pF R_L=400 Ω		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	34	C_L=15pF R_L=400Ω			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	34	C_L=15pF R_L=400Ω			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	33	C_L=15pF R_L=400 Ω	10	14	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	33	C_L=15pF R_L=400 Ω	10	20	40	ns

POSITIVE LOGIC

Low Input to preset sets Q to logical 1. Low input to clear sets Q to logical 0. Preset and clear are independent of clock.

NOTES :

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

(**) All typical values are at V_{CC} = 5 V, T_A = 25°C.

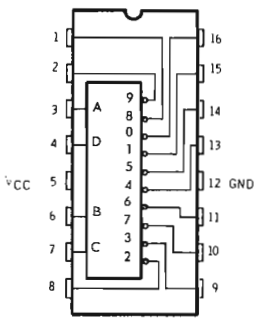
(***) Not more than one output should be shorted at a time.

MSI STANDARD TEMPERATURE RANGE

DESCRIPTION

The T7441A is a monolithic, BCD-to-decimal decoder incorporating high performance output transistors designed for use as indicator or relay drivers.
The BCD-to-decimal decoder consists of familiar transistor - transistor logic (TTL) gate circuits which select one of the ten decimal output drivers. The BCD inputs are fully compatible with Series T74 logic outputs; and, in addition, physical placement of these inputs is coincidental with the BCD outputs of the T7490 decade counter. Decoding and DC switching for components such as miniature lamps and relays may be performed by the T7441A within the ranges specified for the electrical characteristics.

CONNECTION DIAGRAM (Top view)



T 7441 A

positive logic : see truth table.

TRUTH TABLE

INPUT				OUTPUT ON *
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

* All other outputs are off.

ABSOLUTE MAXIMUM RATING (above which the useful life may be impaired)
Current into any Output (off-state) 2 mA

OPERATING CONDITION
Maximum Voltage on any Output 70V

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

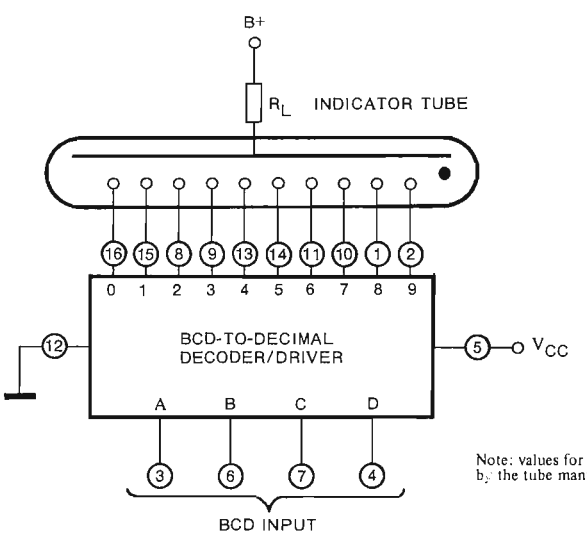
PARAMETER		Test Fig.	TEST CONDITIONS		Min.	Typ.(*)	Max.	Unit
$V_{in(1)}$	Logical 1 input voltage	8	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage	8	V_{CC} = MIN				0.8	V
V_{on}	On-state output voltage	8	V_{CC} = MIN	I_{on} = 7mA			2.5	V
I_{off}	Off-state reverse current	9	V_{CC} = MAX	V_{out} = 55V			50	µA
			V_{CC} = MAX	V_{out} = 70V			2	mA
$I_{in(1)}$	Logical 1 level input current at B, C or D	10	V_{CC} = MAX	V_{in} = 2.4V			40	µA
			V_{CC} = MAX	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at A	10	V_{CC} = MAX	V_{in} = 2.4V			80	µA
			V_{CC} = MAX	V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at B, C or D	11	V_{CC} = MAX	V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current A	11	V_{CC} = MAX	V_{in} = 0.4V			-3.2	mA
I_{CC}	Supply current	10	V_{CC} = MAX			21	42	mA

* This typical value is at V_{CC} = 5V, T_A = 25°C.

TYPICAL APPLICATION DATA

The T7441A output transistors are capable of withstanding voltages and sinking current required to operate most types of gas-filled indicator tubes.

When these decoder/drivers are used in close proximity (on the same circuit board) with standard digital integrated circuits, care should be exercised to ensure that the impedance of the ground bus (including interconnections) is sufficiently low to absorb the normal energy levels resulting from switching the tube elements.

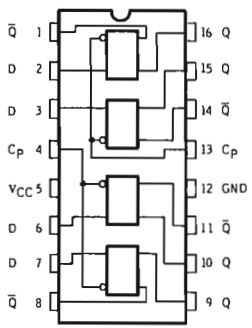


Note: values for B + and R_L are as specified by the tube manufacturer.

DESCRIPTION

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low,the information(which was present at the data input at the time the transition occured) is retained at the Q output until the clock is permitted to go high.
The T7475 features complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in the 16-pin package.
This circuit is completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch.

CONNECTION DIAGRAM (Top view)



T 7475

TRUTH TABLE
(each latch)

t_n	t_{n+1}
D	Q
1	1
0	0

NOTES :
t_n = bit time before clock pulse transition..
t_{n+1} = bit time after clock pulse transition.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		Test Figure	TEST CONDITIONS (*)	Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	12	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	13	V_{CC} = MIN			0.8	V
Vout(1)	Logical 1 output voltage	12 and 13	V_{CC} = MIN I_{load} = -400µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	12 and 13	V_{CC} = MIN I_{sink}=16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at D	14	V_{CC} = MAX V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	14	V_{CC} = MAX			-6.4	mA
$I_{in(1)}$	Logical 1 level input current at D	14	V_{CC} = MAX V_{in} = 2.4V			80	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	14	V_{CC} = MAX V_{in} = 2.4V			160	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current(***)	15	V_{CC} = MAX V_{out} = 0	-18		-57	mA
I_{CC}	Supply current	16	V_{CC} = MAX		32	53	mA

(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C. (***) Not more than one output should be shorted at a time

SWITCHING CHARACTERISTICS, (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Figure	TEST CONDITIONS	Min.	Typ.	Max.	Unit
$t_{setup\ 1}$	Minimum logical 1 level input setup time at D input	35	C_L = 15pF R_L = 400 Ω		7	20	ns
$t_{setup\ 0}$	Minimum logical 0 level input setup time at D input	35	C_L = 15pF R_L = 400 Ω		14	20	ns
$t_{hold\ 1}$	Maximum logical 1 level input hold time required at D input	35	C_L = 15pF R_L = 400 Ω	0	15 *		ns
$t_{hold\ 0}$	Maximum logical 0 level input hold time required at D input	35	C_L = 15pF R_L = 400 Ω	0	6 *		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	35	C_L = 15pF R_L = 400 Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	35	C_L = 15pF R_L = 400 Ω		14	25	ns
$t_{pd1(D-\bar{Q})}$	Propagation delay time to logical 1 level from D input to $\bar{Q}$ output	35	C_L = 15pF R_L = 400 Ω		24	40	ns
$t_{pd0(D-\bar{Q})}$	Propagation delay time to logical 0 level from D input to $\bar{Q}$ output	35	C_L = 15pF R_L = 400 Ω		7	15	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	35	C_L = 15pF R_L = 400 Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	35	C_L = 15pF R_L = 400 Ω		7	15	ns
$t_{pd1(C-\bar{Q})}$	Propagation delay time to logical 1 level from clock input to $\bar{Q}$ output	35	C_L = 15pF R_L = 400 Ω		16	30	ns
$t_{pd0(C-\bar{Q})}$	Propagation delay time to logical 0 level from clock input to $\bar{Q}$ output	35	C_L = 15pF R_L = 400 Ω		7	15	ns

* These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

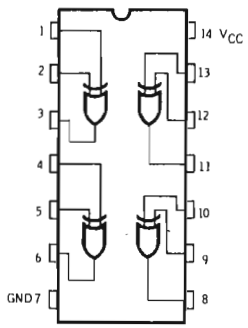
MSI

STANDARD TEMPERATURE RANGE

DESCRIPTION

This monolithic, quadruple 2-input exclusive-OR gate utilizes TTL circuitry to perform the function : $Y = A\overline{B} + \overline{A}B$. When the input states are complementary, the output goes to a logical 1.
This circuit is fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized series T74 load. A full fan out to 10 normalized series T74 loads is available from each of the outputs in the logical 0 state. A fan-out of 20 is provided in the logical 1 state. Propagation delay is 12 nanoseconds and power dissipation is 37.5 milliwatts typically for each exclusive-OR function.

CONNECTION DIAGRAM (Top view)



T 7486

TRUTH TABLE

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN $V_{in(1)}$ = 2V $V_{in(0)}$ = 0.8V I_{load} = -800µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN $V_{in(1)}$ = 2V $V_{in(0)}$ = 0.8V I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{in} = 2.4V			40	µA
		V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX V_{in} = 0.4V			- 1.6	mA
I_{OS}	Short circuit output current (***)	V_{CC} = MAX $V_{in(1)}$ = 4.5V $V_{in(0)}$ = 0	- 18		- 55	mA
I_{CC}	Supply current	V_{CC} = MAX V_{in} = 4.5V		30	50	mA

(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Figure	TEST CONDITIONS	Min.	Typ.	Max.	Unit
t_{pd0}	Propagation delay time to logical 0 level (other input low)	30	C_L = 15pF R_L = 400 Ω		11	17	ns
t_{pd1}	Propagation delay time to logical 1 level (other input low)	30	C_L = 15pF R_L = 400 Ω		15	23	ns
t_{pd0}	Propagation delay time to logical 0 level (other input high)	30	C_L = 15pF R_L = 400 Ω		13	22	ns
t_{pd1}	Propagation delay time to logical 1 level (other input high)	30	C_L = 15pF R_L = 400 Ω		18	30	ns

MSI

STANDARD TEMPERATURE RANGE

DESCRIPTION AND TYPICAL COUNT CONFIGURATIONS

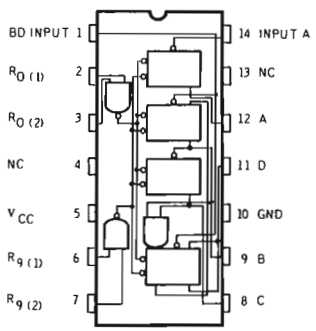
This high-speed, monolithic decade counter consists of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter.Gated direct reset lines are provided to inhibit count inputs and return all outputs to logical zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes :

1) When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown below. In addition to a conventional zero reset, inputs are provided for a reset to nine.

2) If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.

3) For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

CONNECTION DIAGRAM (Top view)



T 7490

TRUTH TABLES

BCD COUNT SEQUENCE (note 1)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (note 2)

RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NOTES :

1) Output A connected to input BD for BCD count.
2) X indicates that either a logical 1 or a logical 0 may be present.

MSI

STANDARD TEMPERATURE RANGE

OPERATING CONDITIONS

Width of Input Count Pulse, $t_{p(in)}$ 50 ns (min)
Width of Reset Pulse, $t_{p(reset)}$ 50 ns (min)

NOTE: Fan-out from output A to input BD and to 10 additional series T74 loads is permitted.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		Test Figure	TEST CONDITIONS (*)	Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	17	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	18	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	18	V_{CC} = MIN I_{load}=-400μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	17	V_{CC} = MIN I_{sink}=16mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	19	V_{CC} = MAX V_{in} = 2.4V			40	μA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at input A	19	V_{CC} = MAX V_{in} = 2.4V			80	μA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at input BD	19	V_{CC} = MAX V_{in} = 2.4V			160	μA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	20	V_{CC} = MAX V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	20	V_{CC} = MAX V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD	20	V_{CC} = MAX V_{in} = 0.4V			-6.4	mA
I_{OS}	Short-circuit output current (***)	21	V_{CC} = MAX V_{out} = 0	-18		-57	mA
I_{CC}	Supply current	19	V_{CC} = MAX V_{in} = 4.5V		32	53	mA

NOTES :

(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be grounded at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25° C, N = 10)

PARAMETER		Test Figure	TEST CONDITIONS	Min.	Typ.	Max.	Unit
f_{max}	Maximum frequency of input count pulses		C_L = 15pF R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output C	36	C_L = 15pF R_L = 400Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output C	36	C_L = 15pF R_L = 400Ω		60	100	ns

MSI

STANDARD TEMPERATURE RANGE

DESCRIPTION

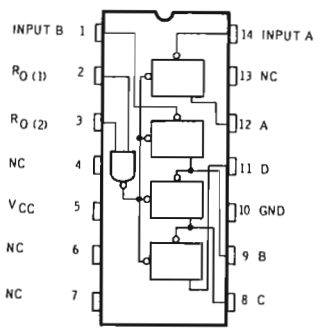
This high-speed, monolithic 4-bit binary counter consists of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0.

As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes :

1) When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table below.

2) When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2,4, and 8 are available at the B, C and D outputs . independent use of flip-flop A is available if the reset function coincides with the reset of the 3-bit ripple-through counter.

CONNECTION DIAGRAM (Top view)



T 7493

TRUTH TABLE (Notes 1, 2 and 3)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES :
1) Output A connected to input B.
2) To reset all outputs to logical 0 both $R_{O(1)}$ and $R_{O(2)}$ inputs must be at a logical 1.
3) Either (or both) reset inputs $R_{O(1)}$ and $R_{O(2)}$ must be at a logical 0 to count.

OPERATING CONDITIONS

Width of Input Count Pulse, $t_{p(in)}$	50 ns (min)
Width of Reset Pulse, $t_{p(reset)}$	50 ns (min)

NOTE : Fan-out from output A to input B and to 10 additional series T 74 loads is permitted.

MSI

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (over recommended free air temperature range unless otherwise noted)

PARAMETER		Test Figure	TEST CONDITIONS (*)	Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	17	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	18	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	18	V_{CC} = MIN I_{load} = -400µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	17	V_{CC} = MIN I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	19	V_{CC} = MAX V_{in} = 2.4V			40	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	19	V_{CC} = MAX V_{in} = 2.4V			80	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	20	V_{CC} = MAX V_{in} = 0.4V			- 1.6	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	20	V_{CC} = MAX V_{in} = 0.4V			- 3.2	mA
I_{OS}	Short-circuit output current (***)	21	V_{CC} = MAX V_{out} = 0	-18		- 57	mA
I_{CC}	Supply current	19	V_{CC} = MAX V_{in} = 4.5V		32	53	mA

NOTES :
(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be grounded at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Figure	TEST CONDITIONS	Min.	Typ.	Max.	Unit
f_{max}	Maximum frequency of input count pulses		C_L = 15pF R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	36	C_L = 15pF R_L = 400 Ω		75	135	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	36	C_L = 15pF R_L = 400 Ω		75	135	ns

MSI

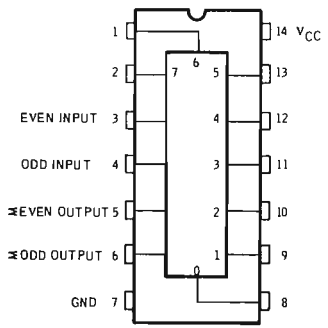
STANDARD TEMPERATURE RANGE

DESCRIPTION

This universal, monolithic, 8-bit parity generator/checker, utilizing familiar Series T74 TTL circuitry, features odd/even outputs and control inputs to facilitate operation in either odd-or even-parity applications. The word-length capability is easily expanded by cascading. Typical applications are shown for this parity circuit being used to generate and check parity.

The T74180 is fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series T74 load. A full fan-out to 10 normalized series T74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized loads is provided in the logical 1 state. Typical power dissipation is 170 mW.

CONNECTION DIAGRAM (Top view)



T 74180

Positive logic : see truth table

TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		Test Figure	TEST CONDITIONS (*)	Min.	Typ(**)	Max.	Unit
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	22	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	22	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	V_{CC} = MIN $V_{in(1)}$ = 2V $V_{in(0)}$=0.8V I_{load} = - 800 µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	22	V_{CC} = MIN $V_{in(1)}$ = 2V, $V_{in(0)}$=0.8V I_{sink} = 16 mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at each data input	23	V_{CC} = MAX V_{in} = 2.4V			40	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at each data input	23	V_{CC} = MAX V_{in} = 0.4V			- 1,6	mA
$I_{in(1)}$	Logical 1 level input current at even or odd input	23	V_{CC} = MAX V_{in} = 2.4V			80	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at even or odd input	23	V_{CC} = MAX V_{in} = 0.4V			- 3.2	mA
I_{OS}	Short circuit output current (***)	24	V_{CC} = MAX	-18		- 55	mA
I_{CC}	Supply current	24 and 25	V_{CC} = MAX		34	56	mA

(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Test Figure	TEST CONDITIONS	Min.	Typ.	Max.	Unit
t_{pd1}	Data	Σ Even	37	C_L = 15pF R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Even	37	C_L = 15pF R_L = 400 Ω		25	38	ns
t_{pd1}	Data	Σ Odd	37	C_L = 15pF R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Odd	37	C_L = 15pF R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Even	37	C_L = 15pF R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Even	37	C_L = 15pF R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Odd	37	C_L = 15pF R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Odd	37	C_L = 15pF R_L = 400 Ω		25	38	ns
t_{pd1}	Even or Odd	Σ Even or Σ Odd	37	C_L = 15pF R_L = 400 Ω		13	20	ns
t_{pd0}	Even or Odd	Σ Even or Σ Odd	37	C_L = 15pF R_L = 400 Ω		7	10	ns

TYPICAL APPLICATIONS

VERIFYING TRANSMITTED DATA

In this example (Figure A), data is being transmitted from data register A to data register B. Parity generators A1 and A2 are connected to generate an even-parity bit Q_{16} which is transmitted to register B. Parity checkers B1 and B2 verify the accuracy of the transmitted data and generate an even true (logical 1) or false (logical 0) parity output signal.

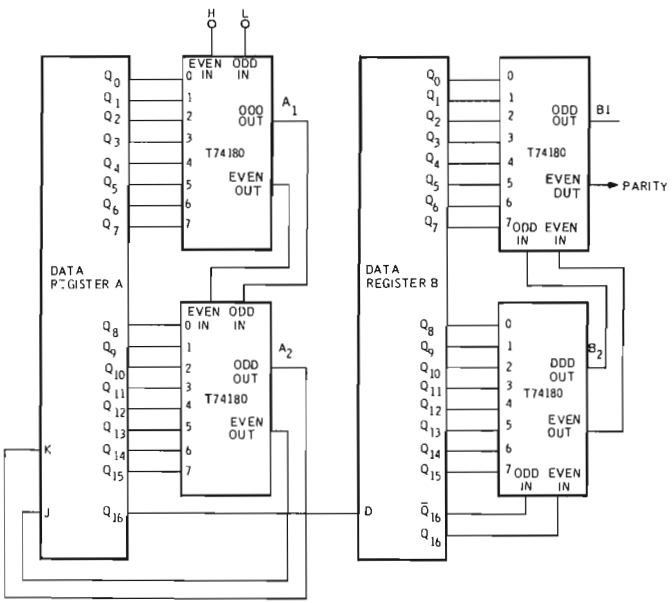


FIG. A

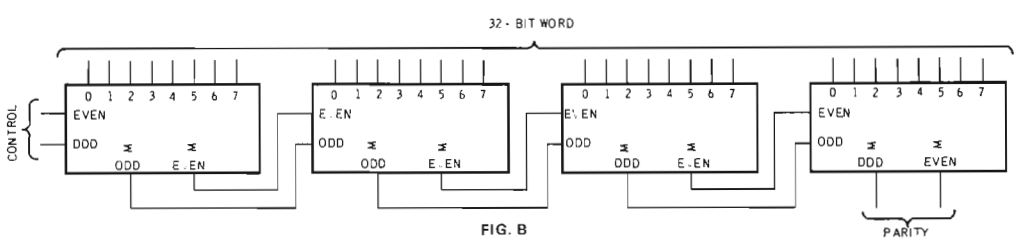


FIG. B

CASCADING FOR LONGER WORD LENGTHS

The parity generator/checker may be cascaded for applications requiring longer word lengths. See Figure B. The ODD IN control is grounded for even parity generation and the EVEN IN control is grounded for odd parity generation. Two control inputs and two outputs ensure faster operation when cascading for word lengths over 8 bits, as only one gate delay is added for each additional 8-bit group. For a 32-bit word, parity can be generated in approximately 65 ns.

D-C TEST CIRCUITS*

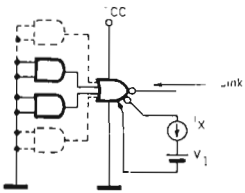


FIG. 1

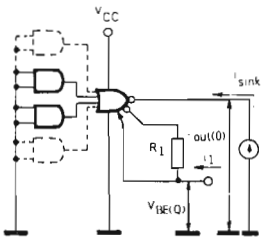


FIG. 2

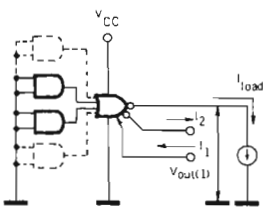


FIG. 3

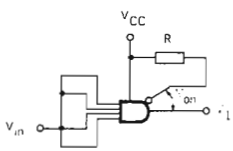


FIG. 4

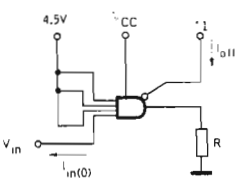


FIG. 5

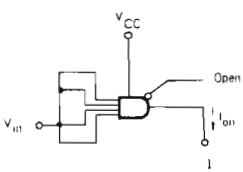
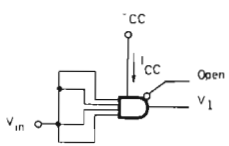


FIG. 6

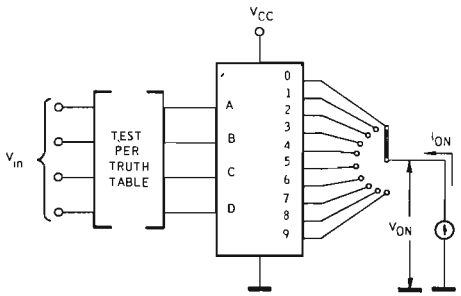


1) "On" and "off" conditions are tested separately
2) Each gate is tested separately.

FIG. 7

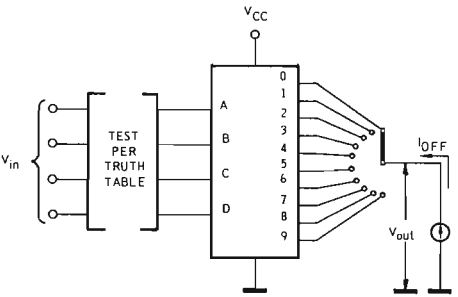
*Arrows indicate actual direction of current flow.

DC TEST CIRCUITS* (contd.)



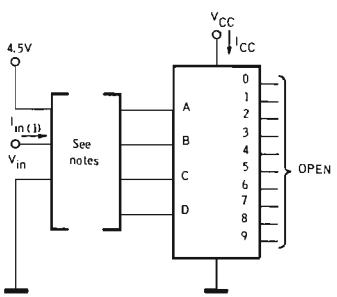
1. Each output is tested separately in the ON state.

FIG. 8



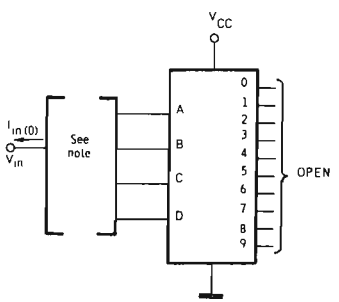
1. Each output is tested separately in the OFF state.

FIG. 9



1. When testing $I_{in(1)}$ each input is tested separately.
2. When testing I_{CC} all outputs are open, inputs A, B, and C are at 4.5V, and input D is grounded.

FIG. 10

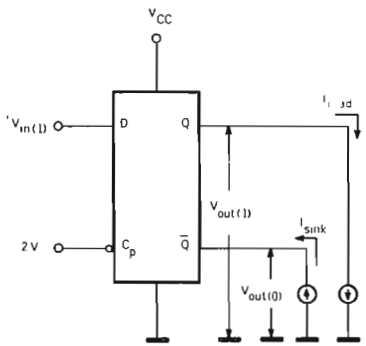


1. Each input is tested separately

FIG. 11

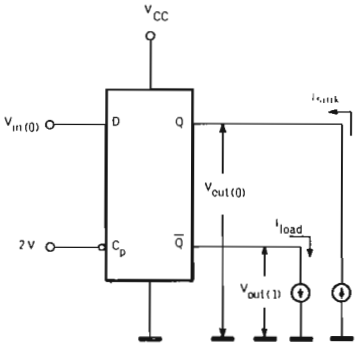
* Arrows indicate actual direction of current flow.

D-C TEST CIRCUITS* (contd.)



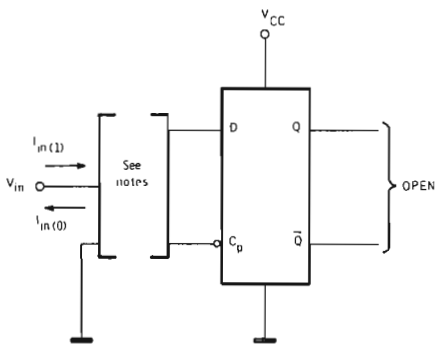
1. Each latch is tested separately.

FIG. 12



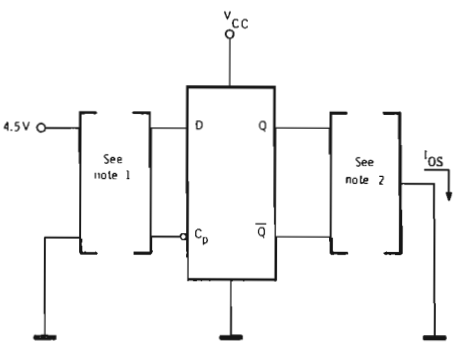
1. Each latch is tested separately.

FIG. 13



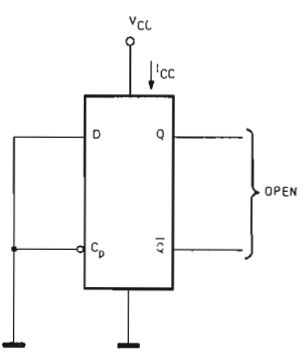
1. Each input is tested separately.
2. When testing $I_{in(1)}$ at D, ground clock.
3. When testing $I_{in(1)}$ at clock, ground all D inputs.

FIG. 14



1. Input conditions are in accordance with truth table.
2. Each latch and each output is tested separately.

FIG. 15

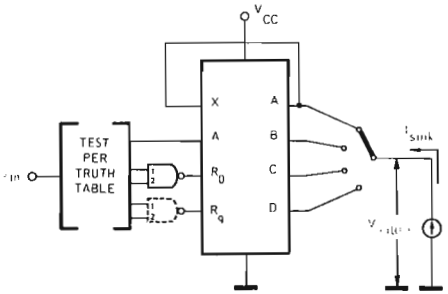


1. All latches are tested simultaneously.

FIG. 16

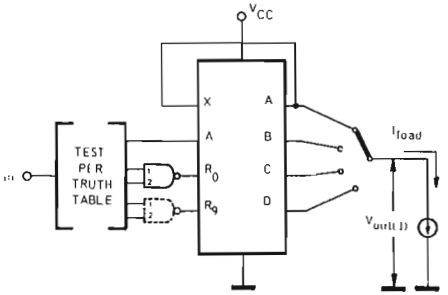
* Arrows indicate actual direction of current flow.

D-C TEST CIRCUITS* (contd.)



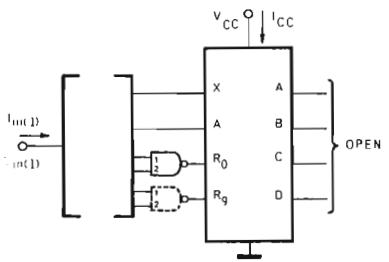
1. Each output is tested in the logical 0 state.

FIG. 17



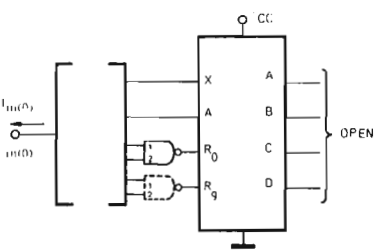
1. Each output is tested in the logical 1 state.

FIG. 18



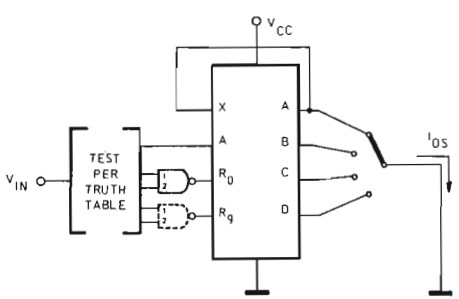
1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ ground $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ ground $R_{0(1)}$ or $R_{9(1)}$.
4. When testing I_{CC} reset all outputs to logical 0, ground all inputs, then measure I_{CC}.

FIG. 19



1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ apply 4.5V to $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ apply 4.5V to $R_{0(1)}$ or $R_{9(1)}$.

FIG. 20



1. Each output is tested in the logical 1 state.

FIG. 21

* – Arrows indicate actual direction of current flow.
– X (pin N° 1) is BD input when testing T7490, B input when testing T7493.
– R_9 (pins N° 6 - N° 7) has to be connected only when testing T7490.

D-C TEST CIRCUITS* (contd.)

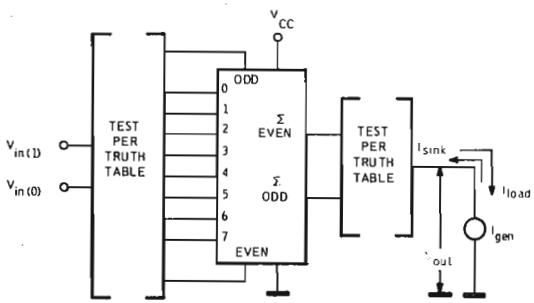
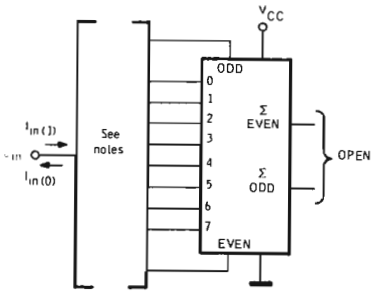
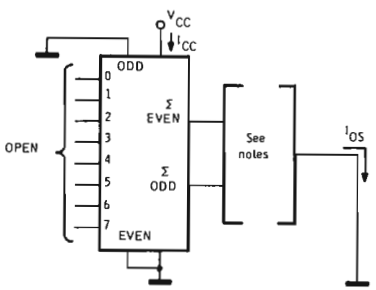


FIG. 22



1. Each input is tested separately.
2. Odd and even inputs are each tested for $I_{in(1)}$ and $I_{in(0)}$ with both an even-code and an odd-code applied at the data inputs.

FIG. 23



1. Each output is tested separately.
2. When testing I_{CC} both outputs are open.

FIG. 24

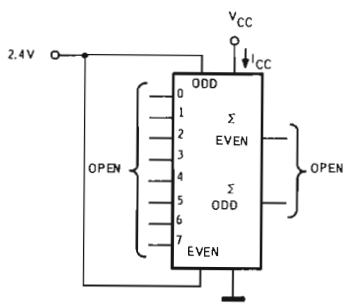


FIG. 25

* Arrows indicate actual direction of current flow.

SWITCHING TIME TEST CIRCUITS

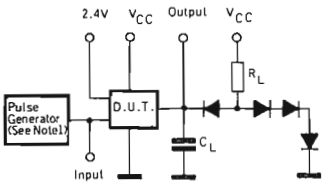


FIG. 26

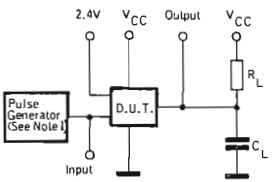


FIG. 27

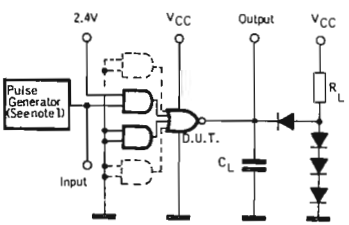


FIG. 28

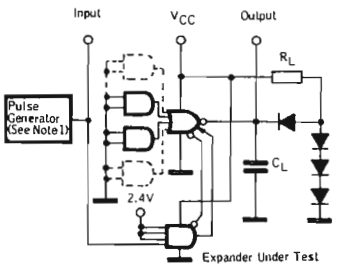
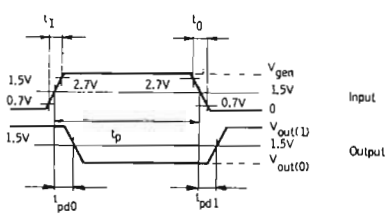


FIG. 29

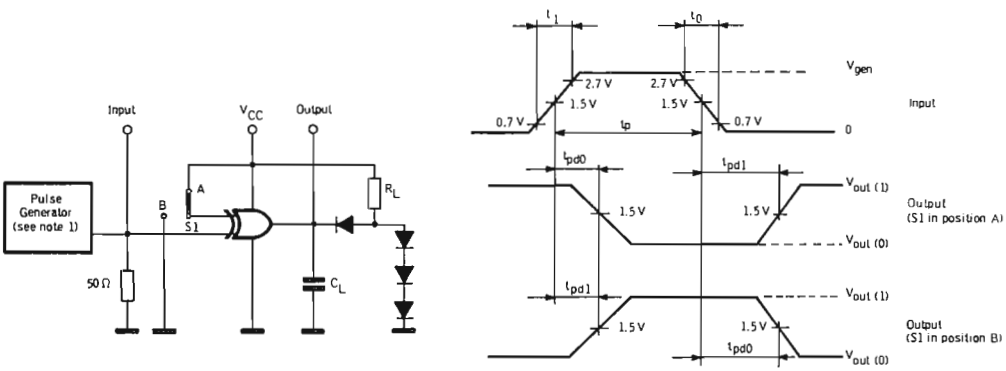
SWITCHING WAVEFORMS FOR FIG. 26 - 27 - 28 - 29



NOTES :

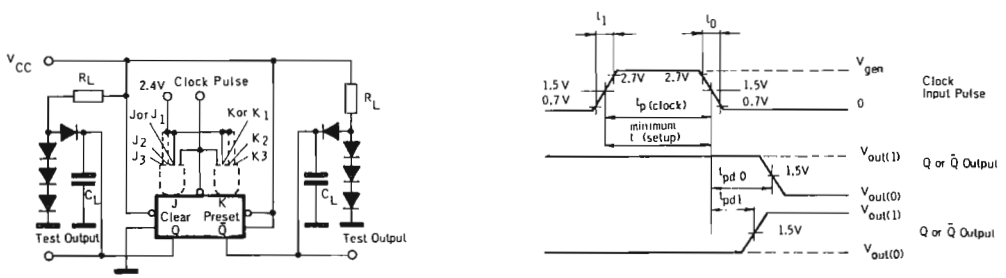
1) The generator has the following characteristics : $V_{gen} = 3.5V$; $t_p = 0.5\ \mu s$; PRR = 1 MHz; $Z_{out} \simeq 50\ \Omega$; $t_o = 5$ ns and $t_1 = 10$ ns (for T 7406 and T7416; to = $t_1 \leqslant 10$ ns.).
2) All diodes are BAY 71.
3) $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$.
4) C_L includes probe and jig capacitance.

SWITCHING TIME TEST CIRCUITS (contd)



NOTES : 1) The generator has the following characteristics; $V_{gen} = 3V$, $t_0 = t_1 \leqslant 15$ ns, $t_p = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \simeq 50\ \Omega$.
2) All diodes are BAY 71. – 3) $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$ – 4) C_L includes probe and Jig capacitance. – 5) Each gate tested separately.

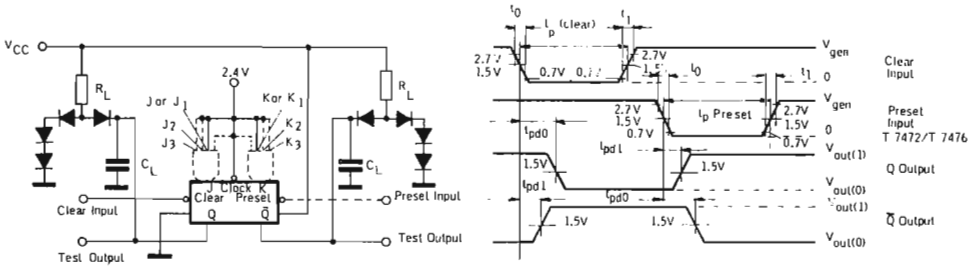
FIG. 30



NOTES : 1) Clock, J and K input pulse characteristics : $V_{gen} = 3.5V$, $t_0 = 5$ ns, $t_1 = 10$ ns, $t_p = 20$ ns, and PRR = 1MHz. When testing f_{clock} vary PRR.
2) For the T7472, $J = J_1 \cdot J_2 \cdot J_3$ and $K = K_1 \cdot K_2 \cdot K_3$.
3) Gates inputs (shown with dotted lines) are for the T7472 only. The T7473, T7476, T74107 dual Flip-Flops have direct J and K inputs and preset is not available on the T 7473 or T74107.
4) All diodes are BAY 71.
5) C_L includes probe and Jig capacitance.

FIG. 31

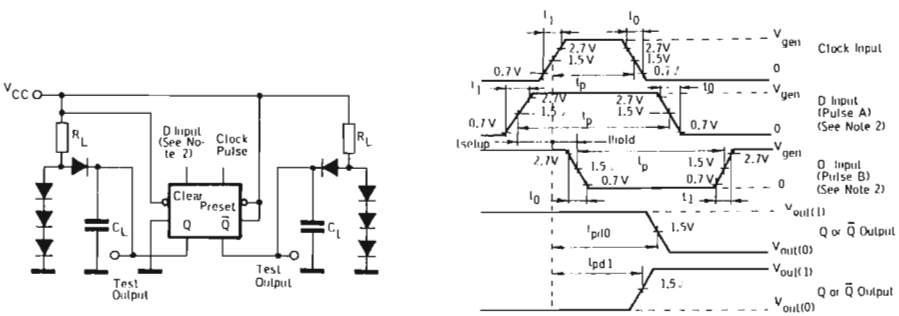
SWITCHING TIME TEST CIRCUITS (contd)



NOTES :

1) Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2) Clear or preset input pulse characteristics: V_{gen} = 3.5V, t_0 = 5ns, t_1 = 10ns, $t_{p(clear)}$ = $t_{p(preset)}$ = 25ns. PRR = 1MHz, and $Z_{out} \simeq 50\,\Omega$.
3) Gates inputs (shown with dotted lines) are for the T7472 only. The T7473, T7476 and T74107, dual Flip-Flops have direct J and K inputs, and preset is not available on the 7473 or 74107.
4) All diodes are BAY71.
5) C_L includes probe and Jig capacitance.

FIG. 32

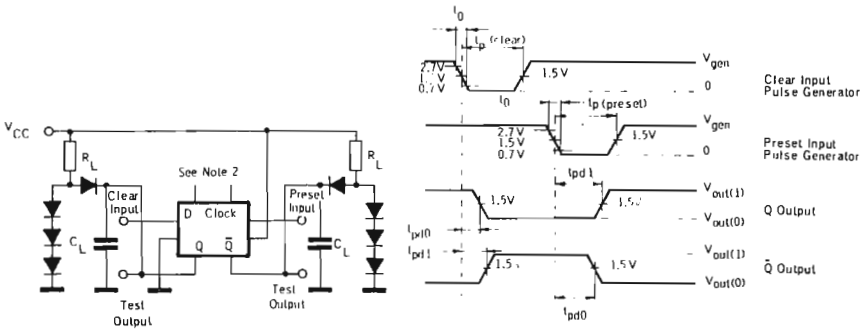


NOTES:

1) Clock input pulse has the following characteristics: V_{gen}=3.5V, t_0=5ns, t_1=10ns, t_p=30ns, and PRR=1 MHz. When testing f_{clock}, vary PRR.
2) D Input (pulse A) has the following characteristics: V_{gen}=3.5V, t_0=5ns, t_1=10ns, t_{setup}=20ns, t_p=60ns, and PRR is 50%of the clock PRR.
   D Input (pulse B) has the following characteristics: V_{gen}=3.5V, t_0=5ns, t_1=10ns, t_{hold}=5ns, t_p=60ns, and PRR is 50%of the clock PRR.
3) All diodes are BAY 71
4) C_L includes probe and Jig capacitance.

FIG. 33

SWITCHING TIME TEST CIRCUIT (contd.)



NOTES :
1) Clear and preset inputs of the T7474 dominate regardless of the state of clock or D inputs. 2) All diodes are BAY 71.
3) C_L includes probe and Jig capacitance. 4) Clear or preset input pulse characteristics : V_{gen} =3.5V, t_0 =5ns, and t_p =30 ns.

FIG. 34

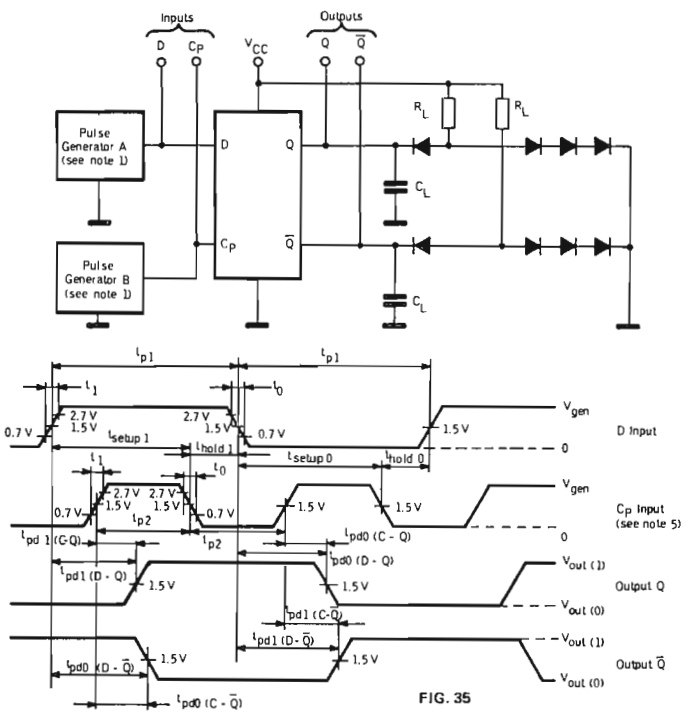
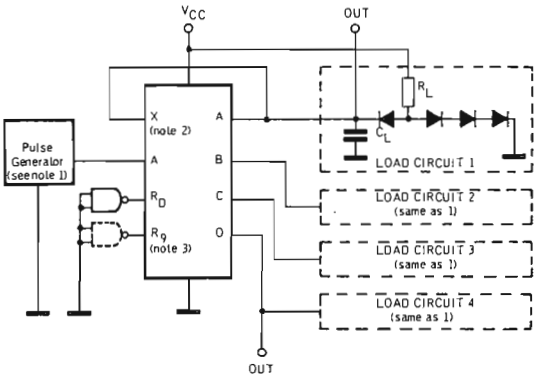


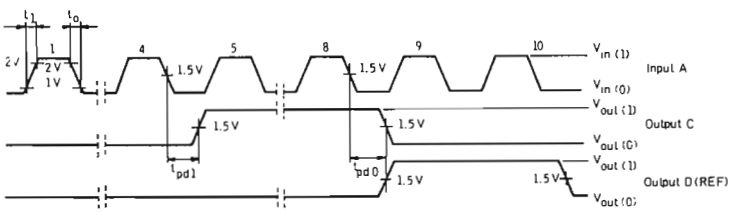
FIG. 35

NOTES : 1) The pulse generators have the following characteristics : V_{gen} = 3V, $t_1 = t_0 \leq 10$ ns, and $Z_{out} \simeq 50\ \Omega$. For pulse generator A t_{p1} =1µs and PRR = 500 kHz. For pulse generator B, t_{p2} = 500 ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.
2) Each latch is tested separately.
3) C_L includes probe and jig capacitance.
4) All diodes are BAY 71.
5) When measuring t_{pd1} (D-Q) and t_{pd0} (D-Q) or t_{pd0} (D-$\bar{Q}$) and t_{pd1} (D-$\bar{Q}$), clock input must be held at logical 1.

SWITCHING TIME TEST CIRCUITS (contd.)



SWITCHING WAVEFORMS FOR T 7490



SWITCHING WAVEFORMS FOR T 7493

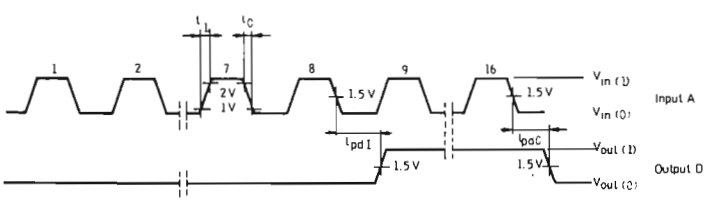


FIG. 36

NOTES :

1) The pulse generator has the following characteristics: $V_{gen} = 3V$; $t_0 = t_1 \leq 15ns$, $t_p = 0.5\,\mu s$, PRR = 1 MHz, $Z_{out} \simeq 50\Omega$

2) X (pin N. 1) is BD input when testing T7490, B input when testing T7493

3) R_9 (pins N. 6 – N. 7) has to be connected only when testing T7490.

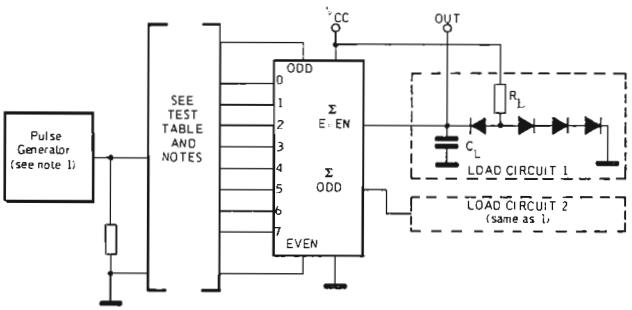
4) All diodes are BAY71

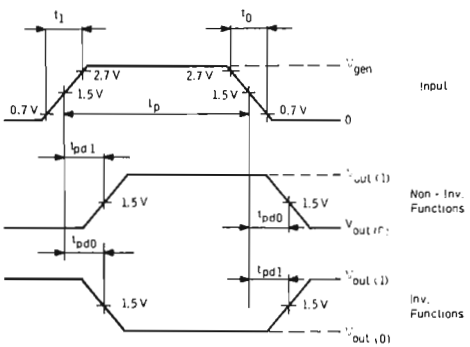
5) C_L includes probe and Jig capacitance

6) $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$

7) Voltage values are with respect to ground terminal.

SWITCHING TIME TEST CIRCUITS (contd)





TEST TABLE

INPUT CONDITIONS		OUTPUT TESTED
PULSE	GND	
0	ODD	Σ EVEN
1	ODD	Σ EVEN
2	ODD	Σ EVEN
3	ODD	Σ EVEN
4	ODD	Σ EVEN
5	ODD	Σ EVEN
6	ODD	Σ EVEN
7	ODD	Σ EVEN
0	ODD	Σ ODD
1	ODD	Σ ODD
2	ODD	Σ ODD
3	ODD	Σ ODD
4	ODD	Σ ODD
5	ODD	Σ ODD
6	ODD	Σ ODD
7	ODD	Σ ODD
EVEN	NONE	Σ EVEN
ODD	0	Σ EVEN
EVEN	0	Σ ODD
ODD	NONE	Σ ODD

NOTES :

1) The pulse generator has the following characteristics:
   V_{gen} = 3V, $t_1 = t_0$ = 10 ns, t_p = 500 ns,
   PRR = 1 MHz, and $Z_{out} \simeq 50\,\Omega$.
2) Inputs not specified are open.
3) C_L includes probe and Jig capacitance.
4) All diodes are BAY 71.

FIG. 37

TTL INTEGRATED CIRCUITS

T 7407
T 7417

HEX BUFFERS/DRIVERS HIGH VOLTAGE OUTPUTS

- HIGH SINK-CURRENT CAPABILITY
- CONVERTS TTL VOLTAGE LEVELS to MOS LEVELS
- INPUT CLAMPING DIODES
- TYPICAL POWER DISSIPATION: 145 mW

These monolithic TTL hex inverter buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS) or for driving high-current loads (such as lamps or relays) and are also characterized for use as inverter buffers for driving TTL inputs.
Available in standard temperature range (0 to 70°C) they come in 14-lead dual in-line plastic package similar to Jedec TO-116.

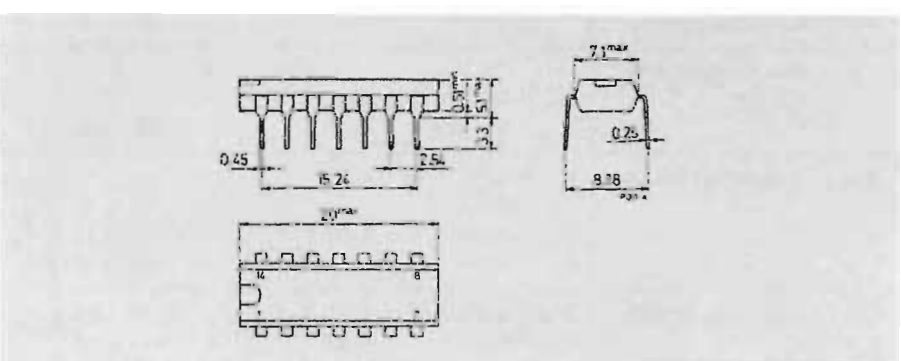
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage		7	V
V_i	Input voltage		5.5	V
V_o	Output voltage	for T **7407**	30	V
		for T **7417**	15	V
T_{op}	Operating temperature		0 to 70	°C
T_{stg}	Storage temperature		-65 to 150	°C

ORDERING NUMBERS : T 7407 B1, T 7417 B1

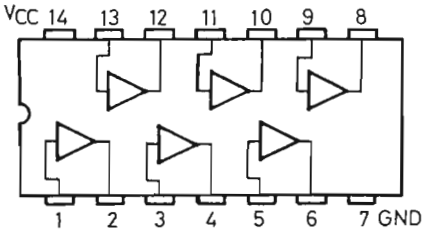
MECHANICAL DATA

Dimensions in mm



T 7407
T 7417

CONNECTION DIAGRAM



S-0241

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
V_o	Output voltage for T **7407**	max 30	V
	for T **7417**	max 15	V
I_{OL}	Output low current	max 40	mA
T_{op}	Operating temperature	0 to 70	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min. Typ.* Max.	Unit	Fig.
V_{IH}	Input high voltage		2	V	1
V_{IL}	Input low voltage		0.8	V	2
I_{CEX}	Output leakage current	V_{CC}= 4.75V V_i = 2V V_{OH}= V_o max	250	μA	1
V_{OL}	Output low voltage	V_{CC}= 4.75V V_i = 0.8V I_{OL}= 40mA	0.7	V	2
		V_{CC}= 4.75V V_i= 0.8V I_{OL}= 16mA	0.4	V	
I_{IH}	Input high current	V_{CC}= 5.25V V_i = 2.4V	40	μA	3
		V_{CC}= 5.25V V_i = 5.5V	1	mA	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.*	Max.	Unit	Fig.
I_{IL}	Input low current	V_{CC} = 5.25V V_i = 0.4V			-1.6	mA	3
I_{CCH}	Supply current at high-level output	V_{CC} = 5.25V V_i = 5V		29	41	mA	4
I_{CCL}	Supply current at low-level output	V_{CC} = 5.25V V_i = 0V		21	30	mA	4

* All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15 pF R_L = 110 Ω		20	30	ns	5
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15 pF R_L = 110 Ω		6	10	ns	5

DC TEST CIRCUITS (Arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{IH}, I_{CEX}

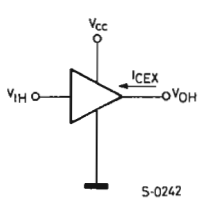
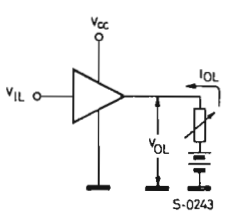


Fig. 2 - V_{IL}, V_{OL}



DC TEST CIRCUITS (continued)

Fig. 3 - I_{IH}, I_{IL}

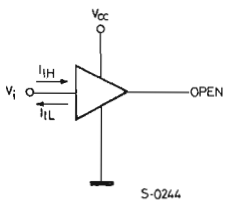
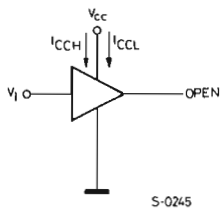


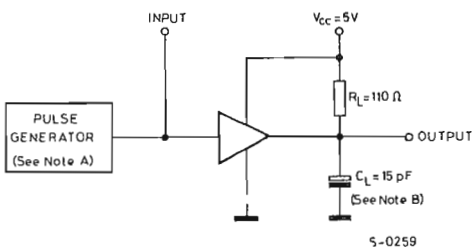
Fig. 4 - I_{CCH}, I_{CCL}



All buffers/drivers are tested simultaneously

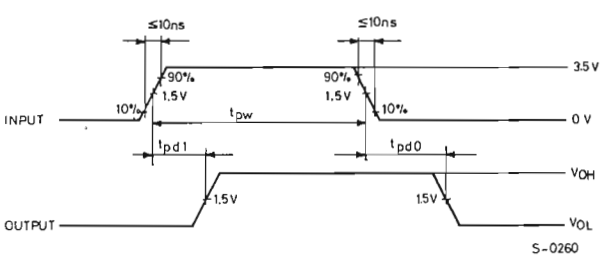
SWITCHING TIMES

Test circuit



NOTES: A. The generator has the following characteristics: $t_{pw} = 0.5\,\mu s$, PRR = 1 MHz, $Z_{out} \approx 50\Omega$
B. C_L includes probe and jig capacitance.

Waveforms



T 7408
T 7409

QUAD 2-INPUT POSITIVE "AND" GATES

- TOTEM-POLE OUTPUTS (T 7408 only)
- OPEN COLLECTOR OUTPUTS (T 7409 only)
- DIODE-CLAMPED INPUTS
- NORMALIZED FAN-OUT OF 10
- 14-PIN PLASTIC DIP

The T 7408 and T 7409 are monolithic quad two input AND gates in a 14-lead dual in-line plastic package similar to Jedec TO-116.
The T 7408, with totem-pole outputs, drives 10 normalized Series 74 loads. The T 7409, with open-collector outputs, provides additional logic flexibility, as the outputs may be wire-AND connected to extend the AND function. They are available in the standard temperature range (0 to +70 °C).

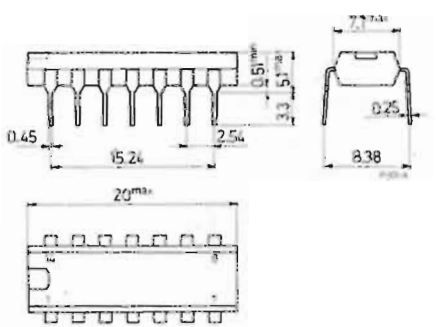
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
V_{IE}	Interemitter voltage	5.5	V
V_{OH}	Output high voltage (T 7409 only)	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBERS: T 7408 B1, T 7409 B1.

MECHANICAL DATA

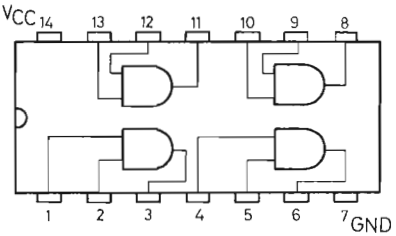
Dimensions in mm



similar to **TO-116**

T 7408
T 7409

CONNECTION DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
N	Normalized fan-out from each output	max 10	—
T_{op}	Operating temperature	0 to 70	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.*	Max.	Unit	Fig.
V_{IH}	Input high voltage		2			V	1
V_{IL}	Input low voltage				0.8	V	2
V_{OH}	Output high voltage (for T 7408 only)	V_{CC} = 4.75 V V_{IN} = 2 V I_{OH} = -800µA	2.4			V	1
V_{OL}	Output low voltage	V_{CC} = 4.75 V V_{IN} = 0.8 V I_{OL} = 16 mA			0.4	V	2
I_{IH}	Input high current (each input)	V_{CC} = 5.25 V V_{IN} = 2.4 V V_{CC} = 5.25 V V_{IN} = 5.5 V			40 1	µA mA	3
I_{IL}	Input low current (each input)	V_{CC} = 5.25 V V_{IN} = 0.4 V			-1.6	mA	4
I_{CEX}	Output leakage current (for T 7409 only)	V_{CC} = 4.75 V V_{IN} = 2 V V_{OH} = 5.5 V			250	µA	1
I_{SC}**	Short-circuit output current (for T 7408 only)	V_{CC} = 5.25 V	-18		-55	mA	5

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.*	Max.	Unit	Fig.
I_{CCL}	Supply current, low level output	$V_{CC} = 5.25$ V $V_{IN} = 0$		20	33	mA	6
I_{CCH}	Supply current, high level output	$V_{CC} = 5.25$ V $V_{IN} = 5$ V		11	21	mA	6

* All typical values are at $V_{CC} = 5$ V, $T_{amb} = 25$ °C.

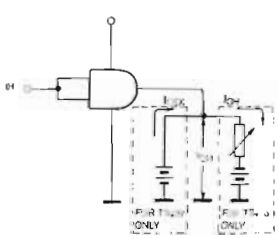
** Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC} = 5$ V, $T_{amb} = 25$ °C, N = 10)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
t_{pd0}	Propagation delay time to logical 0 level	$C_L = 15$ pF $R_L = 400\ \Omega$					
		for **T 7408**		12	19	ns	7-8
		for **T 7409**		16	24	ns	
t_{pd1}	Propagation delay time to logical 1 level	$C_L = 15$ pF $R_L = 400\ \Omega$					
		for **T 7408**		17.5	27	ns	7-8
		for **T 7409**		21	32	ns	

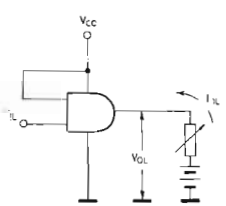
DC TEST CIRCUITS (Arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{IH}, V_{OH}, I_{CEX}



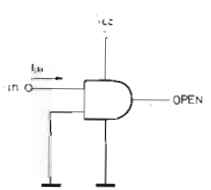
Both inputs are tested simultaneously.

Fig. 2 - V_{IL}, V_{OL}



Each input is tested separately.

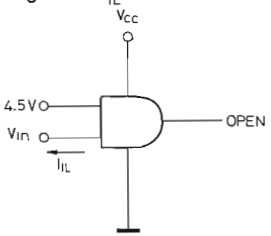
Fig. 3 - I_{IH}



Each input is tested separately.

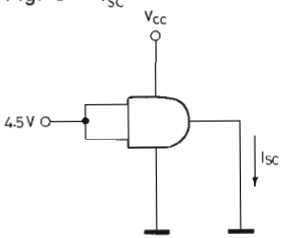
DC TEST CIRCUITS (continued)

Fig. 4 - I_{IL}



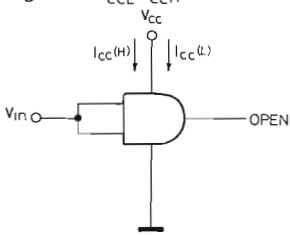
Each input is tested separately.

Fig. 5 - I_{SC}



Each gate is tested separately.

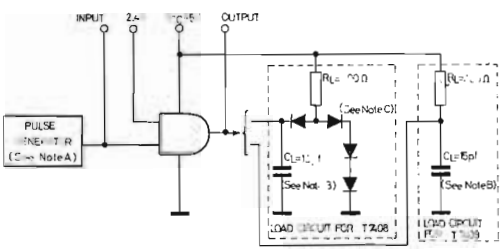
Fig. 6 - I_{CCL}, I_{CCH}



High level and low-level conditions are tested. All gates are tested simultaneously.

SWITCHING TIMES

Fig. 7 - Test circuit



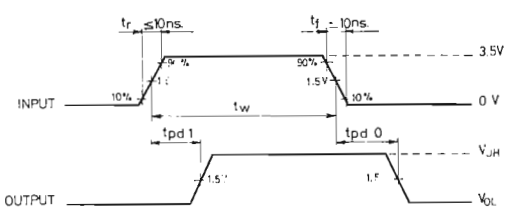
NOTES:

A) The generator has following characteristics: $t_{pw} = 0.5\ \mu s$; PRR = 1 MHz; $Z_{out} \approx 50\ \Omega$

B) C_L includes probe and jig capacitance

C) All diodes are 1N3064

Fig. 8 - Waveforms



Quad 2-input high-voltage interface NAND gate

STANDARD TEMPERATURE RANGE
0°C to 70°C

- OPEN COLLECTOR OUTPUT
- HIGH BREAKDOWN OUTPUT VOLTAGE
- TYPICAL APPLICATION AS DRIVER FOR LOW-THRESHOLD-VOLTAGE MOS INPUTS
- 14-PIN PLASTIC DIP

ORDERING NUMBER
T 7426 BI

This open-collector NAND gate features high output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12V systems. Although the output is rated to withstand 15V, the V_{CC} terminal is connected to the standard 5V source. The output transistor will sink 16mA while maintaining a low-level output voltage of 0.4V maximum, thus providing a high-fan-out driver with the nominal power dissipation of standard series T74 gates.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

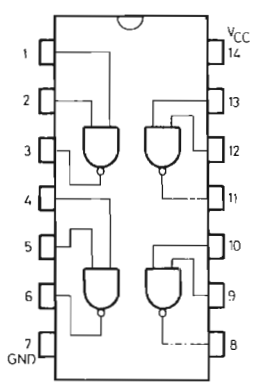
Supply Voltage V_{CC} (1)	7V
Input Voltage (1 and 2)	5.5V
Output Voltage (1 and 3)	15V
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

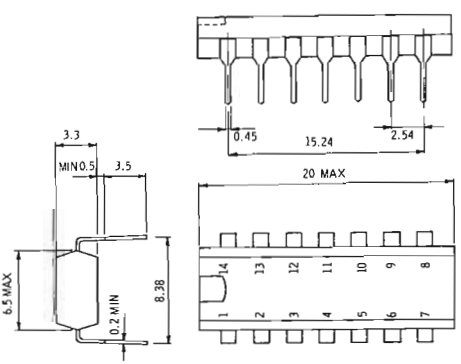
Supply Voltage V_{CC} (1)	4.75V to 5.25V
Maximum Voltage on any Output (1)	12V
Free-Air Temperature Range	0°C to 70°C

Notes : see next page.

CONNECTION DIAGRAM



PHYSICAL DIMENSIONS
14-pin plastic DIP



Note all dimensions in mm.

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

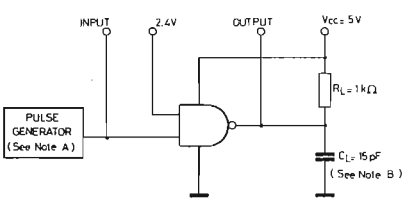
	PARAMETER	TEST CONDITIONS (*)	Min.	Typ (**)	Max.	Unit
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	V_{CC} =MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	V_{CC}=MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} =MIN V_{in}=0.8V I_{load}=1mA	15			V
I_{off}	Off-state reverse current	V_{CC}=MIN V_{in}=0.8V $V_{out(1)}$=12V			50	µA
$V_{out(0)}$	Logical 0 output voltage	V_{CC}=MIN V_{in}=2V I_{sink}=16mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC}=MAX V_{in}=0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC}=MAX V_{in}=2.4V V_{CC}=MAX V_{in}=5.5V			40 1	µA mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC}=MAX V_{in}=5V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC}=MAX V_{in}=0		4	8	mA

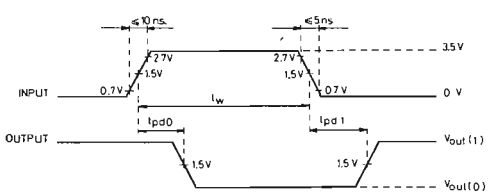
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_A=25°C, N = 10)

	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	Unit
t_{pd0}	Propagation delay time to logical 0 level	C_L=15pF R_L=1KΩ		11	17	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L=15pF R_L=1KΩ		16	24	ns

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC}=5V, T_A=25°C.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





Notes : A. The generator has the following characteristics: t_w = 0.5µs, PRR = 1MHz, Z_{out} ≈50Ω
B. C_L includes probe and jig capacitance

NOTES :
1) Voltage values are with respect to network ground terminal.
2) Input signals must be zero or positive with respect to network ground terminal.
3) This is the maximum voltage which should be applied to any output when it is in the off state.

TTL INTEGRATED CIRCUITS

T 7428
T 7433

PRELIMINARY DATA

QUAD 2 - INPUT NOR BUFFER

- ACTIVE PULL-UP OUTPUT (for **T7428**)
- OPEN COLLECTOR OUTPUT (for **T7433**)
- TTL-DTL COMPATIBILITY
- TYPICAL DISSIPATION of 112 mW
- HIGH FAN-OUT (N = 30)

These positive NOR buffers are functionally identical to T7402 but are designed to drive high capacitive loads with significantly improved dynamic performance.
The devices are directly applicable for use as clock drivers where the distributed capacitive load is relatively large.
Available in standard temperature range (0 to 70°C) they come in 14-lead dual in-line plastic package similar to Jedec TO-116.

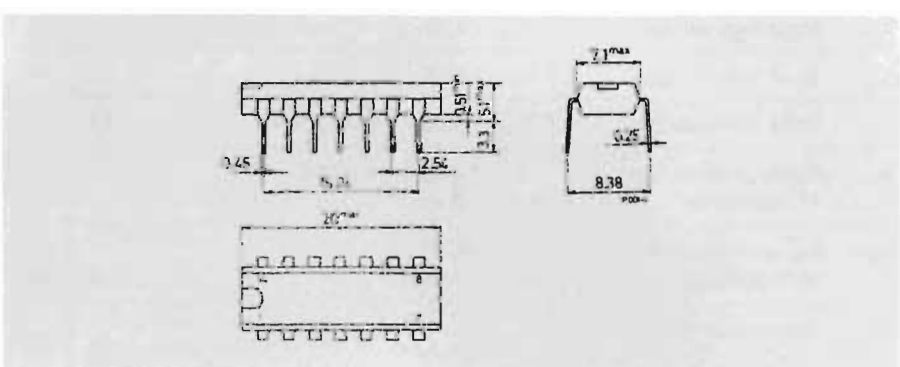
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
V_o	Output voltage (T **7433** only)	5.5	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

ORDERING NUMBERS: T 7428 B1, T 7433 B1

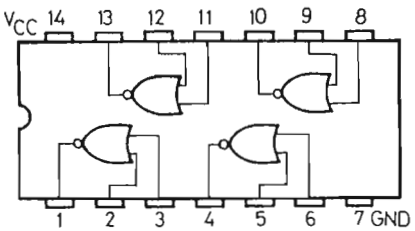
MECHANICAL DATA

Dimensions in mm



T 7428
T 7433

CONNECTION DIAGRAM



S-0238

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage for **T 7428**	4.75 to 5.25	V
	for **T 7433**	4.5 to 5.5	V
N	Normalized fan-out from each output	max 30	–
T_{op}	Operating temperature	0 to 70	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min. Typ.* Max.	Unit
V_{IH}	Input high voltage	V_{CC} = 4.75	2	V
V_{IL}	Input low voltage	V_{CC} = 4.75	0.8	V
V_i	Input clamp voltage	V_{CC} = 4.75 I_I = 12 mA	-1.5	V
V_{OH}	Output high voltage (**T 7428** only)	V_{CC} = 4.75 V_i = 0.8V I_{OH} = -2.4mA	2.4	V
I_{OH}	Output high current (**T 7433** only)	V_{CC} = 4.75 V_i = 0.8V V_{OH} = 5.5V	250	μA
V_{OL}	Output low voltage	V_{CC} = 4.75 V_i = 2V I_{OL} = 48mA	0.4	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.*	Max.	Unit
I_{IH}	Input high current	V_{CC} = 5.25	V_i = 2.4V			40	μA
		V_{CC} = 5.25	V_i = 5.5V			1	mA
I_{IL}	Input low current	V_{CC} = 5.25	V_i = 0.4V			-1.6	mA
I_{SC}**	Short circuit output current (**T 7428** only)	V_{CC} = 5.25		-70		-180	mA
I_{CCH}***	Power dissipation current, high level output	V_{CC} = 5.25			12	21	mA
I_{CCL}****	Power dissipation current, low level output	V_{CC} = 5.25			33	57	mA

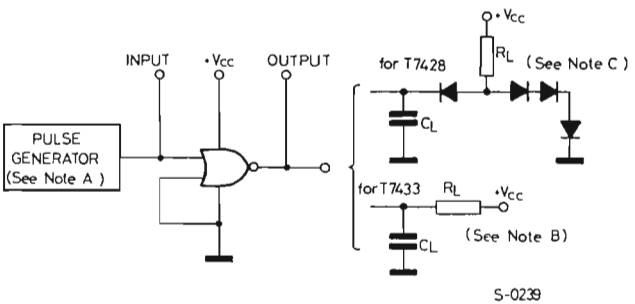
NOTES: * All typical values are at V_{CC} = 5V, T_{amb} = 25°C
** Only one output shorted at a time.
*** It is measured with all inputs grounded and outputs open.
**** It is measured with one input of each gate at 5V, the remaining are grounded; all the outputs open.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C, N = 30)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
t_{pd1}	Propagation delay time to logical 1	C_L = 150 pF	R_L = 133Ω				
			for **T 7428**		10	15	ns
			for **T 7433**		15	22	ns
t_{pd0}	Propagation delay time to logical 0	C_L = 150 pF	R_L = 133Ω				
			for **T 7428**		12	18	ns
			for **T 7433**		16	24	ns

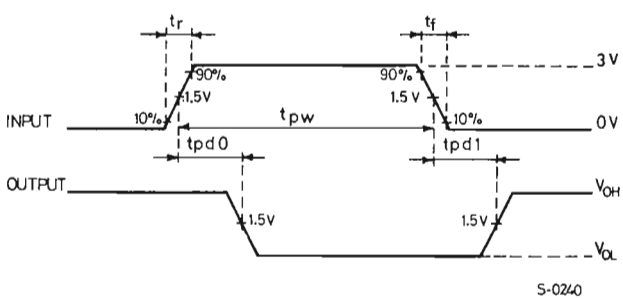
SWITCHING TIMES

Test circuit



NOTES: A. The generator has the following characteristics: t_{pw} = 0.5 μs, PRR = 1 MHz $t_r = t_f \leqslant 10$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N 3064.

Waveforms



4-LINE-TO-10-LINE DECODERS (1 - OF - 10)

- TYPICAL DC NOISE IMMUNITY OF 1 V
- TYPICAL POWER DISSIPATION OF 140 mW
- DIODE-CLAMPED INPUTS
- NORMALIZED FAN-OUT OF 10
- 16-PIN DUAL IN-LINE PLASTIC PACKAGE

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. The T7442 BCD-to-decimal, T7443 excess-3-to-decimal, and T7444 excess-3-gray-to-decimal decoders feature familiar transistor-transistor-logic circuits with inputs and outputs which are compatible with other TTL and DTL circuits. Available in the standard temperature range (0 to 70°C), they come in 16-pin dual in-line plastic package.

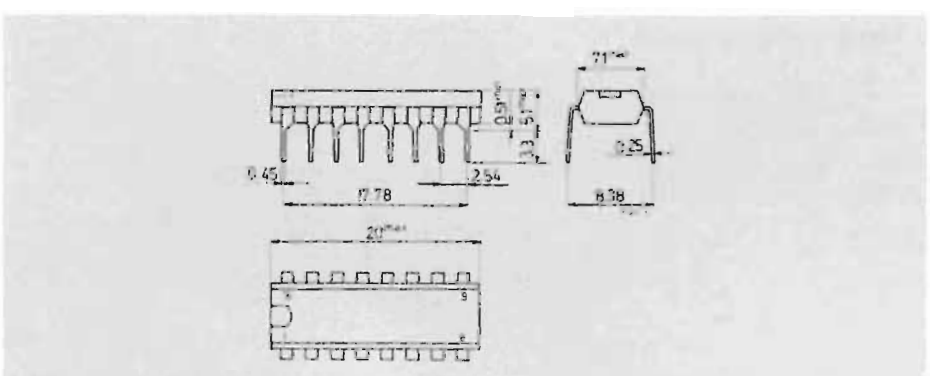
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBERS : T 7442 B1, T 7443 B1, T 7444 B1

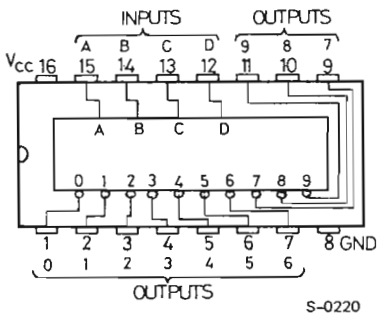
MECHANICAL DATA

Dimensions in mm



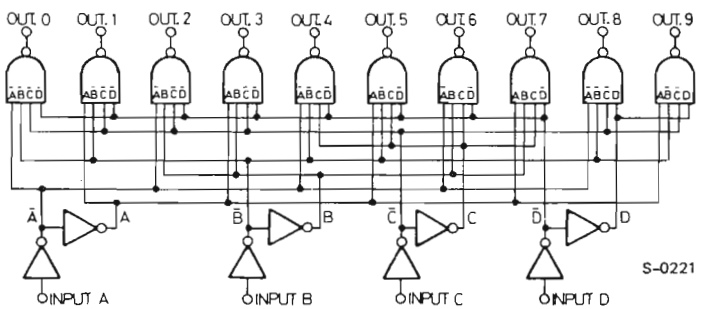
T7442
T7443
T7444

CONNECTION DIAGRAM

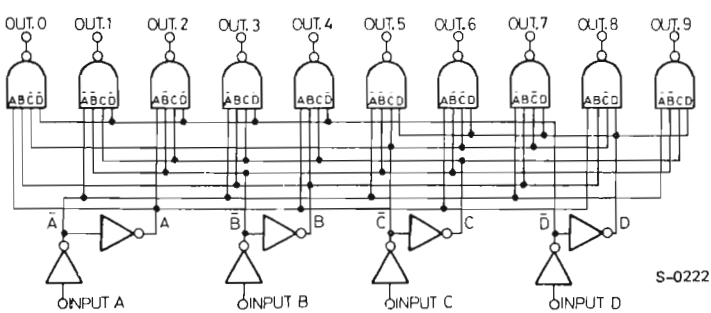


FUNCTIONAL LOGIC DIAGRAMS

T7442 BCD-to-decimal

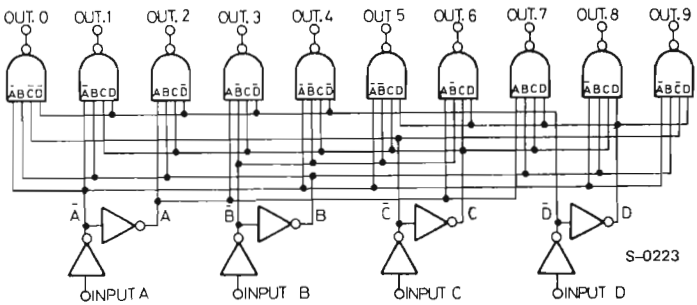


T 7443 Excess-3-to-decimal



FUNCTIONAL LOGIC DIAGRAMS (continued)

T 7444 Excess-3-gray-to-decimal



TRUTH TABLES

T7442 INPUT				T7443 INPUT				T7444 INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
N	Normalized fan-out from each output	max 10	–
T_{op}	Operating temperature	0 to 70	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.*	Max.	Unit	Fig.
V_{IH}	Input high voltage		2			V	1-2
V_{IL}	Input low voltage				0.8	V	1-2
V_{OH}	Output high voltage	V_{CC} = 4.75V V_{IH} = 2V V_{IL} = 0.8V I_{OH} = -400 µA	2.4			V	2
V_{OL}	Output low voltage	V_{CC} = 4.75V V_{IH} = 2V V_{IL} = 0.8V I_{OL} = 16mA			0.4	V	1
I_{IH}	Input high current (each input)	V_{CC} = 5.25V V_i = 2.4V V_{CC} = 5.25V V_i = 5.5V			40 1	µA mA	3
I_{IL}	Input low current (each input)	V_{CC} = 5.25V V_i = 0.4V			-1.6	mA	3
I_{SC}**	Short-circuit output current	V_{CC} = 5.25V	-18		- 55	mA	4
I_{CC}	Supply current	V_{CC} = 5.25V		28	56	mA	3

* All typical values are at V_{CC} = 5V, T_{amb} = 25°C

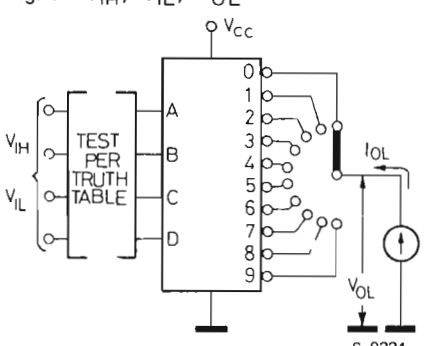
** Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_{amb} = 25°C, N = 10)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	C_L = 15 pF R_L = 400Ω	10	22	30	ns	5-6
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	C_L = 15 pF R_L = 400Ω		23	35	ns	5-6
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	C_L = 15 pF R_L = 400Ω	10	17	25	ns	5-6
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	C_L = 15 pF R_L = 400Ω		26	35	ns	5-6

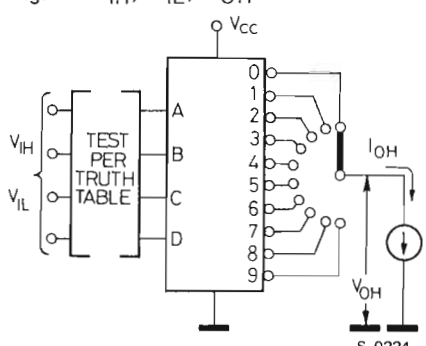
DC TEST CIRCUITS (Arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{IH}, V_{IL}, V_{OL}



Each output is tested separately.

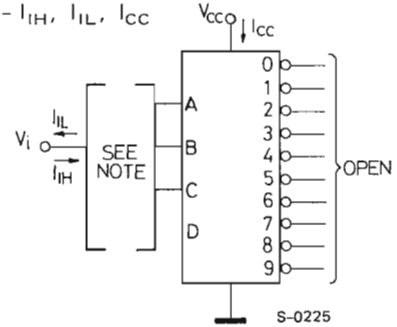
Fig. 2 – V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

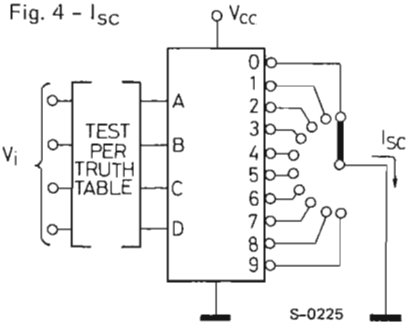
DC TEST CIRCUITS (continued)

Fig. 3 - I_{IH}, I_{IL}, I_{CC}



When testing I_{IH}, I_{IL} each input is tested separately.
When testing I_{CC} all inputs are grounded and outputs are open.

Fig. 4 - I_{SC}



Each output is tested separately

SWITCHING TIMES

Fig. 5 - Test circuit

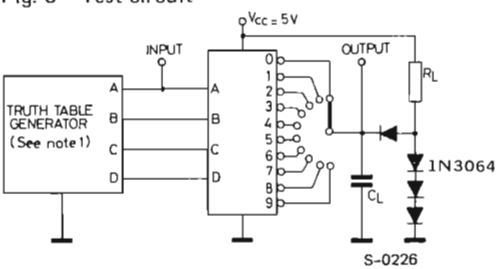
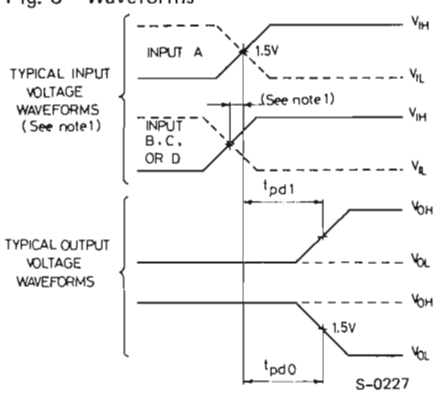


Fig. 6 - Waveforms



Notes :

1. The truth table generator has the following characteristics: $V_{OH} \geq 2.4$ V, $V_{OL} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Input B, C, and D transitions occur simultaneously with or prior to input A transitions.
2. C_L includes probe and jig capacitance.

T 7481
T 7484

16 - BIT RANDOM ACCESS MEMORY

- WIRED-OR OUTPUT for WORD EXPANSION
- TYPICAL NOISE IMMUNITY of 1V
- DTL-TTL COMPATIBILITY

These 16-bit random access memories are monolithic, high-speed, transistor-transistor-logic (TTL) array of 16 flip-flops and two write amplifiers interconnected to from a "scratch-pad" memory with direct-address and non-destructive read-out. A number of active element memories may be paralleled to from the desired matrix size (number of words) and to form the desired word length (number of bits). Available in standard temperature range (0 to 70°C), they come in 14-lead dual in-line plastic package similar to Jedec TO - 116 (T 7481 only) and 16-lead dual in-line plastic package (T 7484 only).

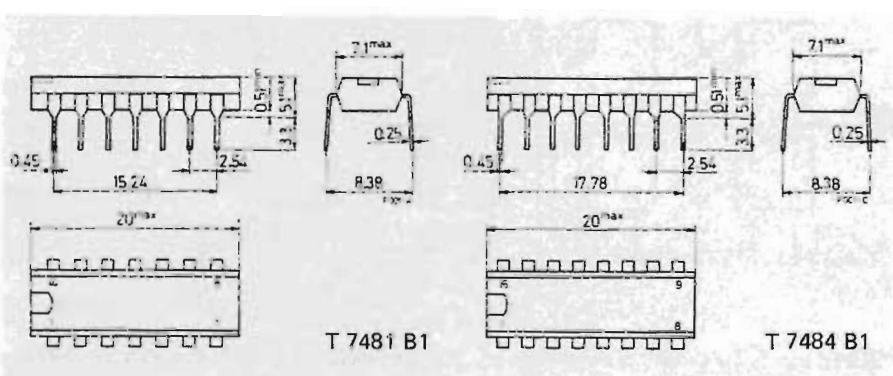
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
T_{stg}	Storage temperature	- 65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

ORDERING NUMBERS : T 7481 B1, T 7484 B1

MECHANICAL DATA

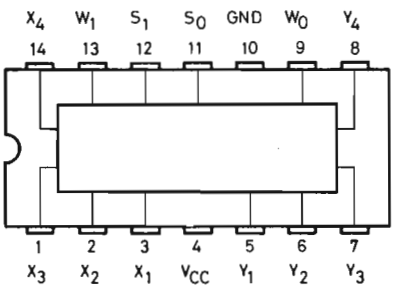
Dimensions in mm



T 7481
T 7484

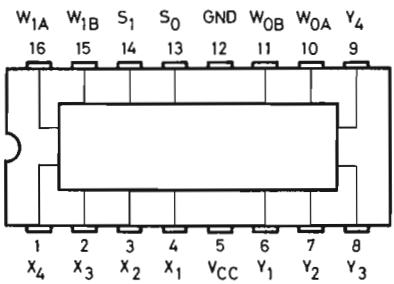
CONNECTION DIAGRAMS

For **T 7481** type



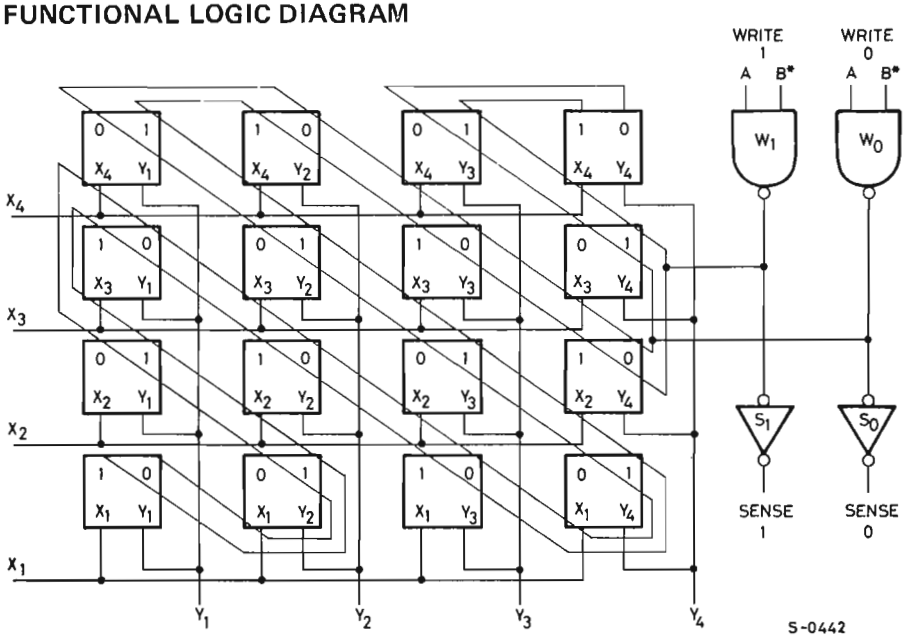
S 0418

For **T 7484** type



S-0417

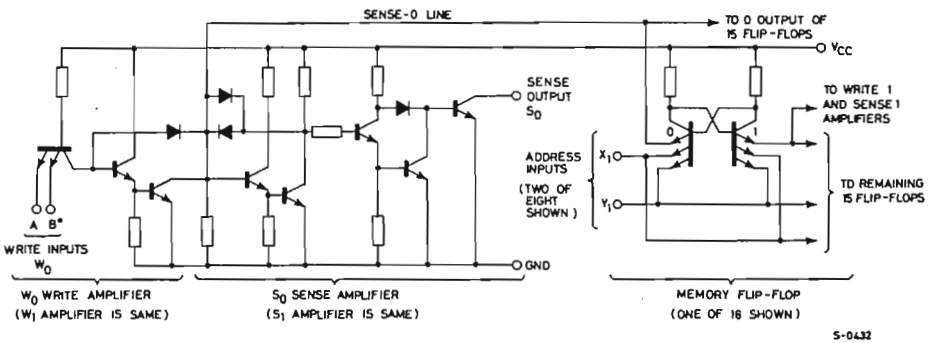
FUNCTIONAL LOGIC DIAGRAM



S-0442

* Gated inputs (as shown) are available on T 7484 only. The T 7481 has one W_0 and one W_1 input.

SCHEMATIC DIAGRAM



* Gated inputs (as shown) are available on T 7484 only. The T 7481 has one W_0 and one W_1 input.

FUNCTIONAL DESCRIPTION

The memory cell consists of 16 flip-flops arranged in a 4-by-4 matrix with each flip-flop representing one bit of 16 words. Four X-address lines and four Y-address lines permit the address of one bit at a time. Each flip-flop, composed of two cross-coupled 3-emitter transistors, is used to store one bit. To determine if a logical 1 or 0 has been stored, it is necessary to know which one of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logical 1 sensing outputs are connected to the sense logical 1 (S_1) amplifier input and all 16 of the logical 0 sensing outputs are connected to the sense logical 0 (S_0) amplifier input. The two remaining emitters on each transistor are used to complete the matrix connections necessary for the X-and Y-address lines. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a logical 0 level and no change will occur on those flip-flops. The desired bit location is selected by raising the coincident X-Y address lines to a logical "H" level and holding the non-selected address lines at logical "L" level. As many as four locations may be addressed simultaneously without destroying stored information. The stored data and its complement at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the S_1 output will be LOW and the S_0 output will be HIGH. If the addressed bit location contains a "0", the S_1 output will be HIGH and the S_0 output will be LOW.

FUNCTIONAL DESCRIPTION (continued)

The memory is non-destructive as the states of the flip-flops are not disturbed during sensing. The memory is volatile and information will be lost if the supply voltage is removed. To store new information in a flip-flop, it is necessary to address it and apply logical 1 voltage to the appropriate write amplifier input. (The T 7484 circuit has gated write amplifier inputs). The output of the write amplifier responds by dropping to a logical 0 level. Since all logical 0 sense lines are connected to the output of the logical 0 write amplifier and all logical 1 sense lines are connected to the output of the logical 1 write amplifier, a logical 0 voltage on the output of a write amplifier will apply the same voltage to emitters of all flip-flop transistors connected to that amplifier. In all flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. But two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. But if the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on causing the other transistor to turn off. Since the connection between the output of the write amplifier and the sense line is common to the input of the sense amplifier, the memory cannot be used to provide information on the state of a bit while the write amplifiers are activated.

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
t_{pw}	Write pulse width	min. 25	ns
t_s	Set-up time (address lines input)	min. 0	ns
T_{op}	Operating temperature	0 to 70	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.*	Max.	Unit	Fig.
V_{IHAW}	Input voltage required at X or Y address line to ensure writing	$V_{CC} = 4.75V$ $V_{OL} \leq 0.4$ V $I_{OL} = 40mA$	2.1			V	1
V_{IHW}	Input voltage required at W_0 or W_1 inputs to ensure writing		2			V	
V_{IHAS}	Input voltage required to X or Y address line to ensure sensing		2.1			V	
$V_{ILA\overline{W}}$	Input voltage required at X or Y address line to prevent writing				0.8	V	2
$V_{IL\overline{W}}$	Input voltage required at W_0 or W_1 to prevent writing				1	V	1
$V_{ILA\overline{S}}$	Input voltage required at X or Y address lines to prevent writing	$V_{CC} = 4.75V$ $V_o = 5.5$ V $I_{OH} = 250\ \mu A$			1	V	3
V_{OH}	Logical 1 output voltage	$V_{CC} = 4.75V$ $I_{OH} = 250\ \mu A$	5.5			V	
V_{OL}	Logical 0 output voltage	$V_{CC} = 4.75V$ $I_{OL} = 40mA$			0.4	V	1,2
I_{IH}	Logical 1 level input current at write 1 and write 0 (each input)	$V_{CC} = 5.25V$ $V_i = 2.4V$ $V_i = 5.5V$			40 1	μA mA	6
I_{IH}	Logical 1 level input current at each X and each Y address line	$V_{CC} = 5.25V$ $V_i = 4.5V$ $V_i = 5.5V$			400 3	μA mA	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.*	Max.	Unit	Fig.
I_{iL}	Logical 0 level input current at write 1 and write 0 (each input).	$V_{CC} = 5.25V$ $V_i = 0.4V$			-1.6	mA	4
I_{iL}	Logical 0 level input current at all X or all Y address lines				-11	mA	5
I_{CC}	Supply current	$V_{CC} = 5.25V$		55	91	mA	6

* All typical values are at $V_{CC} = 5V$, $T_{amb} = 25°C$

SWITCHING CHARACTERISTICS

($V_{CC} = 5V$, $T_{amb} = 25°C$, refer to figs. 7 and 8 test circuits)

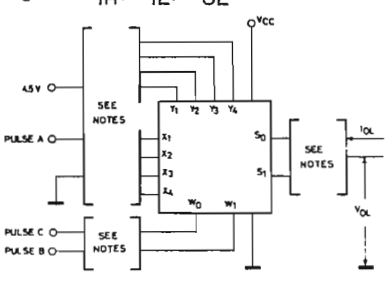
Parameter		Test conditions	Min.	Typ.*	Max.	Unit
t_{wr}	Write recovery time	$X_1 - Y_1$ location addressed $C_L = 15pF$		30	60	ns
t_{pd0}	Propagation delay time to logical 0 level from address-line inputs to S_0 or S_1 outputs.	$X_1 - Y_1$ location addressed $C_L = 15pF$ $C_L = 200pF$		22 27	45 55	ns ns

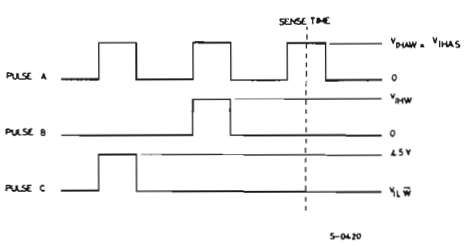
SWITCHING CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{pd1}	Propagation delay time to logical 1 level from address-line inputs to S_0 or S_1 outputs	$X_1 - Y_1$ location addressed $C_L = 15pF$ $C_L = 200pF$		15 20	25 35	ns ns
t_{pd0}	Propagation delay time to logical 0 level from address - line inputs to S_0 or S_1 outputs.	X_1 through X_4 and Y_1 location addressed $C_L = 15pF$		20	30	ns

DC TEST CIRCUITS (Arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{IH}, V_{IL}, V_{OL}



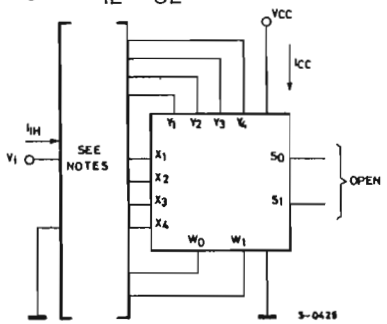


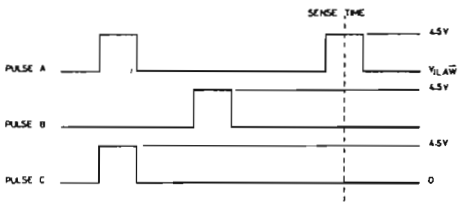
NOTES :

- Each bit location is tested separately by applying pulse A and 4.5V to each of the 16 bit addresses individually. All unused address lines are grounded.
- W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, pulse C to W_1, and measure V_{OL} at S_0. Unused output is open.
- W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, pulse C to W_0, and measure V_{OL} at S_1. Unused output is open.
- For the T7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5V to unused W_0 or W_1 inputs.

DC TEST CIRCUITS (continued)

Fig. 2 - V_{IL}, V_{OL}

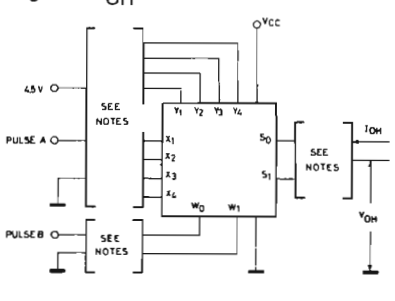


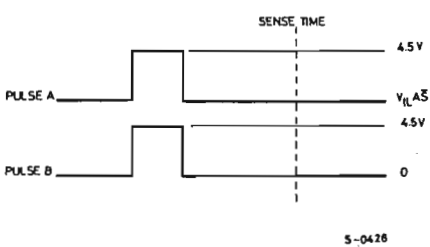


NOTES :

- Each bit location is tested separately by applying pulse A and 4.5V to each of the 16 bit addresses individually. All unused address lines are grounded.
- W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, pulse C to W_1, and measure V_{OL} at S_0. Unused output is open.
- W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, pulse C to W_0, and measure V_{OL} at S_1. Unused output is open.
- For the T7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5V to unused W_0 or W_1 inputs.

Fig. 3 - V_{OH}

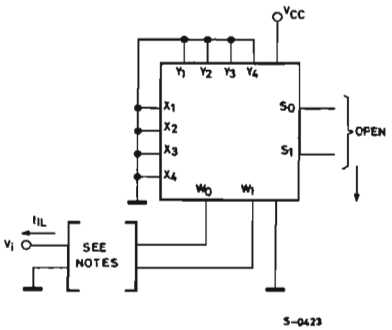




NOTES :

- Each bit location is tested separately by applying pulse A and 4.5V to each of the 16 bit adresses individually. All unused adress lines are grounded.
- W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, ground W_1, and measure V_{OH} at S_0. Unused output is open.
- W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, ground W_0 and measure V_{OH} at S_1. Unused output is open.
- For the T7484, each of the two W_0, or two W_1 inputs are tested separately. Apply 4.5V to the unused input of the gate under test and ground both inputs of the unused gate.

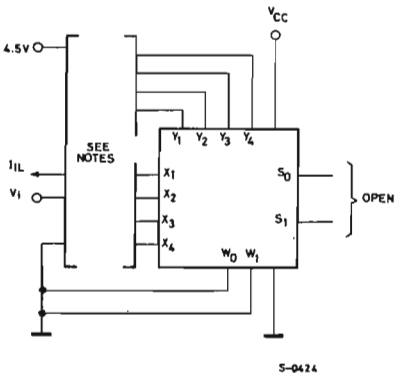
Fig. 4 - I_{IL}



NOTES :

— Each input is tested separately.
— All unused inputs are grounded.

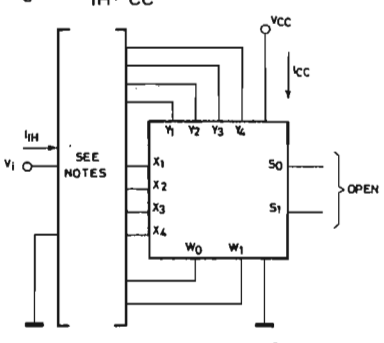
Fig. 5 - I_{IL}



NOTES :

— Each X input is tested separately with the other three X inputs grounded and 4.5V applied to all Y inputs.
— Each Y input is tested separately with the other three Y inputs grounded and 4.5V applied to all Y inputs.
— For the T7484 both W_0 and both W_1 inputs are grounded.

Fig. 6 - I_{IH}, I_{CC}

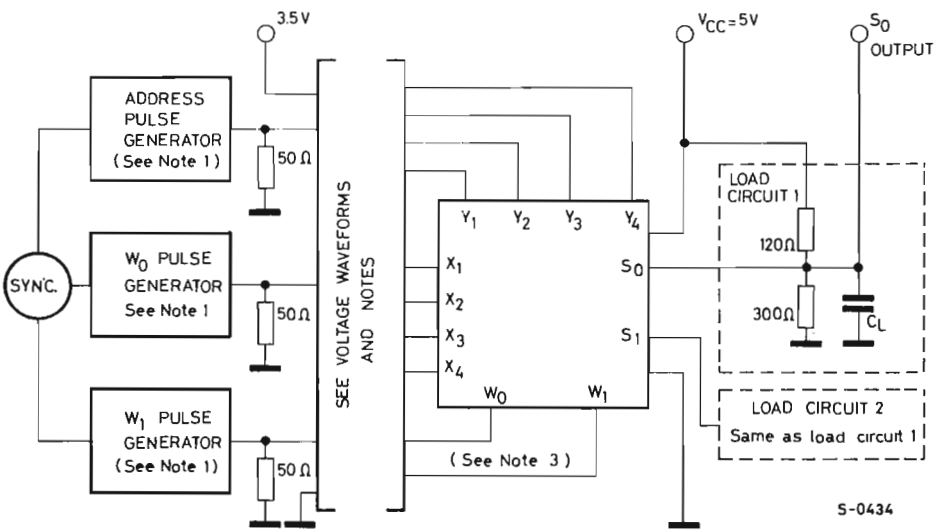


NOTES :

— Each input is tested separately for I_{IH} with all unused inputs grounded.
— When measuring I_{CC} all inputs are grounded.

SWITCHING TIMES

Fig. 7 - Test circuit

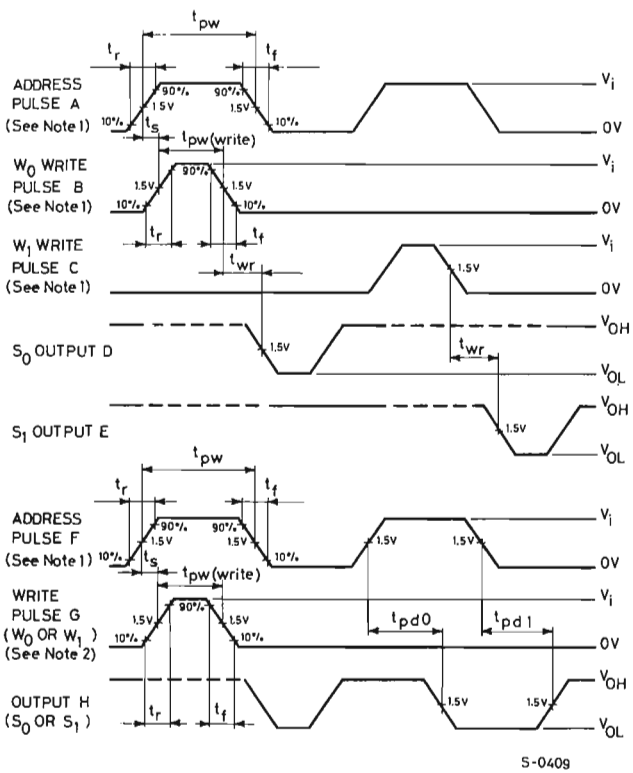


NOTES (for test circuit and waveforms):

1) The pulse generators have the following characteristics : $V_i = 3V$, $t_r = t_f = 10$ ns, $t_s = 0$ to 10 ns. For the address pulse generator, $t_{pw} = 100$ ns and PRR = 2MHz. For the W_0 and W_1 pulse generators, $t_p = 25$ ns and PRR = 1 MHz.
2) C_L includes probe and jig capacitance.
3) For the T7484, unused W_0 and W_1 inputs are 3.5V.

SWITCHING TIMES (continued)

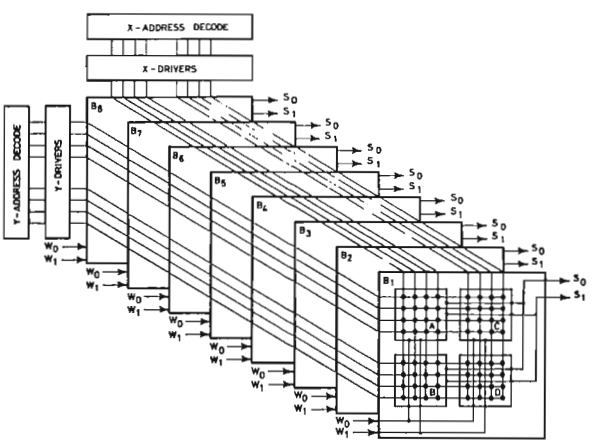
Fig. 8 - Waveforms



T 7481
T 7484

TYPICAL APPLICATIONS

The T 7481/T 7484 can be used to build a memory with a storage capability of m-words (multiples of 16) of n-bit length. Here below a memory of 64 words of 8-bit length is illustrated. Each bit plane (B_1 through B_8) is formed by paralleling the W_0, W_1 inputs, S_0, S_1 outputs, and completing the X-Y matrix connections. The matrix is completed by paralleling the X lines of Circuits A-B and C-D and the Y lines of A-C then B-D, to form the 64 addresses of plane B_1. Two pull-up resistors, one for S_0 and one for S_1, should be provided for wired-OR outputs. The other seven planes are identical to B_1. The X and Y lines of the eight planes are paralleled so that all bits of each word are addressed simultaneously. Addressing of a particular word is accomplished by the X-Y decoder/drivers. For this particular example, the decoder could be a 1-of-8 decoder (see T 7442 and T 7444 applications) and the drivers may consist of discrete transistors, each of supplying current for 16 address inputs. A number of decoding/driving schemes are possible. The T 7484 has gated W_0 and W_1 inputs which may be used to perform the write enable function. External gating may be employed if enabling functions are required xith the T 7481.



TTL INTEGRATED CIRCUIT

T 7483

4 - BIT BINARY FULL ADDER

- ACTIVE PULL-UP OUTPUTS
- DTL - TTL COMPATIBILITY
- HIGH FANOUT

The **T 7483** is a 4-bit binary full adder for adding two four bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit.
A carry look ahead circuit is included to provide minimum carry propagation delays. Designed for medium to high speed, multiple bit, parallel-add/serial-carry applications, the circuit utilizes high speed, high fan-out TTL.
Available in standard temperature range (0 to 70°C) it comes in 16 pin dual in-line plastic package.

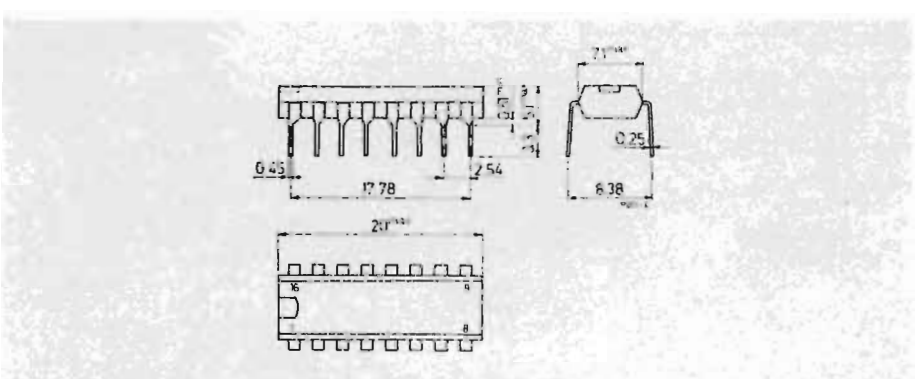
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_I	Input voltage	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBER : T 7483 B1

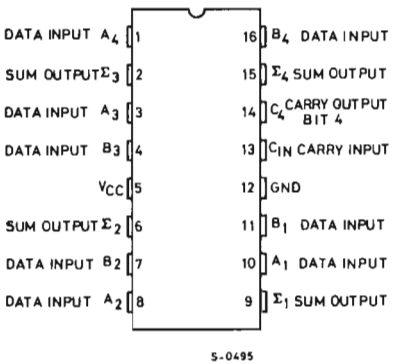
MECHANICAL DATA

Dimensions in mm

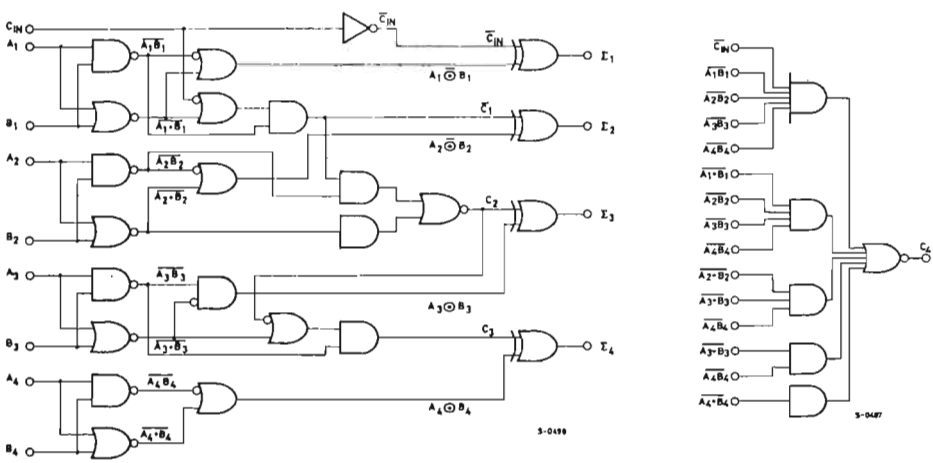


T 7483

CONNECTION DIAGRAM



FUNCTIONAL LOGIC DIAGRAM



TRUTH TABLE

INPUT				OUTPUT					
				When $C_{IN}=0$ / When $C_2=0$			When $C_{IN}=1$ / When $C_2=1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_3	C_2 / C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE: Input conditions at A_1, A_2, B_1, B_2 and C_{IN} are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4 and B_4, are then used to determine outputs Σ_3, Σ_4 and C_4.

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
N	Normalized fan-out from outputs:		
	C_4	max 5	
	$\Sigma_1 - \Sigma_2 - \Sigma_3 - \Sigma_4$	max 10	
T_{op}	Operating temperature	0 to 70	°C

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.*	Max.	Unit	Fig.
V_{IH}	Input high voltage		2			V	1-2
V_{IL}	Input low voltage				0.8	V	1-2
V_{OH}	Output high voltage	V_{CC} = 4.75V	2.4			V	2
V_{OL}	Output low voltage	V_{CC} = 4.75V			0.4	V	1
I_{IH}	Input high current at A_1-A_3-B_1-B_3 or C_{IN} A_2-A_4-B_2-B_4	V_{CC} = 5.25V V_I = 2.4V V_{CC} = 5.25V V_I = 5.5V			80 1	µA mA	3
I_{IL}	Input low current at A_1-A_3-B_1-B_3 or C_{IN} A_2-A_4-B_2-B_4	V_{CC} = 5.25V V_I = 0.4V			-3.2	mA	3
I_{SC} **	Short-circuit output current at Σ_1-Σ_2-Σ_3-Σ_4	V_{CC} = 5.25V	-18		-55	mA	4
I_{SC} **	Short-circuit output current at C_4	V_{CC} = 5.25V	-18		-70	mA	4
I_{CC}	Supply current	V_{CC} = 5.25V		58	79	mA	3

* All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
** Not more than one output should be shorted at a time.

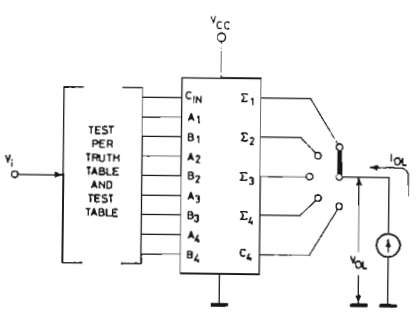
DYNAMIC ELECTRICAL CHARACTERISTICS (V_{CC}=5V, T_{amb}=25°C, N = 10)

Parameter		Test conditions*		Min.	Typ.	Max.	Unit
		from input	to output				
t_{pd1}	Propagation delay time to logical 1 level	C_{IN}	Σ_1		23	34	ns
		C_{IN}	Σ_2		24	35	ns
		C_{IN}	Σ_3		30	50	ns
		C_{IN}	Σ_4		30	50	ns
		C_{IN}	C_4		12	20	ns
		A_2 or B_2	Σ_2			40	ns
		A_4 or B_4	Σ_4			40	ns
t_{pd0}	Propagation delay time to logical 0 level	C_{IN}	Σ_1		20	34	ns
		C_{IN}	Σ_2		22	35	ns
		C_{IN}	Σ_3		24	40	ns
		C_{IN}	Σ_4		28	50	ns
		C_{IN}	C_4		12	20	ns
		A_2 or B_2	Σ_2			35	ns
		A_4 or B_4	Σ_4			35	ns

* See switching times

DC TEST CIRCUITS (Arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{OL}, I_{OL}



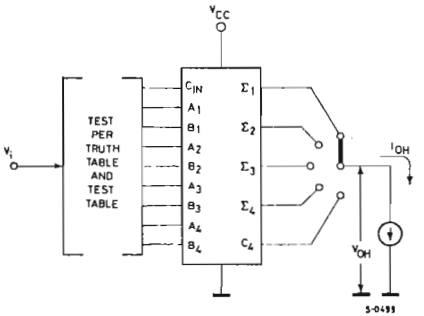
Test table

Output Under Test	I_{OL}
Σ_1 - Σ_2 - Σ_3 - Σ_4	16 mA
C_4	8 mA

Each input or output is tested separately.

DC TEST CIRCUITS (continued)

Fig. 2 - V_{OH}, I_{OH}

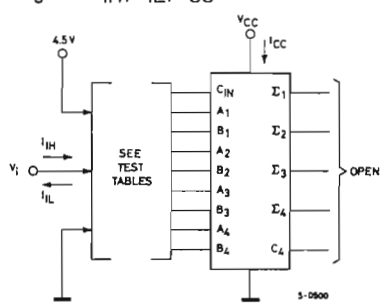


Test table

Output Under Test	I_{OH}
$\Sigma_1 - \Sigma_2 - \Sigma_3 - \Sigma_4$	-400 μA
C_4	-200 μA

Each input or output is tested separately

Fig. 3 - I_{IH}, I_{IL}, I_{CC}



I_{IL} Test table

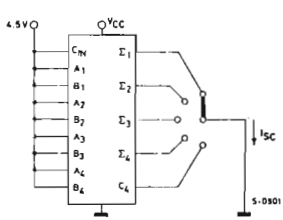
APPLY V_i TEST I_i	APPLY 4.5V
C_{IN}	A_1 and B_1
A_1	C_{IN} and B_1
B_1	C_{IN} and A_1
A_2	None
B_2	None
A_3	A_2-B_2 and B_3
B_3	A_2-B_2 and A_3
A_4	None
B_4	None

I_{IH} Test table

APPLY V_i TEST I_i	GND
C_{IN}	A_1 and B_1
A_1	C_{IN} and B_1
B_1	C_{IN} and A_1
A_2	None
B_2	None
A_3	A_2-B_2 and B_3
B_3	A_2-B_2 and A_3
A_4	None
B_4	None

1. Each input is tested separately.
2. When testing I_{CC} apply 4.5V to A_1-A_2-A_3-A_4, and C_{IN}; and ground B_1, B_2, B_3 and B_4.

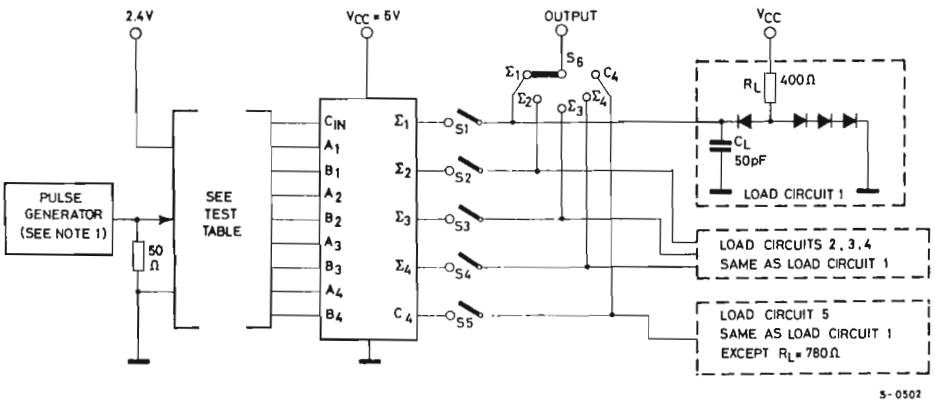
Fig. 4 - I_{SC}



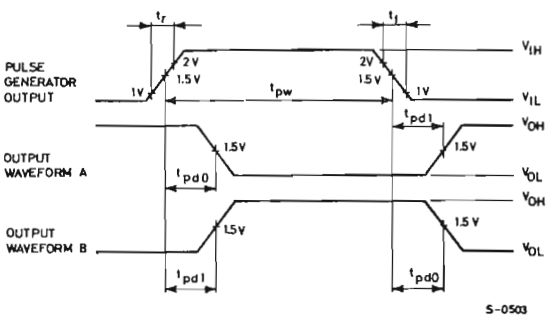
Each output is tested separately.

SWITCHING TIMES

Test circuit



Waveforms



NOTES:

1 - Pulse generator output pulse characteristics: $V_{IH} \leqslant 2.4V$, $V_{IL} \leqslant 0.4V$, $t_r = 8$ to 15 ns, $t_f = 3$ to 5 ns, PRR = 1 MH_Z, $t_{pw} = 200$ ns, and $Z_{out} \approx 50\ \Omega$

2 - Perform test in accordance with test table.

3 - Each output is tested separately.

4 - Voltage values are with respect to network ground terminal.

5 - C_L includes probe and jig capacitance.

6 - All diodes are 1N3064.

SWITCHING TIMES (continued)

Test table

PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
t_{pd1} t_{pd0}	C_{IN}	Σ_1 (WAVEFORM A)	A_1	B_1, A_2 and B_2	CLOSED	OPEN	OPEN	OPEN	OPEN
t_{pd1} t_{pd0}	C_{IN}	Σ_2 (WAVEFORM A)	A_1 and A_2	B_1 and B_2	OPEN	CLOSED	OPEN	OPEN	OPEN
t_{pd1} t_{pd0}	C_{IN}	Σ_3 (WAVEFORM A)	A_1, A_2 and A_3	B_1, B_2 and B_3	OPEN	OPEN	CLOSED	OPEN	OPEN
t_{pd1} t_{pd0}	C_{IN}	Σ_4 (WAVEFORM A)	A_1, A_2, A_3 and A_4	B_1, B_2, B_3 and B_4	OPEN	OPEN	OPEN	CLOSED	CLOSED
t_{pd1} t_{pd0}	C_{IN}	C_4 (WAVEFORM B)	A_1, A_2, A_3 and A_4	B_1, B_2, B_3 and B_4	OPEN	OPEN	OPEN	OPEN	CLOSED
t_{pd1} t_{pd0}	A_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2 and C_{IN}	OPEN	CLOSED	OPEN	OPEN	OPEN
t_{pd1} t_{pd0}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2 and C_{IN}	OPEN	CLOSED	OPEN	OPEN	OPEN
t_{pd1} t_{pd0}	A_4	Σ_4 (WAVEFORM B)	None	A_3, B_3 and B_4	OPEN	OPEN	OPEN	CLOSED	OPEN
t_{pd1} t_{pd0}	B_4	Σ_4 (WAVEFORM B)	None	A_3, B_3 and A_4	OPEN	OPEN	OPEN	CLOSED	OPEN

NOTE: Inputs and outputs not otherwise specified are open.

TTL INTEGRATED CIRCUIT

T 7492

DIVIDE-BY-12 COUNTER/DIVIDE-BY-2 AND DIVIDE-BY-6

- ACTIVE PULL-UP OUTPUTS
- DTL AND TTL COMPATIBLE
- AVERAGE POWER DISSIPATION of 155 mW
- HIGH FANOUT

The **T 7492** is a versatile MSI constructed on a single silicon chip by means of the planar epitaxial process.
This device is a 4-bit Binary counter consisting of four master slave flip-flops which are internally interconnected to provide a divide-by-2 counter and a divide-by-6 counter. Available in standard temperature range (0 to 70°C) it comes in 14-lead dual in-line plastic package.

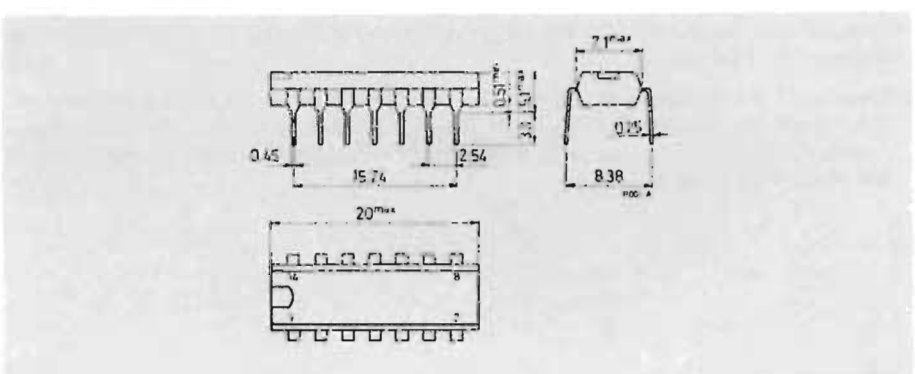
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_I	Input voltage	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBER: T 7492 B1

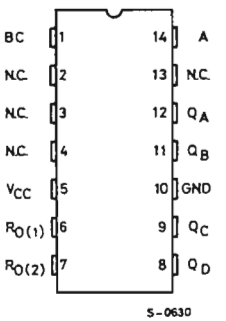
MECHANICAL DATA

Dimensions in mm



T 7492

CONNECTION DIAGRAM



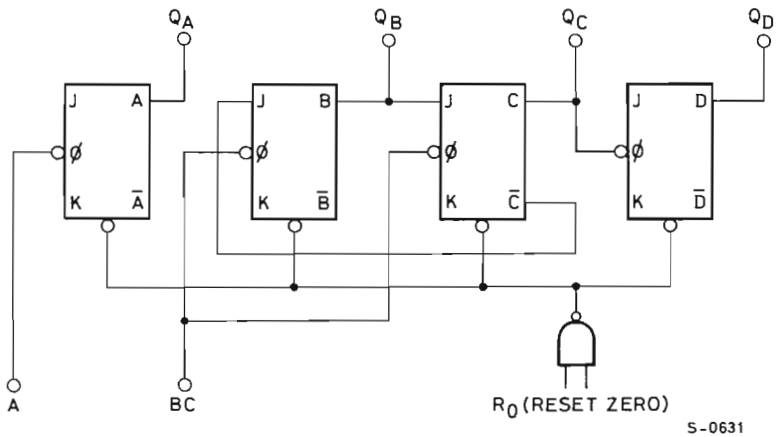
FUNCTIONAL DESCRIPTION

A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical "0" level.
As the output from flip-flop "A" is not internally connected to the succeeding flip-flop, the counter may be operated in two independent modes :

1) When used as a divide-by-12 counter, output Q_A must be externally connected to input BC.
   Simultaneous divisions of 2, 6, and 12 are performed at the Q_A, Q_C, and Q_D outputs as shown in the truth table.

2) When used as a divide-by-6 counter, the input count pulses are applied to input BC. Simultaneously, frequency divisions of 3 and 6 are available at Q_C and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-6 counter.

FUNCTIONAL LOGIC DIAGRAM



TRUTH TABLE (See NOTES 1, 2 and 3)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

NOTES :

1. Output Q_A connected to input BC.
2. To reset all outputs to LOW level both $R_{O(1)}$ and $R_{O(2)}$ inputs must be at HIGH level state.
3. Either (or both) reset inputs $R_{O(1)}$ and $R_{O(2)}$ must be at a LOW level to count.

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
N*	Normalized fanout (each output)	max 10	–
t_{pw}	Pulse width (at reset and count inputs)	min 50	ns
T_{op}	Operating temperature	0 to 70	°C

* Fanout from output Q_A to input BC and to 10 additional series T 74 loads is permitted.

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ*	Max.	Unit
V_{IH}	Input high voltage		2			V
V_{IL}	Input low voltage				0.8	V
V_{OH}	Output high voltage	V_{CC} = 4.75V I_{OH} = -400μA	2.4			V
V_{OL}	Output low voltage	V_{CC} = 4.75V I_{OL} = 16 mA			0.4	V
I_{IH}	Input high current at $R_{O(1)}$ or $R_{O(2)}$	V_{CC} = 5.25V V_i = 2.4V V_{CC} = 5.25V V_i = 5.5V			40 1	μA mA
I_{IH}	Input high current at A	V_{CC} = 5.25V V_i = 2.4V V_{CC} = 5.25V V_i = 5.5V			80 1	μA mA
I_{IH}	Input high current at BC	V_{CC} = 5.25V V_i = 2.4V V_{CC} = 5.25V V_i = 5.5V			160 1	μA mA
I_{IL}	Input low current at $R_{O(1)}$ or $R_{O(2)}$	V_{CC} = 5.25V V_i = 0.4V			-1.6	mA
I_{IL}	Input low current at A	V_{CC} = 5.25V V_i = 0.4V			-3.2	mA
I_{IL}	Input low current at BC	V_{CC} = 5.25V V_i = 0.4V			-6.4	mA
I_{SC} **	Short-circuit output current	V_{CC} = 5.25V	-18		-57	mA
I_{CC}	Supply current	V_{CC} = 5.25V V_i = 4.5V		31	51	mA

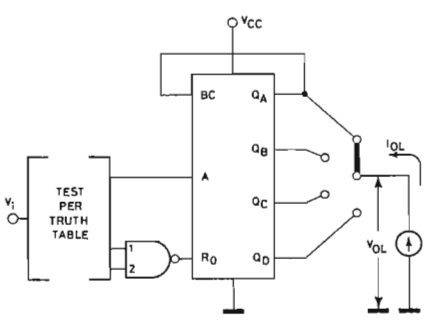
* All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
** Not more than one output should be shorted at a time.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{CC}=5V, T_{amb}=25°C, N=10)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
f_{max}	Maximum count frequency	C_L = 15 pF R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical "1" level from input count pulse to output D	C_L = 15 pF R_L = 400 Ω		60	100	ns
t_{pd0}	Propagation delay time to logical "0" level from input count pulse to output D	C_L = 15 pF R_L = 400 Ω		60	100	ns

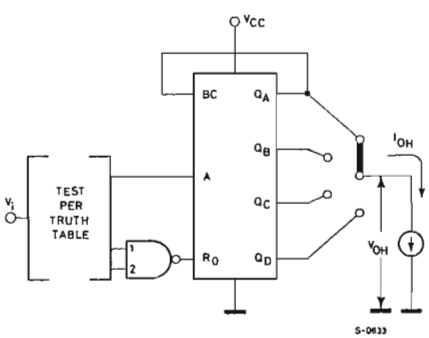
DC TEST CIRCUITS (Arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{IH}, V_{OL}



1. Each output is tested in the LOW level state.

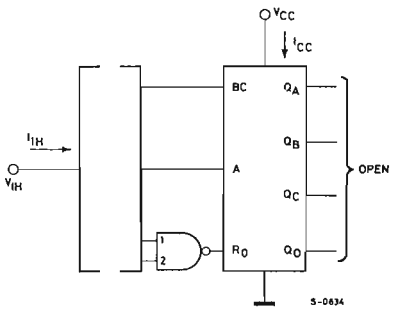
Fig. 2 - V_{IL}, V_{OH}



1. Each output is tested in the HIGH level state.

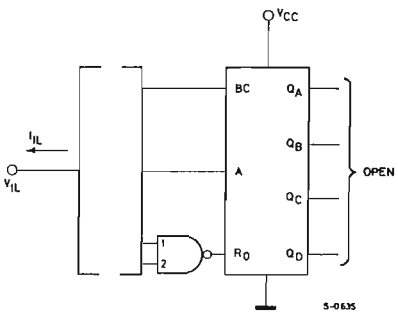
DC TEST CIRCUITS (continued)

Fig. 3 - I_{IH}, I_{CC}



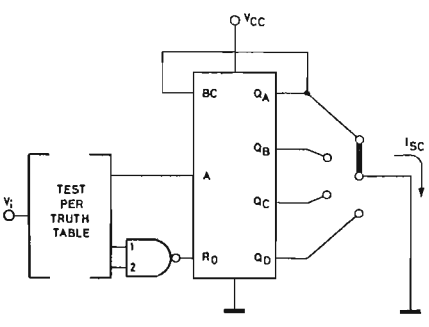
1. Each input is tested separately.
2. When testing $R_{O(1)}$ ground $R_{O(2)}$.
3. When testing $R_{O(2)}$ ground $R_{O(1)}$.
4. When testing I_{CC} reset all outputs to LOW level, ground all inputs, then measure I_{CC}.

Fig. 4 - I_{IL}



1. Each input is tested separately.
2. When testing $R_{O(1)}$ apply 4.5V to $R_{O(2)}$.
3. When testing $R_{O(2)}$ apply 4.5V to $R_{O(1)}$.

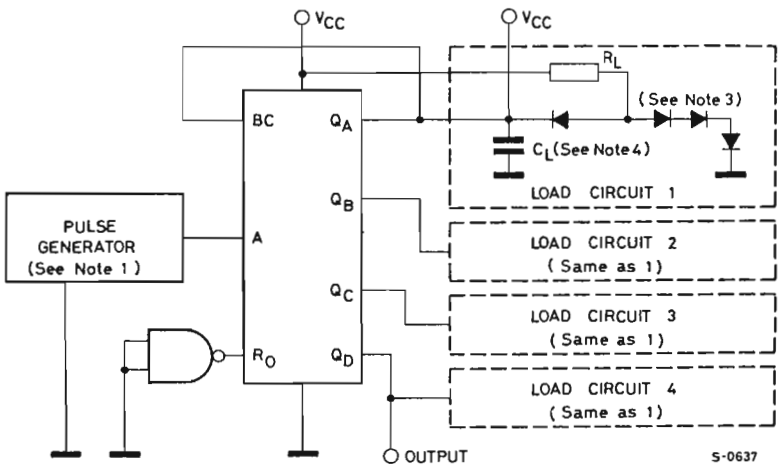
Fig. 5 - I_{SC}



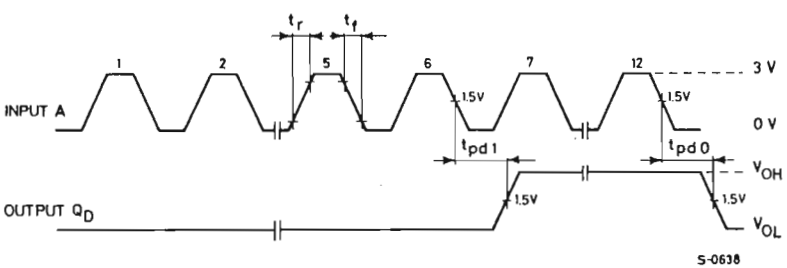
1. Each output is tested in the HIGH level state.

SWITCHING TIMES

Test circuit



Waveforms (See note 2)



NOTES:

1. The pulse generator has the following characteristics; $V_i = 3V$, $t_r = t_f \leqslant 15$ ns, $t_{pw} = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. Propagation delay $= \dfrac{t_{pd0} + t_{pd1}}{2}$
3. All diodes are 1N3064.
4. C_L includes probe and jig capacitance.

TTL INTEGRATED CIRCUIT

T 74121

PRELIMINARY DATA

MONOSTABLE MULTIVIBRATOR

- TTL COMPATIBLE
- ACTIVE PULL-UP OUTPUT
- NORMALIZED FANOUT of 10

The T **74121** is a monostable multivibrator, featuring d-c triggering from positive or gated negative-going inputs with inhibit facility.
Both positive and negative-going output pulses are provided.
Available in standard temperature range (0 to 70°C), it comes in 14-lead dual in-line plastic or ceramic package.

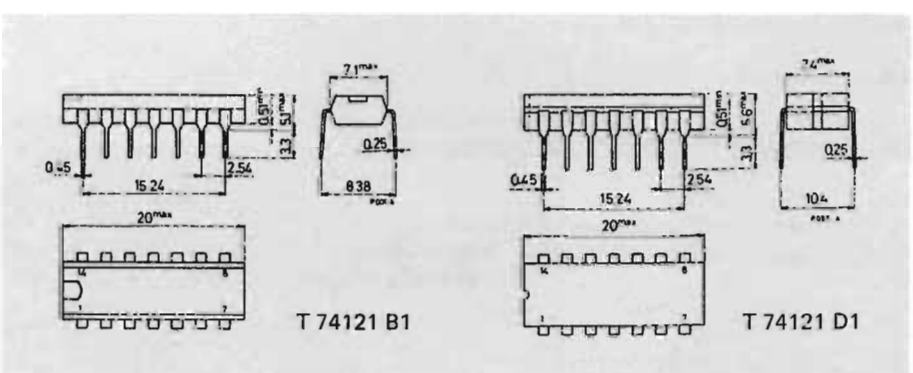
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBERS : T 74121 B1 for dual in-line plastic package
T 74121 D1 for dual in-line ceramic package

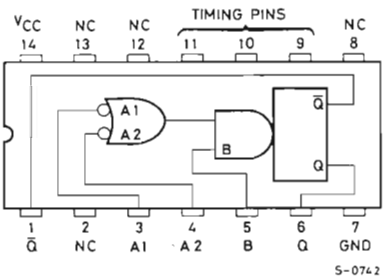
MECHANICAL DATA

Dimensions in mm



T 74121

CONNECTION DIAGRAM



TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Short
X	0	0	X	0	1	One Short
1	1	1	X	0	1	One Short
1	1	1	0	X	1	Inhibit
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

$1 = V_i\ (1) \geqslant 2V$
$0 = V_i\ (0) \leqslant 0.8V$

NOTES :

1. t_n = time before input transition
2. t_{n+1} = time after input transition
3. X indicates that either a logical 0 or 1 may be present
4. NC = no internal connection
5. A1 and A2 are negative-edge triggered logic inputs–and will trigger the one shot when either or both go to logical 0 with B at logical 1
6. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See truth table)
7. External timing capacitor may be connected between pin 10 (positive) and pin 11. With no external capacitance, an output pulse width of typically 30 ns is obtained
8. To use the internal timing resistor(2kΩ nominal), connect pin 9 to pin 14
9. To obtain variable pulse width connect external variable resistance between pin 9 and 14. No external current limiting needed
10. For accurate repeatable pulse widths connect an external resistor between pin 11 and pin 14 with pin 9 open-circuit

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
N	Normalized fanout from each output	max 10	
$t_r - t_f$	Input pulse rise and fall time: Schmitt input (B)	max 1	V/s
	Logic input (A1, A2)	max 1	V/μs
t_{pw}	Input pulse width	min 50	ns
R_t	External timing resistance	max 40	kΩ
C_t	External timing capacitance	0 to 1000	μF

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.*	Max.	Unit
V_{IH}	Input high voltage		2			V
V_{IL}	Input low voltage				0.8	V
V_{OH}	Output high voltage	V_{CC} = 4.75V I_{OH}=-400μA	2.4	3.3		V
V_{OL}	Output low voltage	V_{CC} = 4.75V I_{OL}= 16 mA		0.22	0.4	V
I_{IH}	Input high current at A1 or A2	V_{CC} = 5.25V V_i = 2.4V		2	40	μA
		V_{CC} = 5.25V V_i = 5.5V		0.05	1	mA
I_{IH}	Input high current at B	V_{CC} = 5.25V V_i ≧ 2.4V		4	80	μA
		V_{CC} = 5.25V V_i = 5.5V		0.05	1	mA
I_{IL}	Input low current at A1 or A2	V_{CC} = 5.25V V_i = 0.4V		-1	-1.6	mA
I_{IL}	Input low current at B	V_{CC} = 5.25V V_i = 0.4V		-2	-3.2	mA
I_{SC}**	Short-circuit output current at Q or $\overline{Q}$	V_{CC} = 5.25V	-18	-25	-55	mA
I_{CC}	Power supply current in quiescent (unfired) state	V_{CC} = 5.25V		13	25	mA
I_{CC}	Power supply current in fired state	V_{CC} = 5.25V		23	40	mA

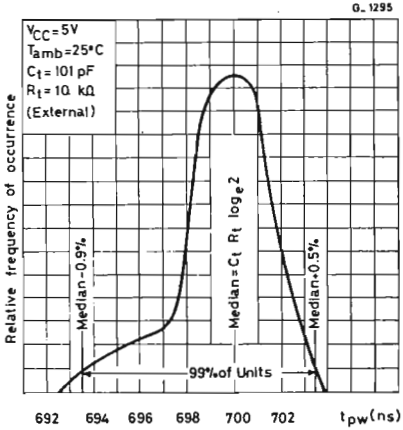
* All typical values are at V_{CC} = 5V, T_{amb} = 25°C

** Not more than one output should be shorted at a time

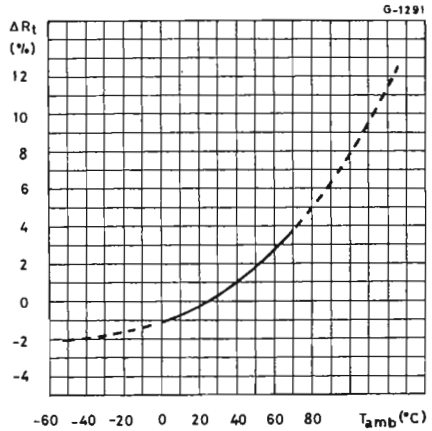
DYNAMIC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
$t_{pd\ 1}$	Propagation delay time to logical 1 level from B input to Q output	C_L = 15 pF	C_t = 80 pF	15	35	55	ns
$t_{pd\ 1}$	Propagation delay time to logical 1 level from A1/A2 inputs to Q output	C_L = 15 pF	C_t = 80 pF	25	45	70	ns
$t_{pd\ 0}$	Propagation delay time to logical 0 level from B input to $\overline{Q}$ output	C_L = 15 pF	C_t = 80 pF	20	40	65	ns
$t_{pd\ 0}$	Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{Q}$ output	C_L = 15 pF	C_t = 80 pF	30	50	80	ns
t_{pw}	Pulse width obtained using internal timing resistor	C_L = 15 pF R_t = open	C_t = 80 pF Pin 9 to V_{CC}	70	110	150	ns
t_{pw}	Pulse width obtained with 0 timing capacitance	C_L = 15 pF R_t = open	C_t = 0 Pin 9 to V_{CC}	20	30	50	ns
t_{pw}	Pulse width obtained using external timing resistor	C_L = 15 pF R_t = 10 kΩ	C_t = 100 pF Pin 9 open	600	700	800	ns
		C_L = 15 pF R_t = 10 kΩ	C_t = 1 μF Pin 9 open	6	7	8	ms
t_h	Input hold time	C_L = 15 pF R_t = open	C_t = 80 pF Pin 9 to V_{CC}		30	50	ns

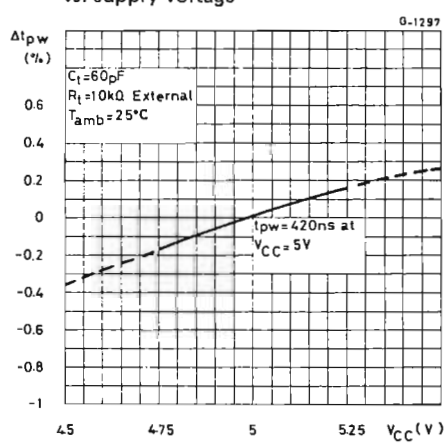
Typical distribution of units for output pulse width



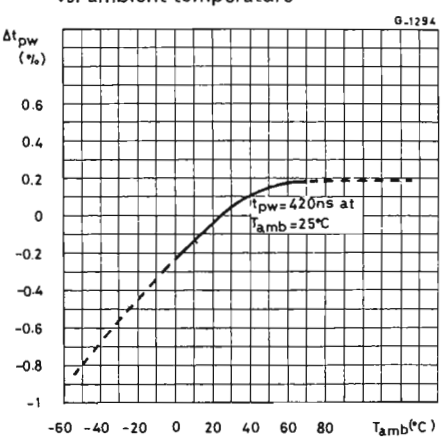
Typical variation in internal timing resistor value vs. ambient temperature



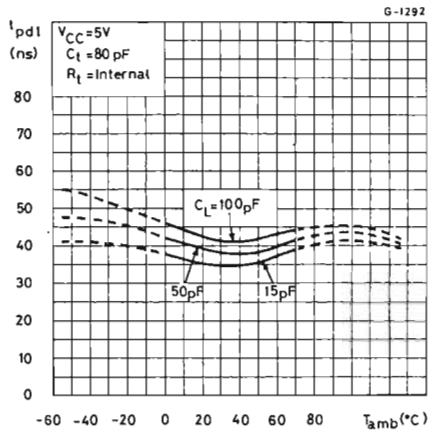
Typical variation in output pulse width vs. supply voltage



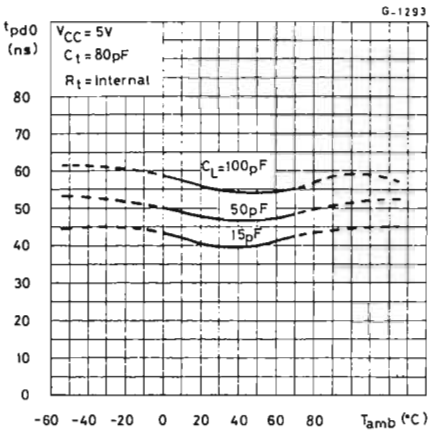
Typical variation in output pulse width vs. ambient temperature



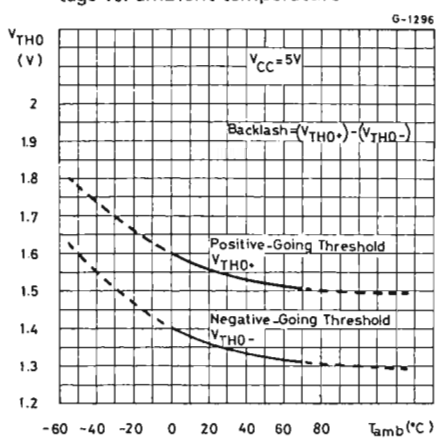
Typical propagation delay time to logical 1 level vs. ambient temperature (B input to Q output)



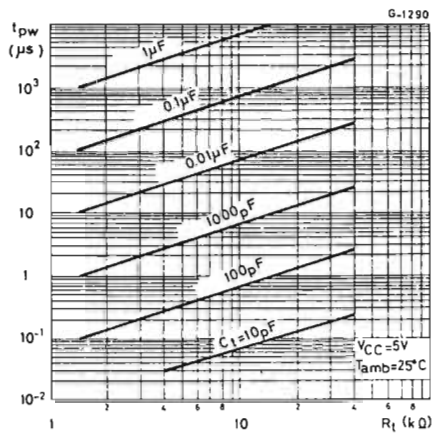
Typical propagation delay time to logical 0 level vs. ambient temperature (B input to $\overline{Q}$ output)



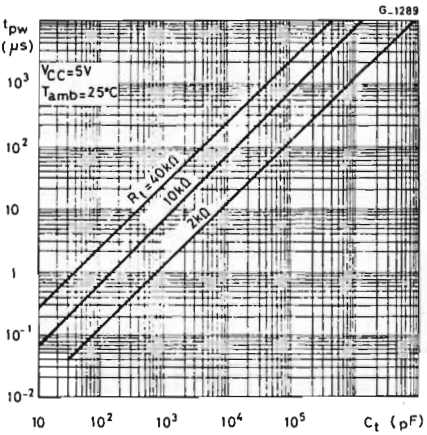
Typical Schmitt trigger threshold voltage vs. ambient temperature



Typical output pulse width vs. timing resistor value

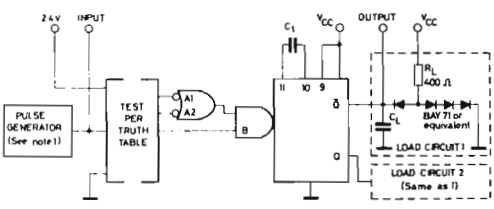


Typical output pulse width vs. external capacitance

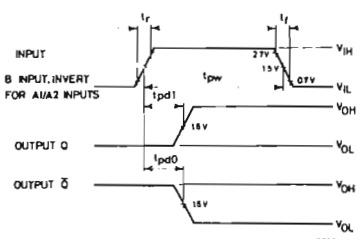


SWITCHING TIMES

Test circuit



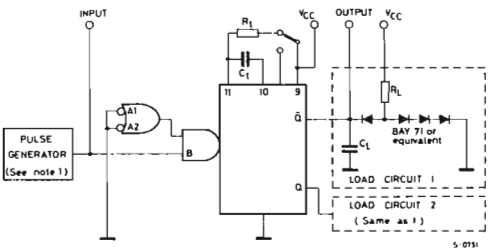
Waveforms



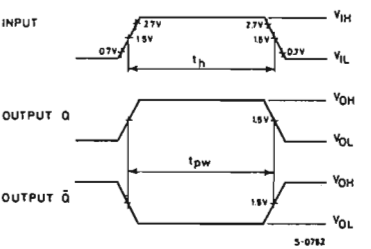
NOTES:
1. The pulse generator has the following characteristics: V_I = 3.5V, t_r = 10 ns, t_f = 5 ns, $t_{pw} \geqslant$ 50 ns, PRR = 1 MHz, and $Z_{out} \approx$ 50 Ω
2. C_L includes probe and jig capacitance

SWITCHING TIMES (continued)

Test circuit (t_{pw} "internal/minimum" t_h)



Waveforms



NOTES:
1. The pulse generator has the following characteristics: V_i = 3.5V, t_r = 10 ns, t_f = 5 ns, t_{pw} = 50 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$
2. C_L includes probe and jig capacitance

T 74122
T 74123

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

- RETRIGGERABLE FOR VERY LONG OUTPUT PULSES: up to 100% DUTY-CYCLE
- OVERRIDING CLEAR TERMINATES OUTPUT PULSE

The T 74122 is a TTL and T 74123 is a dual TTL retriggerable monostable multivibrator featuring DC triggering from gated low-level active (A) and high level active (B) inputs, and also provides overriding direct clear inputs. The retrigger capability simplifies the generation of output pulses of extremely long duration. Available in standard temperature range (0 to 70°C), it comes in 14 and 16 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS

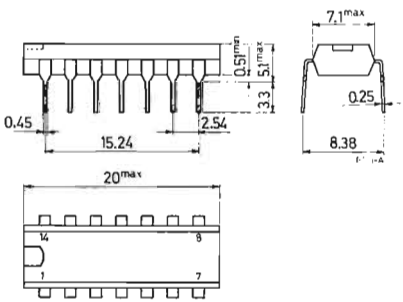
V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

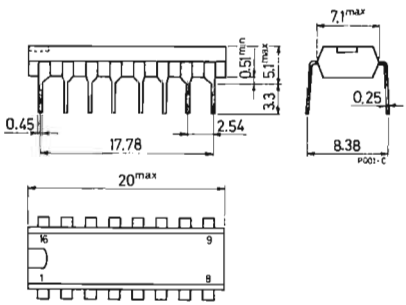
ORDERING NUMBERS: T 74XXX B1 for dual in-line plastic package
T 74XXX D1 for dual in-line ceramic package

T 74122
T 74123

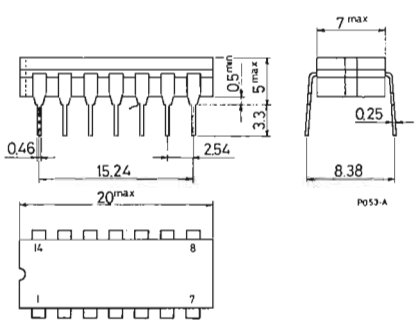
MECHANICAL DATA (dimensions in mm)

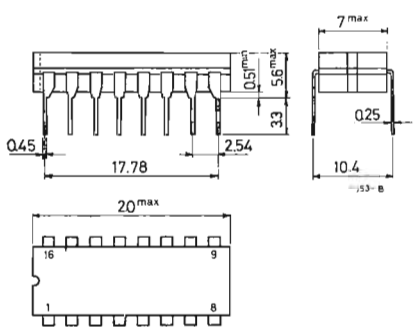
Dual in-line plastic packages: for T74 XXX B1





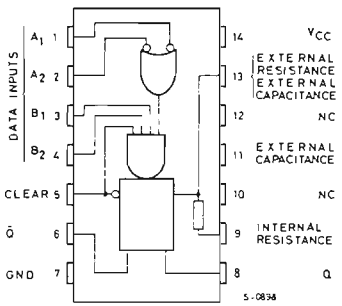
Dual in-line ceramic packages: for T74 XXX D1





CONNECTION DIAGRAMS and TRUTH TABLE

For **T 74122** (See note B and C)

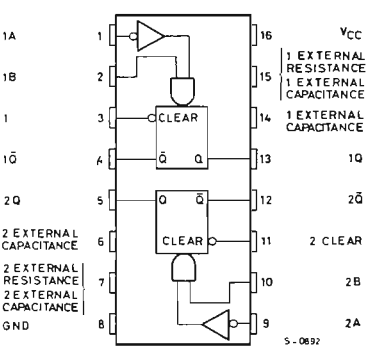


POSITIVE LOGIC:
Low input to clear resets Q to low level and inhibits data inputs

(See note A)

INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	$\bar{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
↓	H	H	H	⎍	⎎

For **T 74123** (See note C)



POSITIVE LOGIC:
Low input to clear resets Q to low level and inhibits data inputs

(See note A)

INPUTS		OUTPUTS	
A	B	Q	$\bar{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎎
↓	H	⎍	⎎

NOTES: A) H = high level (steady state), L = low level (steady state), ↑ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions)

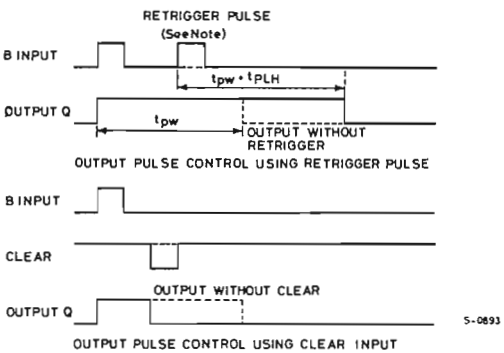
B) To use the internal timing resistor of T 74122 (10 kΩ nominal), connect R_{int} to V_{CC}

C) An external timing capacitor may be connected between C_t and R_t/C_t (positive)

FUNCTIONAL LOGIC DIAGRAM

TYPICAL INPUT/OUTPUT PULSES

Below illustrates triggering the one-shot with the high-level active (B) inputs



NOTE: Retrigger pulse must not start before 0.22 C_t (pF) nsec. after previous trigger pulse

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
R_t	External timing resistance	5 to 50	kΩ
C_t	External timing capacitance	no restriction	
t_{pw}	Pulse width	min. 40	ns
t_s	Set-up time (see note 1)	min. 40	ns
t_h	Hold time (see note 2)	min. 40	ns
N	Normalized fanout	max. 10	—
T_{op}	Operating temperature	0 to 70	°C

NOTES: 1) Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition

2) Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.*	Max.	Unit
V_{IH}	Input high voltage		2			V
V_{IL}	Input low voltage				0.8	V
V_{OH}	Output high voltage	V_{CC} = 4.75V I_{OH} = -800μA	2.4			V
V_{OL}	Output low voltage	V_{CC} = 4.75V I_{OL} = 16 mA		0.22	0.4	V
I_{IH}	Input high current	V_{CC} = 5.25V V_i = 2.4V for DATA INPUTS for CLEAR INPUT			 40 80	 μA μA
I_{IL}	Input low current	V_{CC} = 5.25V V_i = 0.4V for DATA INPUTS for CLEAR INPUT			 -1.6 -3.2	 mA mA
I_{SC}**	Short-circuit output current	V_{CC} = 5.25V	-10		-40	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = 5.25V		46	66	mA

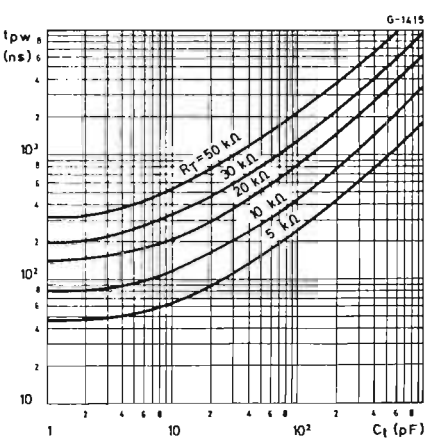
* All typical values are at V_{CC} = 5V, T_{amb} = 25°C

** Not more than one output should be shorted at a time

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C, N = 10, C_t = 0, R_t = 5 kΩ, R_L = 400Ω)

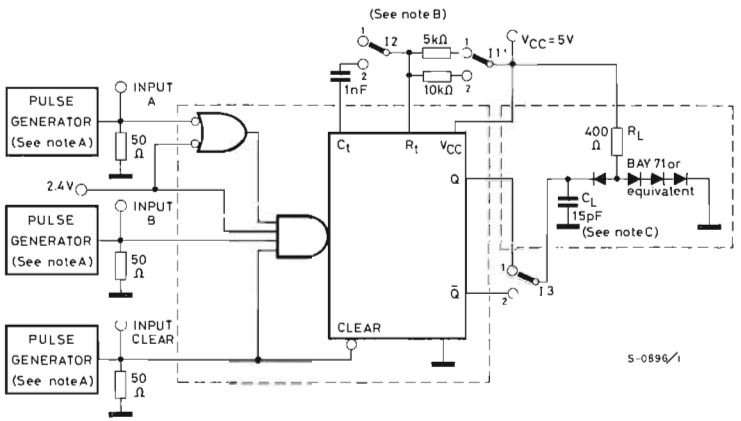
Parameter		Test conditions		Min.	Typ.	Max.	Unit
		from input	to output				
t_{PLH}	Propagation delay time low-to-high-level	Either A	Q		22	33	ns
		Either B	Q		19	28	ns
t_{PHL}	Propagation delay time high-to-low-level	Either A	$\overline{Q}$		30	40	ns
		Either B	$\overline{Q}$		27	36	ns
t_{PHL}	Propagation delay time high-to-low-level	Clear	Q		18	27	ns
t_{PLH}	Propagation delay time low-to-high-level	Clear	$\overline{Q}$		30	40	ns
t_{pw}	Minimum pulse width		Q		45	65	ns
t_{pw}	Pulse width	C_t = 1000 pF R_t = 10 kΩ	Q				
			for **T 74122**	3.08	3.42	3.76	µs
			for **T 74123**	2.7	3.03	3.76	µs

Output pulse width vs. external timing capacitance



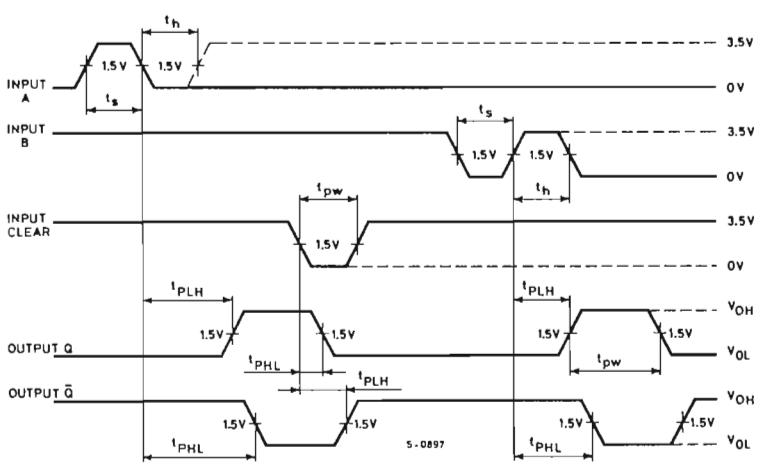
SWITCHING TIMES

Test circuit



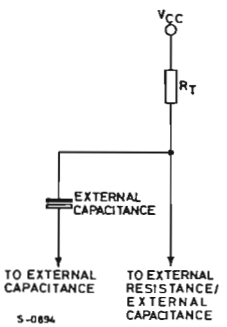
NOTES: A) The pulse generators have the following characteristics: $t_r = t_f \leqslant 10$ ns, PRR $\leqslant 1$ MHz
B) See "test conditions" for R_t and C_t values
C) C_L include probe and jig capacitance

Waveforms

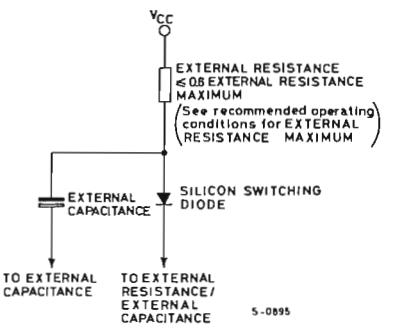


TYPICAL APPLICATIONS

Timing component connections when $C_t \leqslant 1000$ pF (Fig. 1)



Timing component connections when $C_t > 1000$ pF and clear is used (Fig. 2)



To prevent reverse voltage across C_t, it is recommended that the method shown in figure 2 be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

$$t_{pw} = 0.28\ R_t\ C_t\ (1 + \frac{0.7}{R_t})$$

where R_t is in kΩ
C_t is in pF
t_{pw} is in ns

TTL INTEGRATED CIRCUIT

T 74157

QUAD 2 - INPUT MULTIPLEXER

- FULLY BUFFERED OUTPUTS
- ON-CHIP SELECT LOGIC DECODING
- TYPICAL PROPAGATION DELAY of 9 ns DATA to OUTPUT
- INPUT CLAMPING DIODES
- TTL-DTL COMPATIBLE

The T 74157 is a monolithic high speed quad two input digital multiplexer circuit. It consists of four multiplexing circuits with common select and enable logic, and each circuit contains two inputs and one output. Active pull-up outputs ensure high drive and high speed performance.
The enable input ($\overline{E}$) is active low. When not activated all outputs are low regardless of all other inputs. Available in standard temperature range (0 to 70°C) it comes in 16-lead dual in-line plastic package.

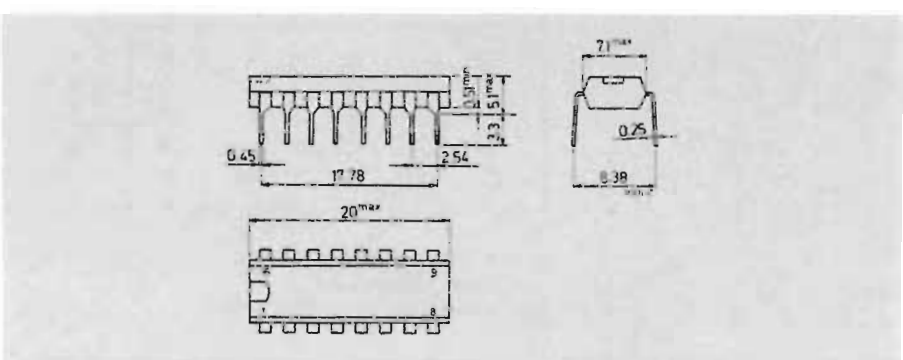
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBER: T 74157 B1

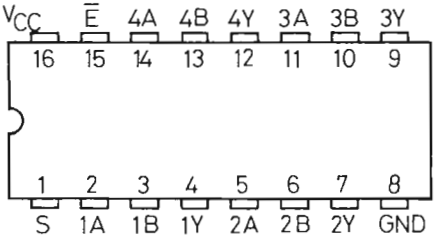
MECHANICAL DATA

Dimensions in mm



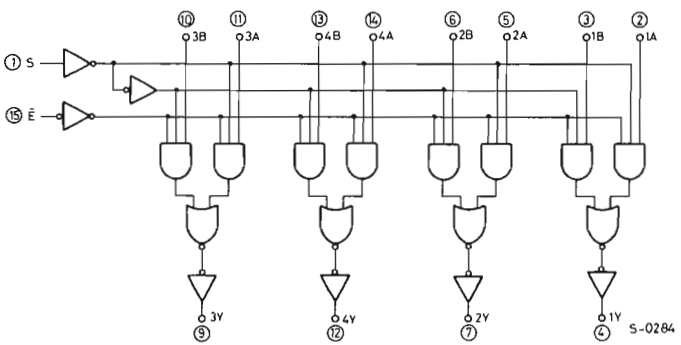
T 74157

CONNECTION DIAGRAM



S-0283

LOGIC DIAGRAM



S-0284

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	B	A	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level.
L = LOW Voltage Level.
X = Either HIGH or LOW Logic Level.

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
N	Normalized fan-out (each output)	max 10	–
T_{op}	Operating temperature	0 to 70	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.*	Max.	Unit
V_{IH}	Input high voltage		2			V
V_{IL}	Input low voltage				0.8	V
V_C	Input clamp diode voltage	V_{CC}= 4.75V I_i= -12mA			-1.5	V
V_{OH}	Output high voltage	V_{CC}= 4.75V V_{IH}= 2V V_{IL}= 0.8V I_{OH}= -800µA	2.4			V
V_{OL}	Output low voltage	V_{CC}= 4.75V V_{IH}= 2V V_{IL}= 0.8V I_{OL}= 16mA			0.4	V
I_{IH}	Input high current	V_{CC}= 5.25V V_I= 2.4V V_{CC}= 5.25V V_I= 5.5V			40 1	µA mA
I_{IL}	Input low current	V_{CC}= 5.25V V_I= 0.4V			-1.6	mA
I_{SC}**	Short-circuit output current	V_{CC}= 5.25V	-18		-55	mA
I_{CC}***	Supply current	V_{CC}= 5.25V		30	48	mA

* All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

** Not more than one output should be shorted at a time

*** It is measured with 4.5V applied to all inputs and all outputs open.

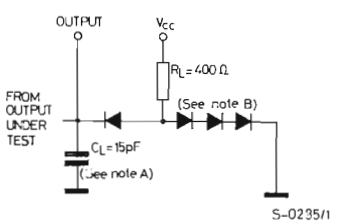
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C, N = 10)

Parameter		Test conditions*		Min.	Typ.	Max.	Unit
		From	To				
t_{pd1}	Propagation delay time to logical 1 level	Data	Output		9	14	ns
		Enable	Output		13	20	ns
		Select	Output		15	23	ns
t_{pd0}	Propagation delay time to logical 0 level	Data	Output		9	14	ns
		Enable	Output		14	21	ns
		Select	Output		18	27	ns

* See switching times load circuit and waveforms.

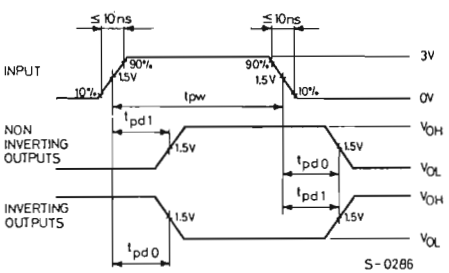
SWITCHING TIMES

Load circuit



NOTE: A. C_L includes probe and jig capacitance.
B. All diodes are 1N 3064.

Waveforms



NOTE: The input waveform is supplied by a generator with the following characteristics: PRR = 1 MHz, Z_{out} = 50 ohm, t_{pw} = 100 ns.

TTL INTEGRATED CIRCUITS

T 74192
T 74193

PRELIMINARY DATA

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

- TTL-DTL COMPATIBILITY
- SYNCHRONOUS OPERATION
- FULLY INDEPENDENT CLEAR INPUT
- INDIVIDUAL PRESET to EACH FLIP-FLOP
- TYPICAL MAXIMUM INPUT COUNT FREQUENCY of 32 MHz

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The T 74192 is an Up/Down BCD Decade Counter and the T 74193 is an Up/Down 4-bit Binary Counter. Both counters have separate up/down clocks, parallel load facility, terminal count outputs for multidecade operation and an asynchronous overriding master reset.
Available in standard temperature range (0 to 70°C) they come in 16-lead dual in-line plastic package.

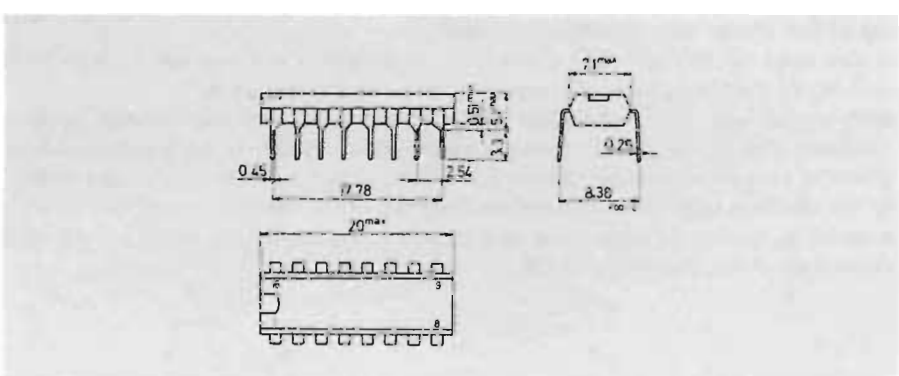
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBERS : T 74192 B1, T 74193 B1

MECHANICAL DATA

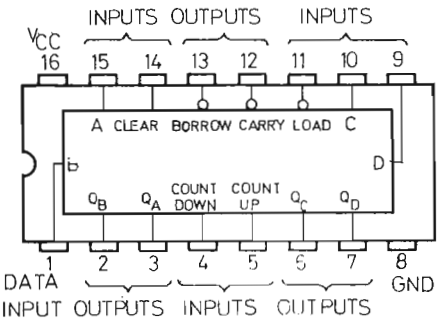
Dimensions in mm



11/73

T 74192
T 74193

CONNECTION DIAGRAM



S-0246

FUNCTIONAL DESCRIPTION

For both counters synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. The outputs of the four masters flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

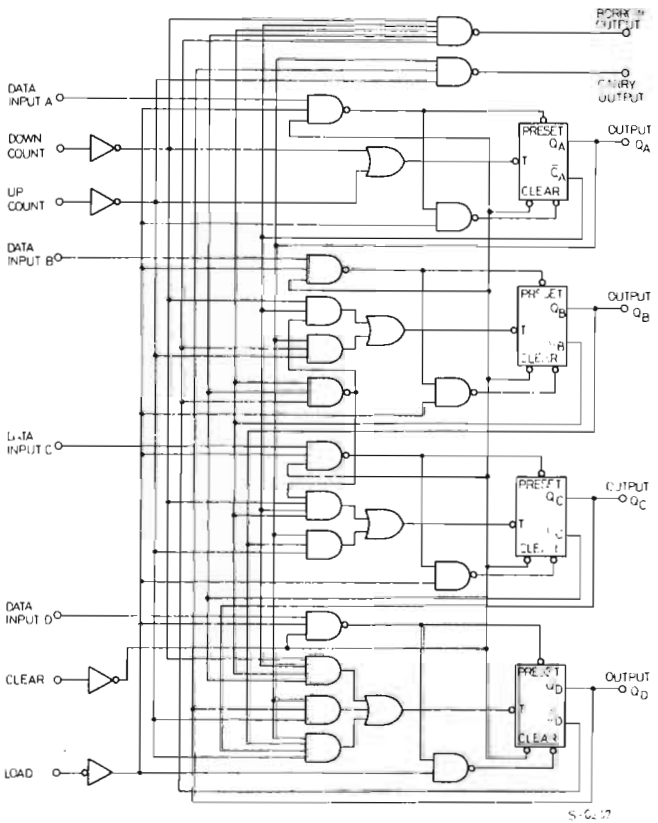
All these counters are fully programmable; the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. In this condition the outputs change independently of count pulses.

A clear input has been provided which forces all outputs to low level when a high level is applied; the clear function is independent of the count and load inputs.

Both borrow and carry outputs are available to cascade both the up/down counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter under flows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

FUNCTIONAL LOGIC DIAGRAMS

T 74192 decade counter.

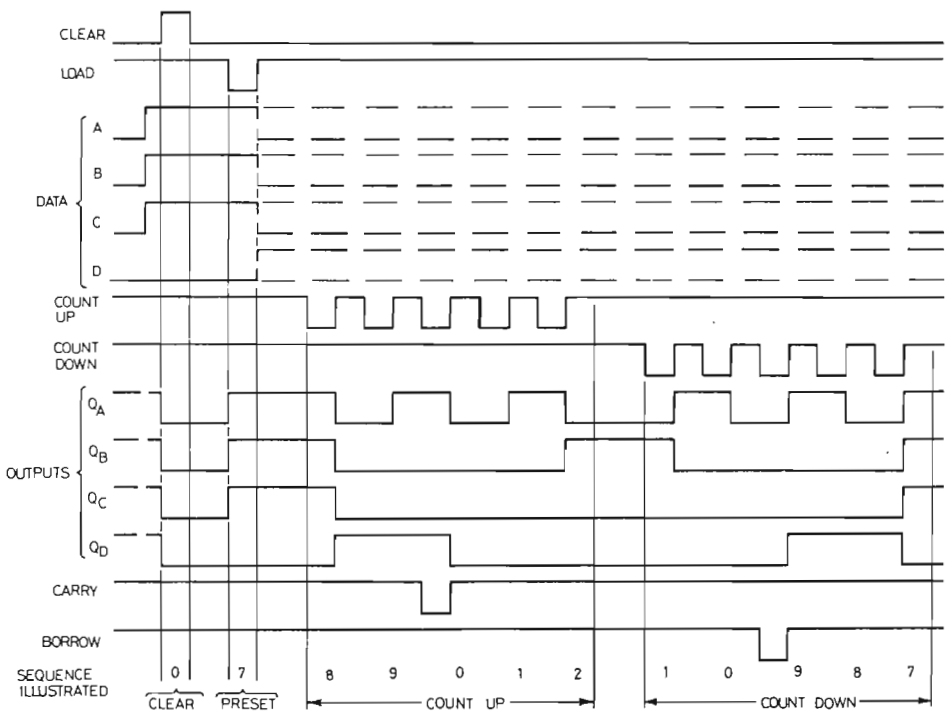


FUNCTIONAL LOGIC DIAGRAMS (continued)

T 74192 decade counters (typical clear, load, and count sequences)

Illustrated below is the following sequence:

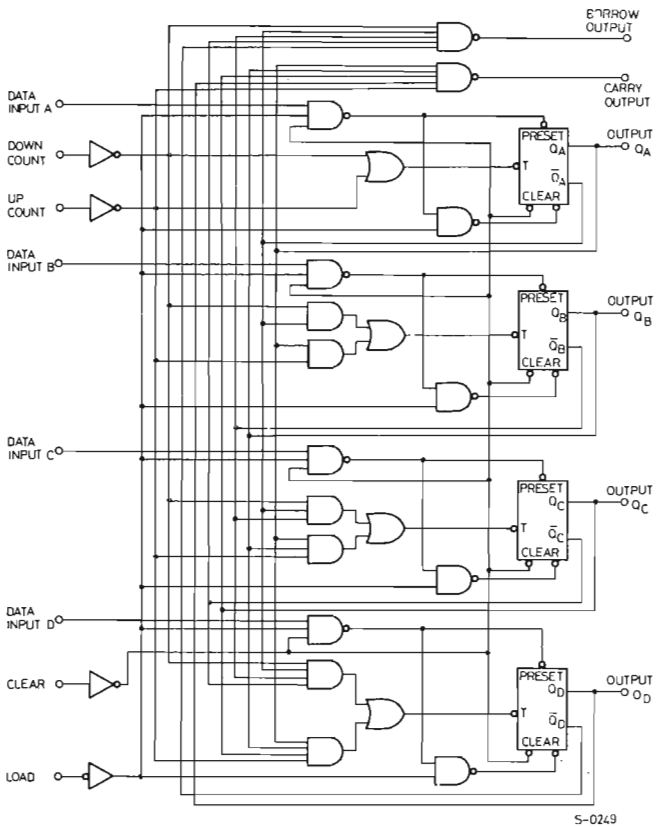
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: – Clear overrides load, data, and count inputs.
– When counting up, count down input must be high; when counting down, count-up input must be high.

FUNCTIONAL LOGIC DIAGRAMS (continued)

T 74193 binary counter.

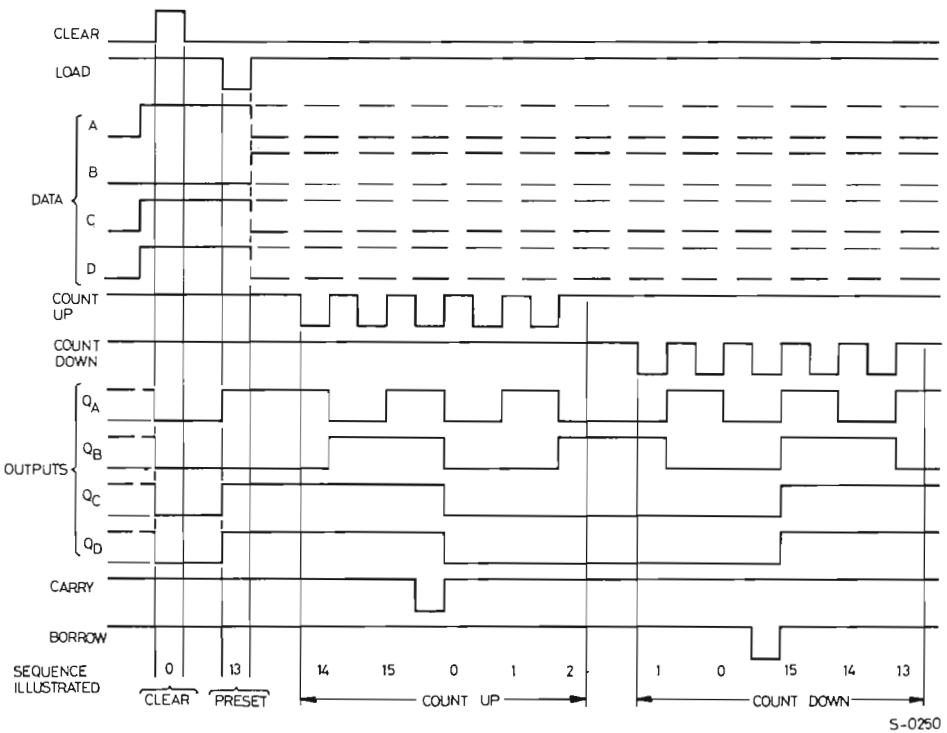


FUNCTIONAL LOGIC DIAGRAMS (continued)

T 74193 binary counters (typical clear, load, and count sequences)

Illustrated below is the following sequence :

1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: – Clear overrides load, data, and count inputs.
– When counting up, count-down input must be high; when counting down, count-up input must be high.

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
f_{count}	Input count frequency	0 to 25	MHz
t_{pw}	Pulse width (any input)	min. 20	ns
t_s	Set-up time (see note 1)	min. 20	ns
t_h	Hold time (see note 2)	min. 0	ns
N	Normalized fan-out from each output	max. 10	–
T_{op}	Operating temperature	0 to 70	°C

NOTES: 1) Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to insure its recognition.

2) Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test conditions	Min.	Typ.*	Max.	Unit	Fig.
V_{IH}	Input high voltage		2			V	1
V_{IL}	Input low voltage				0.8	V	1
V_{OH}	Output high voltage	V_{CC}=4.75V V_{IH}= 2V V_{IL}= 0.8V I_{OH}=-400μA	2.4			V	1
V_{OL}	Output low voltage	V_{CC}= 4.75V V_{IH}= 2V V_{IL}= 0.8V I_{OL}= 16mA			0.4	V	1
I_{IH}	Input high current	V_{CC}= 5.25V V_i= 2.4V V_{CC}= 5.25V V_i= 5.5V			40 1	μA mA	2
I_{IL}	Input low current	V_{CC}= 5.25V			-1.6	mA	2
I_{sc}**	Short-circuit current	V_{CC}= 5.25V	-18		-65	mA	3
I_{CC}	Supply current	V_{CC} = 5.25V		65	102	mA	2

* All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

** Not more than one output shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C, N = 10)

Parameter		Test conditions*		Min.	Typ.	Max.	Unit	Fig.
		from input	to output					
t_{pd1}	Propagation delay time to logical 1 level	Count-up	Carry		17	26	ns	7,8
t_{pd0}	Propagation delay time to logical 0 level				16	24	ns	
t_{pd1}	Propagation delay time to logical 1 level	Count-down	Borrow		16	24	ns	
t_{pd0}	Propagation delay time to logical 0 level				16	24	ns	
t_{pd1}	Propagation delay time to logical 1 level	Either count	Q		25	38	ns	
t_{pd0}	Propagation delay time to logical 0 level				31	47	ns	
t_{pd1}	Propagation delay time to logical 1 level	Load	Q		27	40	ns	4,5
t_{pd0}	Propagation delay time to logical 0 level				29	40	ns	
t_{pd0}	Propagation delay time to logical 0 level	Clear	Q		22	35	ns	

* See "Switching times test circuit and waveforms".

DC TEST CIRCUITS (Arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{IH}, V_{IL}, V_{OH}, V_{OL}.

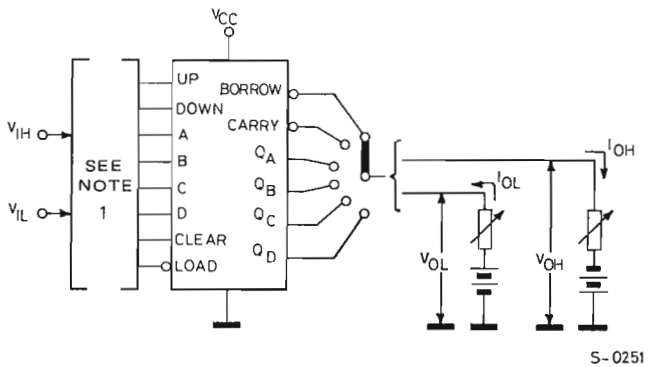


Fig. 2 - I_{IH}, I_{IL}, I_{CC}.

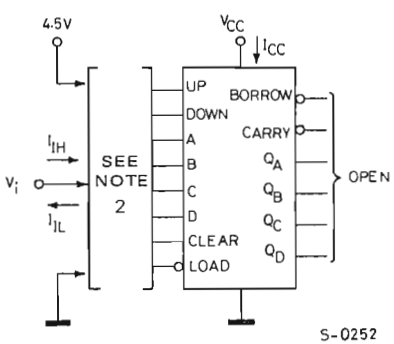
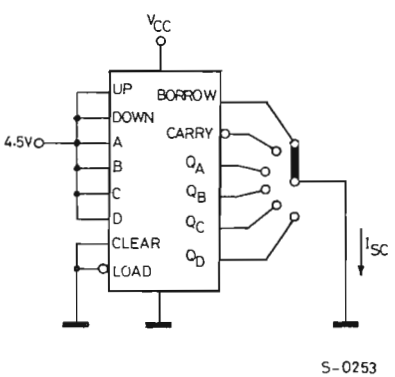


Fig. 3 - I_{sc} (see note 3).



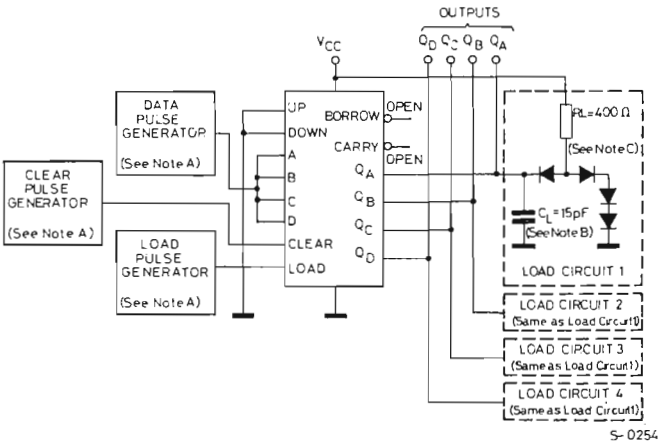
NOTES: 1) - Each output is tested separately.

2) - Each input is tested separately.
- When testing I_{IH}, apply V_i to input under test and ground other inputs except when testing data inputs, apply 4.5V to clear and load inputs.
- When testing I_{IL}, apply V_i to input under test and ground other inputs.
- When testing I_{CC} apply 4.5V to inputs; clear and load inputs are grounded.

3) - Each output is tested separately in the 1 level state.

SWITCHING TIMES

Fig. 4 - Clear, set-up and load times test circuit.

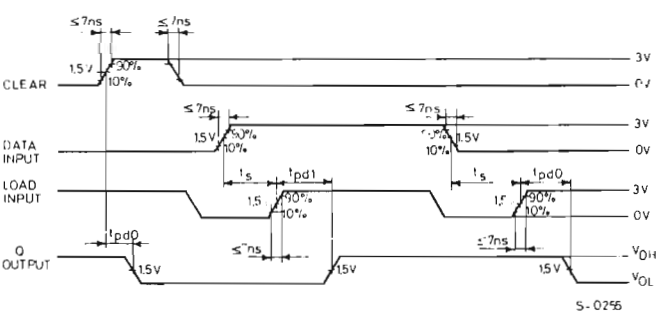


NOTES : A. The pulse generators have the following characteristics: $Z_O \approx 50\Omega$; for the data pulse generator, PRR = 500 kHz, duty cycle = 50%; for the load pulse generator, PRR = 1MHz, duty cycle = 50%.

B. C_L includes probe and jig capacitance.

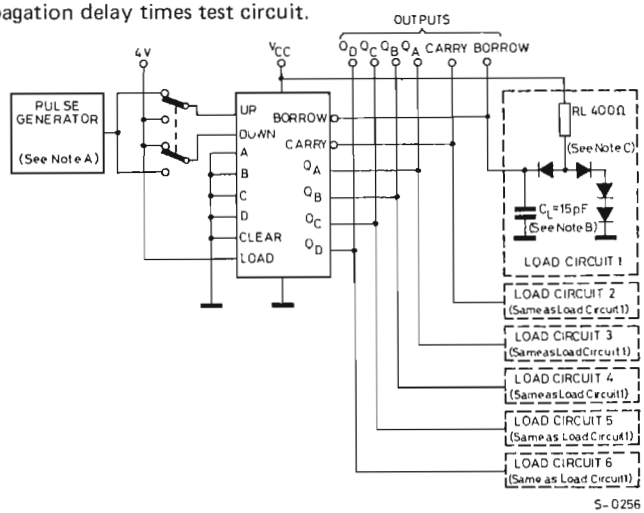
C. All diodes are 1N3064.

Fig. 5 - Clear, set-up and load times waveforms.



SWITCHING TIMES (continued)

Fig. 6 - Propagation delay times test circuit.



NOTES: A. The pulse generator has the following characteristics; PRR = 1 MHz, $Z_o \approx 50\Omega$, duty cycle = 50%.

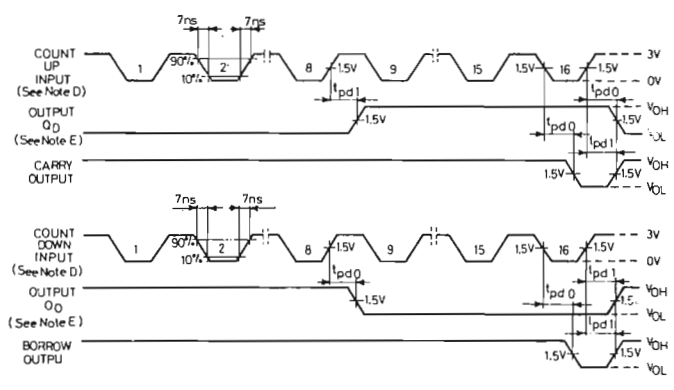
B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. Count-up and count-down pulses shown are for the T74193 binary counter. Count cycle for T74192 decade counter is 1 through 10.

E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.

Fig. 7 - Propagation delay times waveforms.

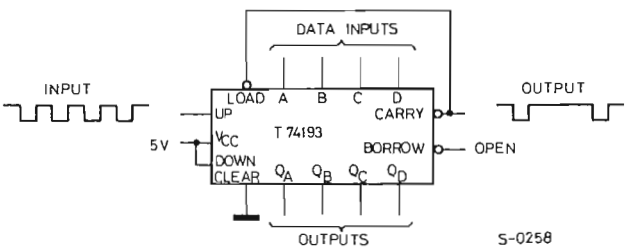


11/73

TYPICAL APPLICATION

Modulo-N divider

The T74193 can be used to divide an incoming count frequency by any integral number (N) from one to 16. This is done by modifying the count frequency occurring at the carry output by presetting the data inputs to 16 minus N. By connecting the carry output to the load input, the counter will count to the maximum state (15) and the data inputs will then be enabled on the succeeding clock pulse. The counter outputs are then preset to the levels applied at the data inputs and the count sequence is repeated.



The T74192 may be used in the same manner to perform division by any number from 1 to 10.

TTL INTEGRATED CIRCUITS

DUAL LINE RECEIVERS

- TTL COMPATIBLE
- HIGH INPUT IMPEDANCE
- LOW INPUTS CURRENTS
- USEFUL IN PARTY-LINE SYSTEM APPLICATIONS
- EXCELLENT INPUTS SENSITIVITY (3 mV TYP.)

The **T 75107A - T 75108A** and **T 75207A - T 75208A** line circuits are designed to detect low level differential input signals as 25 mV for (**T 75107A - T 75108A**), 10 mV for (**T 75207A - T 75208A**) amplitude and converter the polarity of the signals into appropriate TTL compatible output logic levels. There are dual line receivers featuring independent channels with common voltage supply and ground terminals. The **T 75107A - T 75207A** circuit features a TTL - compatible active pull up output, while the **T 75108A - T 75208A** circuit is also TTL compatible, sub features on open collector output.
The receivers feature independent strobe inputs for each channels and a strobe input common to both channels.
Available in standard temperature range (0 to 70°C), they come in 14-lead dual in-line plastic or ceramic package.

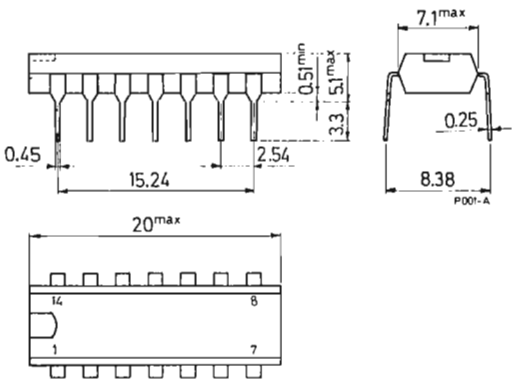
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i (D)	Differential input voltage	6	V
V_i (C)	Common - mode input voltage	5	V
V_i (S)	Strobe input voltage	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

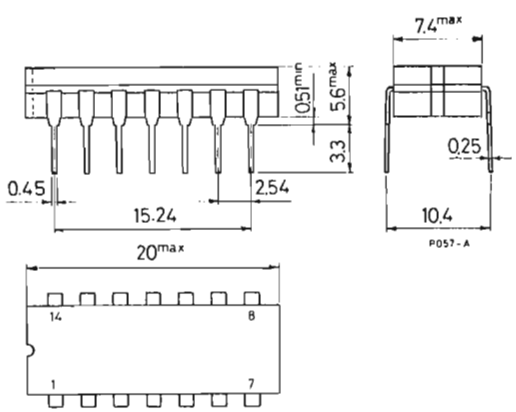
ORDERING NUMBERS : T 75XXXA B1 for dual in-line plastic package
T 75XXXA D1 for dual in-line ceramic package

MECHANICAL DATA (dimensions in mm)

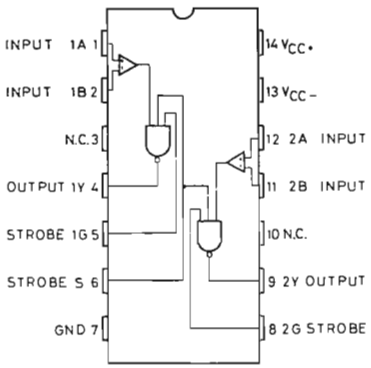
Dual in-line plastic package
for T 75XXXA B1



Dual in-line ceramic package
for T 75XXXA D1



CONNECTION DIAGRAM



TRUTH TABLE

DIFFERENTIAL INPUTS A - B		STROBES		OUTPUT
		G	S	Y
T 75107A T 75108A	**T 75207A T 75208A**			
$V_i \geqslant 25$ mV	$V_i \geqslant 10$ mV	X	X	H
-25 mV $\leqslant V_i \leqslant$ 25 mV	-10 mV $\leqslant V_i \leqslant$ 10 mV	X L H	L X H	H H INDETERMINATE
$V_i \leqslant$ -25 mV	$V_i \leqslant$ -10 mV	X L H	L X H	H H L

RECOMMENDED OPERATING CONDITIONS

V_{CC}+ *	Supply voltage	4.75 to 5.25	V
V_{CC} -*	Supply voltage	-4.75 to -5.25	V
V_i (D)	Differential input voltage	-5 to 5	V
V_i(C)*	Common-mode input voltage	-3 to 3	V
V_i*	Input voltage (any differential input)	-5 to 3	V

* This is measured with respect to the ground.

STATIC ELECTRICAL CHARACTERISTICS ($V_{CC}^+ = 5.25V$, $V_{CC}^- = -5.25V$ unless otherwise specified)

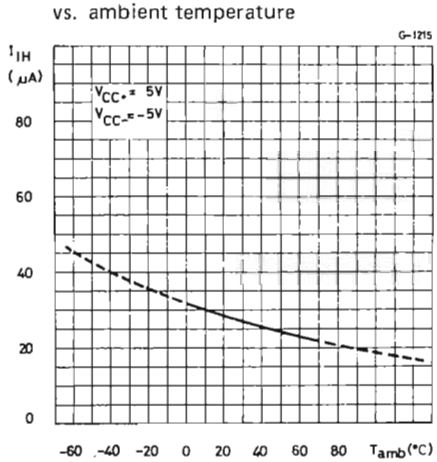
Parameter		Test conditions	Min.	Typ.*	Max.	Unit
V_{IH}	Input high voltage between differential inputs		0.025		5	V
V_{IL}	Input low voltage between differential inputs		-5		-0.025	V
$V_{IH}(S)$	Input high voltage at strobe inputs		2		5.5	V
$V_{IL}(S)$	Input low voltage at strobe inputs		0		0.8	V
V_{OH}	Output high voltage (**T75107A-T75207A** only)	$V_{CC}^+ = 4.75V$ $V_{CC}^- = -4.75V$ $I_{load} = -400\ \mu A$	2.4			V
V_{OL}	Output low voltage	$V_{CC}^+ = 4.75V$ $V_{CC}^- = -4.75V$ $I_{sink} = 16$ mA			0.4	V
$I_{IH}(D)$	Input high current into differential 1A or 2A	$V_i(D) = 0.5V$ $V_i(C) = -3V$ to $3V$		30	75	μA
$I_{IL}(D)$	Input low current into differential 1A or 2A	$V_i(D) = -2V$ $V_i(C) = -3V$ to $3V$			-10	μA
$I_{IH}(S)$	Input high current into strobe 1G or 2G	$V_{IH}(S) = 2.4V$			40	μA
		$V_{IH}(S) = 5.25V$			1	mA
$I_{IL}(S)$	Input low current into strobe 1G or 2G	$V_{IL}(S) = 0.4V$			-1.6	mA
$I_{IH}(S)$	Input high current into strobe S	$V_{IH}(S) = 2.4V$			80	μA
		$V_{IH}(S) = 5.25V$			2	mA
$I_{IL}(S)$	Input low current into strobe S	$V_{IL}(S) = 0.4V$			-3.2	mA
I_{SC} **	Short-circuit current (**T75107A-T75207A** only)		-18		-70	mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

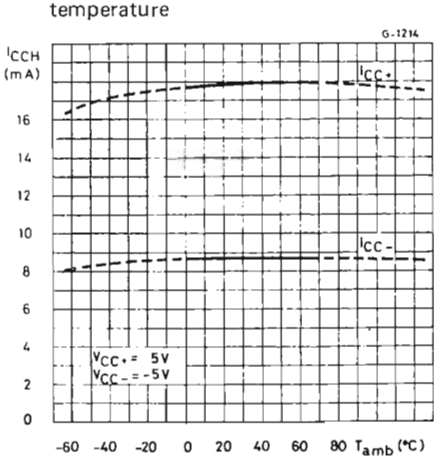
Parameter	Test conditions	Min.	Typ.*	Max.	Unit
$I_{CCH}+$ Supply current from $V_{CC}+$	$V_i(D)= 25mV$ $V_{IH}(S)= 5V$ $T_{amb}= 25°C$		18	30	mA
$I_{CCH}-$ Supply current from $V_{CC}-$	$V_i(D)= 25mV$ $V_{IH}(S)= 5V$ $T_{amb}= 25°C$		-8.4	-15	mA
I_{sink} Sinking current				16	mA
I_{load} Load current				-400	μA

* All typical values are at $V_{CC}+ = 5V$, $V_{CC}- = -5V$, $T_{amb} = 25°C$.
** Not more than one output should be shorted at a time.

Typical input current into 1A or 2A vs. ambient temperature

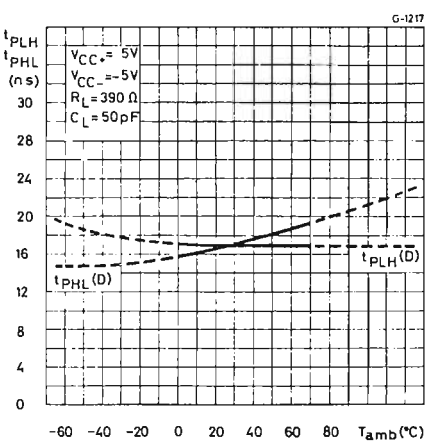


Typical supply current vs. ambient temperature



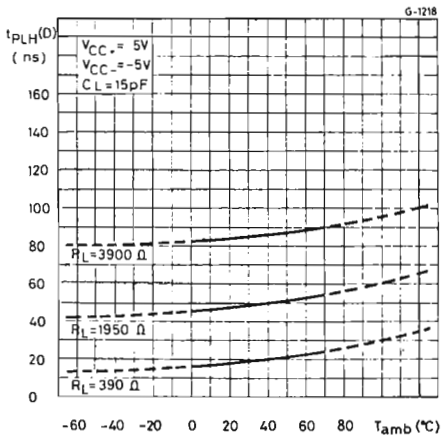
DYNAMIC ELECTRICAL CHARACTERISTICS ($V_{CC}^+ = 5V$, $V_{CC}^- = -5V$, $R_L = 390\Omega$, $T_{amb} = 25°C$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}(D) Propagation delay time, from differential inputs A and B to output	$C_L = 15$ pF for **T 75108A - T 75208A**		19	25	nsec
	$C_L = 50$ pF for **T 75107A - T 75207A**		17	25	nsec
t_{PHL}(D) Propagation delay time, from differential inputs A and B to output	$C_L = 15$ pF for **T 75108A - T 75208A**		19	25	nsec
	$C_L = 50$ pF for **T 75107A - T 75207A**		17	25	nsec
t_{PLH}(S) Propagation delay time, from strobe input G or S to output	$C_L = 15$ pF for **T 75108A - T 75208A**		13	20	nsec
	$C_L = 50$ pF for **T 75107A - T 75207A**		10	15	nsec
t_{PHL}(S) Propagation delay time, from strobe input G or S to output	$C_L = 15$ pF for **T 75108A - T 75208A**		13	20	nsec
	$C_L = 50$ pF for **T 75107A - T 75207A**		8	15	nsec

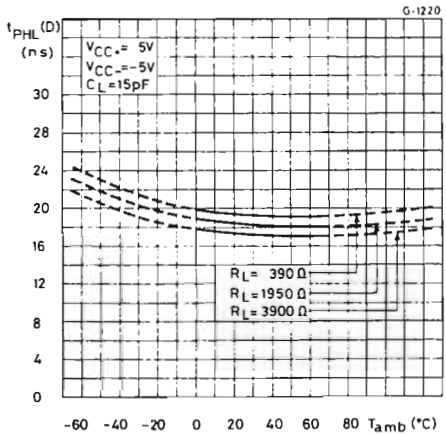


Typical propagation delay time (differential inputs) vs. ambient temperature (for **T 75107A-T 75207A** only)

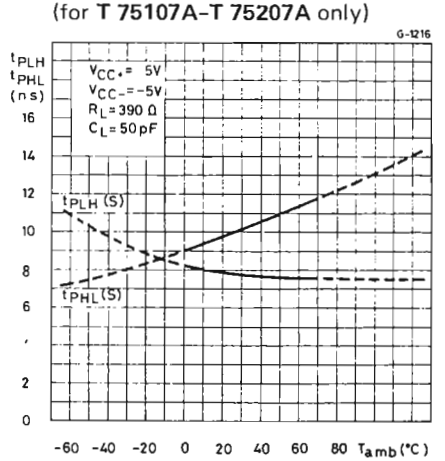
Typical propagation delay time (differential inputs) vs. ambient temperature (for **T 75108A-T 75208A** only)



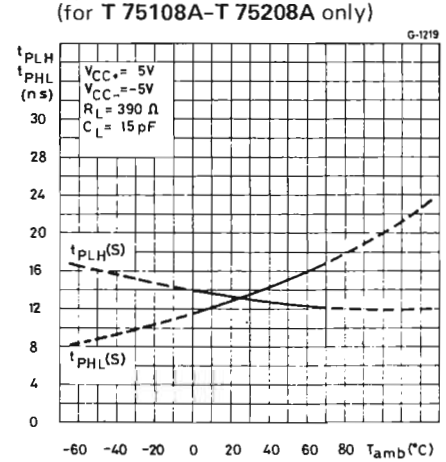
Typical propagation delay time (differential inputs) vs. ambient temperature (for **T 75108A-T 75208A** only)



Typical propagation delay time (strobe inputs) vs. ambient temperature (for **T 75107A-T 75207A** only)

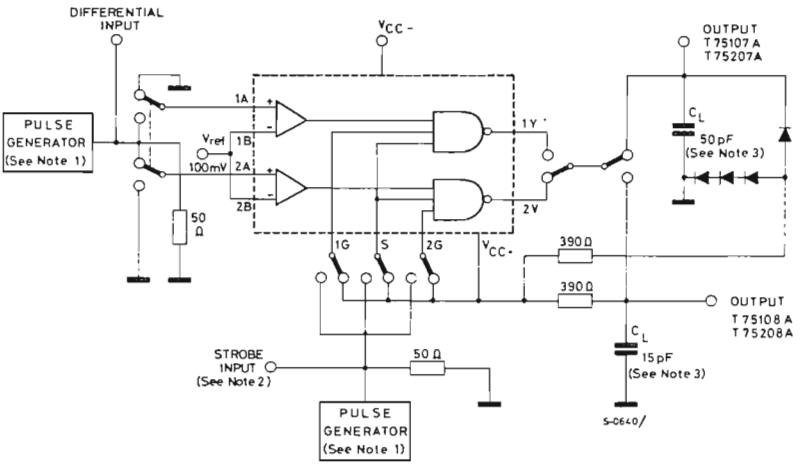


Typical propagation delay time (strobe inputs) vs. ambient temperature (for **T 75108A-T 75208A** only)



SWITCHING TIMES

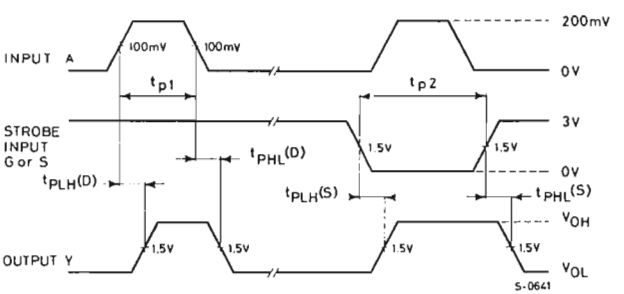
Test circuit.



NOTES: 1. The pulse generators have the following characteristics: $Z_{out} = 50\ \Omega$ $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz $t_{p2} = 1\ \mu$s, PRR = 500 kHz.

2. Strobe input pulse is applied to Strobe 1G when inputs 1A–1B are being tested, to Strobe S when inputs 1A–1B or 2A–2B are being tested, and to Strobe 2G when inputs 2A–2B are being tested.
3. C_L includes probe and jig capacitance.

Waveforms



T 75109
T 75110

DUAL LINE DRIVERS

- HIGH SPEED DATA-TRASMISSION
- TTL COMPATIBLE

The T **75109** and T **75110** are dual line drivers featuring independent channels with common supply voltage and ground terminals.
The difference between the two drivers is in the output current specification, it is nominally 6 mA for the T **75109** and 12 mA for the T **75110**.
The output current can be inhibited by appropriate logic levels on the inhibit inputs. This device is available in 14 lead dual in-line plastic and ceramic package for a standard temperature range (0 to 70°C).

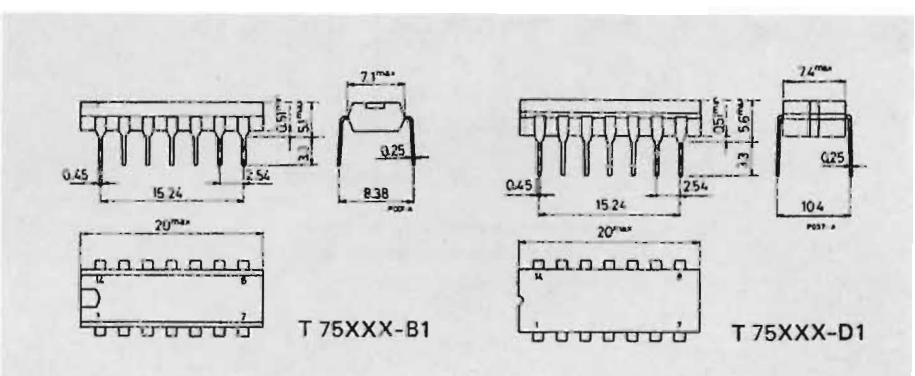
ABSOLUTE MAXIMUM RATINGS

$V_{CC}+$	Supply voltage	7	V
$V_{CC}-$	Supply voltage	-7	V
V_i	Input voltage	5.5	V
V_o	Common-mode output voltage	- 5 to 12	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBERS: T 75 XXX - B1 for dual in-line plastic package
T 75 XXX - D1 for dual in-line ceramic package

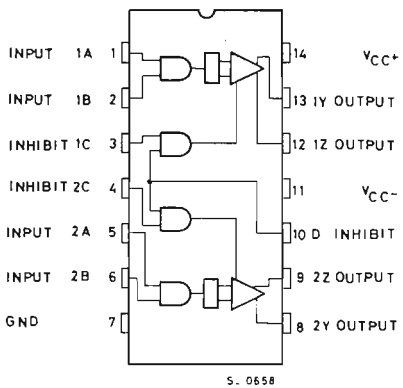
MECHANICAL DATA

Dimensions in mm



T 75109
T 75110

CONNECTION DIAGRAM



TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	H	H
X	X	X	L	H	H
L	X	H	H	L	H
X	L	H	H	L	H
H	H	H	H	H	L

L = Low output represents the on state
H = High output represents the off state
X = Either High or Low

RECOMMENDED OPERATING CONDITIONS*

$V_{CC}+$	Supply voltage	4.75 to 5.25	V
$V_{CC}-$	Supply voltage	-4.75 to -5.25	V
V_o	Positive common mode output voltage	0 to 10	V
V_o	Negative common mode output voltage	0 to -3	V

*These are measured with respect to the ground

STATIC ELECTRICAL CHARACTERISTICS ($V_{CC}^+ = 5.25V$, $V_{CC}^- = -5.25V$ unless otherwise specified)

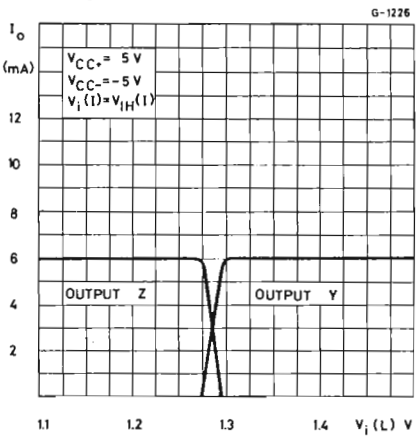
Parameter		Test conditions	Min.	Typ.*	Max.	Unit
V_{IH}	Input high voltage at any input		2		5.5	V
V_{IL}	Input low voltage at any input		0		0.8	V
$I_{IH}(L)$	Input high current into logic 1A, 1B, 2A or 2B	$V_{IH}(L) = 2.4V$			40	μA
		$V_{IH}(L) = 5.25V$			1	mA
$I_{IL}(L)$	Input low current into logic 1A, 1B, 2A or 2B	$V_{IL}(L) = 0.4V$			-3	mA
$I_{IH}(I)$	Input high current into inhibit 1C or 2C	$V_{IH}(I) = 2.4V$			40	μA
		$V_{IH}(I) = 5.25V$			1	mA
$I_{IL}(I)$	Input low current into inhibit 1C or 2C	$V_{IL}(I) = 0.4V$			3	mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

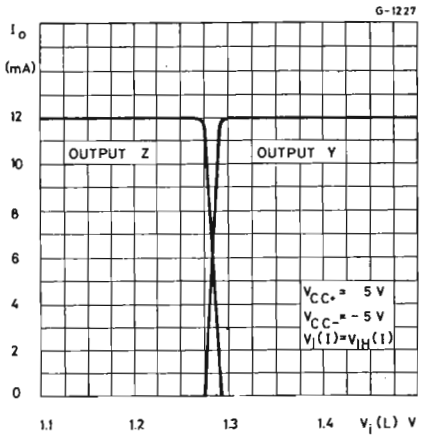
Parameter		Test conditions	Min.	Typ.*	Max.	Unit
I_{IH} (I)	Input high current into inhibit D	V_{IH}(I) = 2.4V			80	µA
		V_{IH}(I) = 5.25V			2	mA
I_{IL} (I)	Input low current into inhibit D	V_{IL}(I) = 0.4V			-6	mA
I_O	Output current into on-state	for **T 75109**			7	mA
		for **T 75110**			15	mA
		V_{CC}= 4.75V V_{CC}=-5.25V for **T 75109**	3.5			mA
		V_{CC}=4.75V V_{CC}=-5.25V for **T 75110**	6.5			mA
I_O	Output current into off-state				100	µA
I_{CC}^+	Supply current with driver enabled into on-state	V_{IH}(I) = 2V V_{IL}(L)=0.4V for **T 75109**		18	30	mA
		for **T 75110**		23	50	mA
I_{CC}^-	Supply current with driver enabled into on-state	V_{IH}(I) = 2V V_{IL}(L)=0.4V for **T 75109**		-18	-30	mA
		for **T 75110**		-34	-50	mA
I_{CC}^+	Supply current with driver inhibited into off-state	V_{IL}(I) = 0.4V V_{IL}(L)=0.4V for **T 75109**		18		mA
		for **T 75110**		21		mA
I_{CC}^-	Supply current with driver inhibited into off-state	V_{IL}(I) = 0.4V V_{IL}(L)=0.4V for **T 75109**		-10		mA
		for **T 75110**		-17		mA

* All typical values are at $V_{CC}^+ = 5V$, $V_{CC}^- = -5V$, $T_{amb} = 25°C$

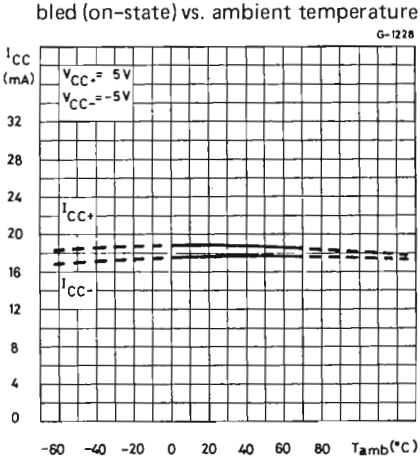
Typical output current vs. logic input voltage



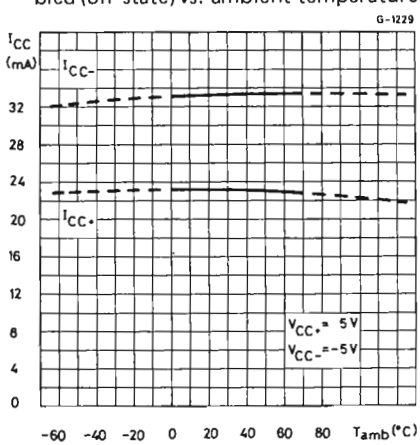
Typical output current vs. logic input voltage



Typical supply current with driver enabled (on-state) vs. ambient temperature



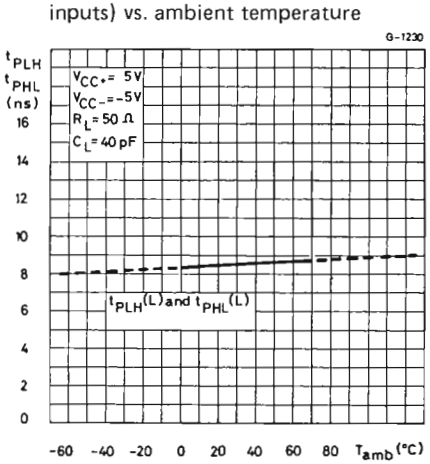
Typical supply current with driver enabled (on-state) vs. ambient temperature



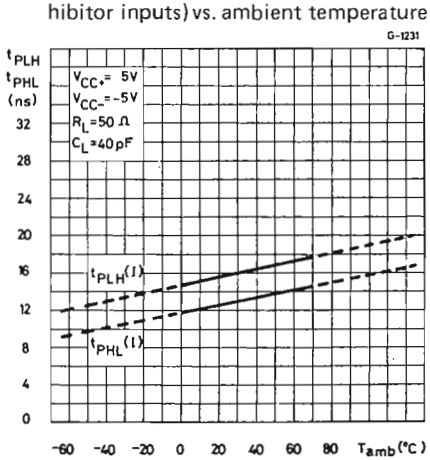
DYNAMIC ELECTRICAL CHARACTERISTICS (V_{CC}^+=5V, V_{CC}^-=-5V, R_L=50 Ω, T_{amb} = 25°C)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PLH} (L) Propagation delay time from logic input A or B to output Y or Z	C_L = 40 pF		9	15	nsec
t_{PHL} (L) Propagation delay time from logic input A or B to output Y or Z	C_L = 40 pF		9	15	nsec
t_{PLH} (I) Propagation delay time from inhibitor input C or D to output Y or Z	C_L = 40 pF		16	25	nsec
t_{PHL} (I) Propagation delay time from inhibitor input C or D to output Y or Z	C_L = 40 pF		13	25	nsec

Typical propagation delay time (logic inputs) vs. ambient temperature

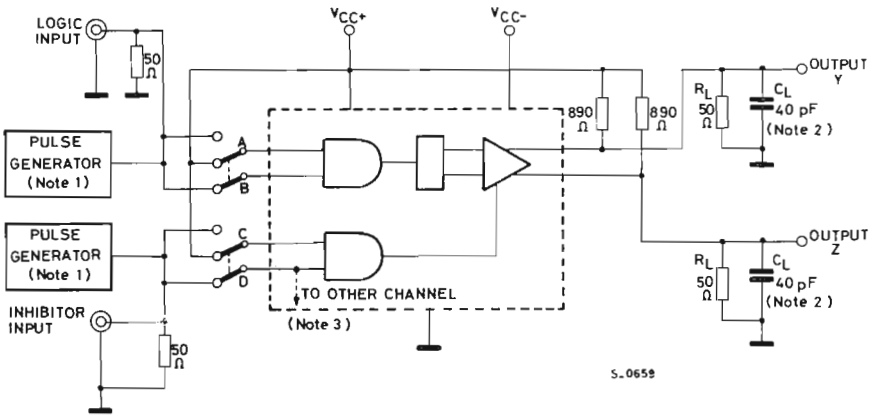


Typical propagation delay time (inhibitor inputs) vs. ambient temperature



SWITCHING TIMES

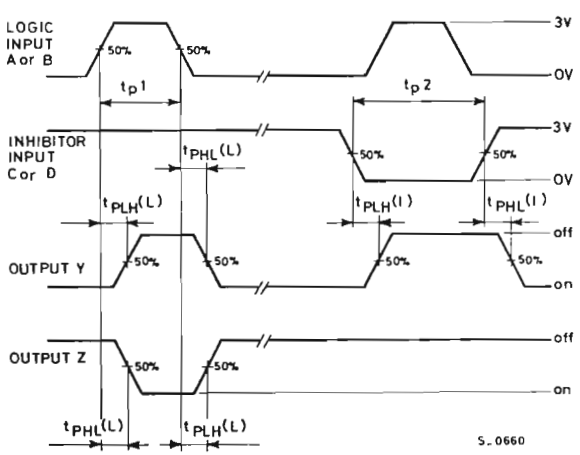
Test circuit



NOTES:

1. The pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 10 \pm 5$ns, $t_{p1} =$ 500ns, PRR = 1MHz, $t_{p2} = 1$ ms, PRR = 500kHz
2. C_L includes probe and jig capacitance
3. For simplicity, only one channel and the inhibitor connections are shown

Waveforms



Dual peripheral positive AND driver

STANDARD TEMPERATURE RANGE
0°C to 70°C

- OUTPUT CURRENT CAPABILITY 300mA
- HIGH-VOLTAGE OUTPUTS
- HIGH-SPEED SWITCHING
- CIRCUIT FLEXIBILITY FOR VARIED APPLICATIONS
- TTL OR DTL COMPATIBLE DIODE-CLAMPED INPUTS
- STANDARD SUPPLY VOLTAGE
- 8-PIN PLASTIC DIP

ORDERING NUMBER : T 75451A B1

The T 75451A is a dual peripheral driver designed for use in systems that employ TTL and DTL logic. Typical applications include high speed logic buffer, power driver, relay driver, lamp driver, MOS driver and memory driver. The T 75451A offers large freedom from latch-up, diode-clamped inputs to simplify system design and can drive lamps, relays, and memories to rated levels of voltage and current without external loading capacitors. The device is available in eight pin plastic mini-DIP.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

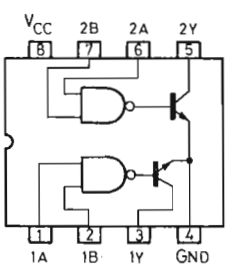
Supply Voltage V_{CC} (1)	7V
Input Voltage V_{in} (1 and 2)	5.5V
Intermitter Voltage (3)	5.5V
Continuous Output Current (5)	300 mA
Continuous Total Power Dissipation	800 mW
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

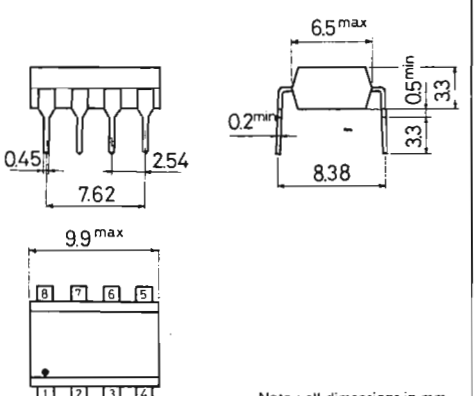
Supply Voltage V_{CC} (1)	4.75V to 5.25V
Maximum Voltage on any Output (1 and 4)	30V
Free-Air Temperature Range	0°C to 70°C

NOTES : see next page.

CONNECTION DIAGRAM



PHYSICAL DIMENSIONS
8-pin plastic DIP
(MINI DIP)



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on) level at output	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off) level at output	V_{CC} = MIN			0.8	V
V_c	Input clamp voltage	V_{CC} = MIN I_C = -12mA			- 1.5	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN V_{in} = 2V $V_{out(1)}$ = 30V			100	µA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN V_{in} = 0.8V I_{sink} = 100mA			0.4	V
		V_{CC} = MIN V_{in} = 0.8V I_{sink} = 300mA			0.7	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX V_{in} = 0.4V			- 1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{in} = 2.4V			40	µA
		V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX V_{in} = 0		52	65	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX V_{in} = 5V		7	11	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Uni
t_{pd0}	Propagation delay time to logical 0 level	$I_{sink} \approx$ 200mA C_L = 15pF R_L = 50Ω		45		ns
t_{pd1}	Propagation delay time to logical 1 level			25		ns
t_{T0}	Transition time, high-to-low level output			12		ns
t_{T1}	Transition time, low-to-high level output			10		ns

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

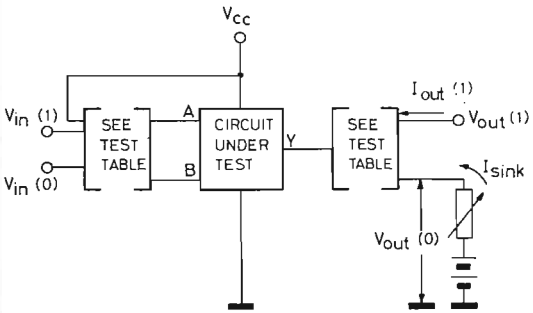
(**) All typical values at V_{CC} = 5V, T_A = 25°C.

NOTES :

1) These voltage values are with respect to network ground terminal unless otherwise specified.
2) Input signals must be zero or positive with respect to network ground terminal.
3) This is the voltage between two emitters of a multiple emitter transistor.
4) This is the maximum voltage which should be applied to any output when it is in the off state.
5) Both halves of this dual circuit may conduct rated current simultaneously.

DC TEST CIRCUITS (arrows indicate actual direction of current flow. Current into a terminal is a positive value)

$V_{in(1)} - V_{in(0)} - I_{out(1)} - V_{out(0)}$ TEST CIRCUIT

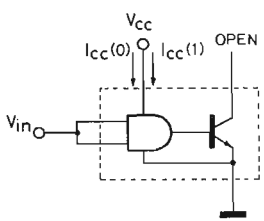


TEST TABLE

INPUT UNDER TEST	OTHER INPUT	OUTPUT	
		APPLY	MEASURE
$V_{in(1)}$	$V_{in(1)}$	$V_{out(1)}$	$I_{out(1)}$
$V_{in(0)}$	V_{CC}	I_{out} (0)	$V_{out(0)}$

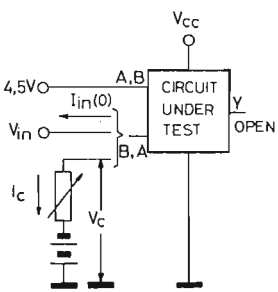
Note : Each input is tested separately

$I_{CC(0)}$ - $I_{CC(1)}$ TEST CIRCUIT



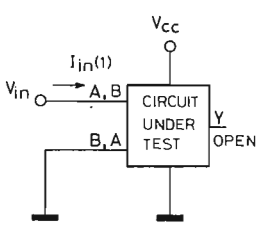
Note : Both gates are tested simultaneously

V_C - $I_{in(0)}$ TEST CIRCUIT



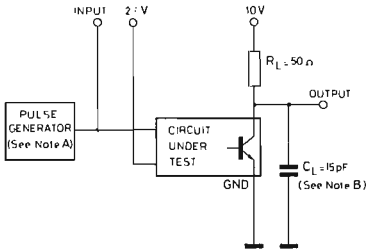
Note : Each input is tested separately

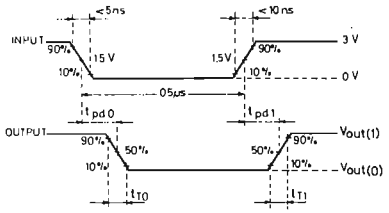
$I_{in(1)}$ TEST CIRCUIT



Note : Each input is tested separately

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

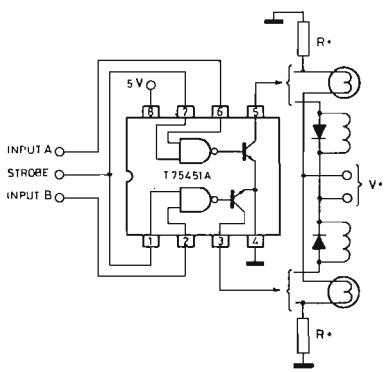




Notes :
A) The pulse generator has the following characteristics : PRR = 1 MHz, $Z_{out} \approx 50\Omega$
B) C_L includes probe and jig capacitance.

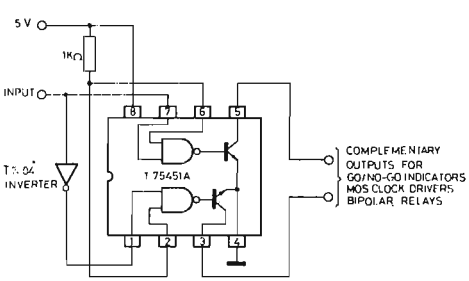
TYPICAL APPLICATION DATA

A) DUAL LAMP OR RELAY DRIVER



Note: Optional keep alive resistors, maintain off-state lamp current at ≈ 10% to reduce surge current.

B) COMPLEMENTARY DRIVER



PRELIMINARY DATA

HIGH - SPEED TRANSISTOR - TRANSISTOR LOGIC

- HIGH-SPEED-TYPICAL GATE PROPAGATION DELAY TIMES: 6 ns at $C_L = 25$ pF
- HIGH DC NOISE IMMUNITY: 1V (TYP.)
- LOW OUTPUT IMPEDANCE
- POWER DISSIPATION: 23 mW (TYP.) per NAND GATE at 50% DUTY CYCLE
- FANOUT: 10 SERIES T54H/74H or 12 SERIES T54/74 LOADS
- COMPATIBLE WITH STANDARD SERIES T54/74 LOGIC CIRCUITS
- ALL INPUTS ARE DIODE CLAMPED to MINIMIZE TRASMISSION LINE EFFECTS
- MULTIFUNCTION GATES and DUAL FLIP-FLOPS OFFER LOW COST per FUNCTION
- SPECIAL CIRCUIT TYPES (AND and AND-OR FUNCTIONS) REDUCE SYSTEM PACKAGE COUNT

Series **T54H** and **T74H TTL** integrated circuits are designed to be used in very high speed digital system.
This logic series includes the gates and flip-flop elements needed to perform all functions within general purpose digital system.
Serie **T54H** and **T74H** circuits feature a darlington-connected, double-ended, high-speed output for improved switching speeds. Typical flip-flop clock frequencies are 30 and 50 MHz.
Series **T54H** are integrated circuits available in 14 or 16 - lead dual in-line ceramic package.
Series **T74H** are integrated circuits available in 14 or 16 - lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS

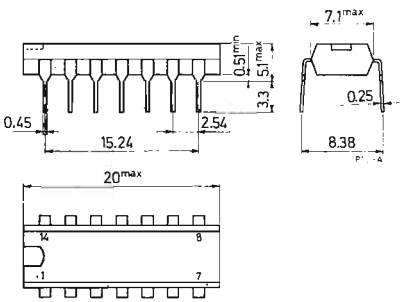
V_{CC}	Supply voltage		7	V
V_i	Input voltage		5.5	V
T_{stg}	Storage temperature		-65 to 150	°C
T_{op}	Operating temperature:	for **T54H** type	-55 to 125	°C
		for **T74H** types	0 to 70	°C

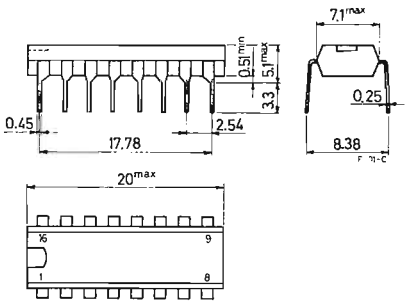
ORDERING NUMBERS:

T54H XX D2 for dual in-line ceramic package
T74H XX B1 for dual in-line plastic package
T74H XX D1 for dual in-line ceramic package

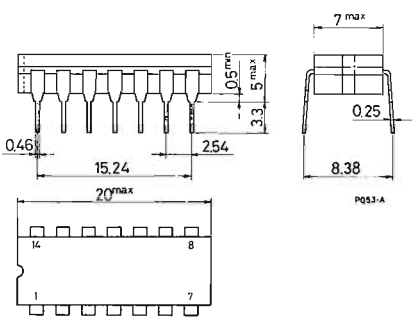
MECHANICAL DATA (dimensions in mm)

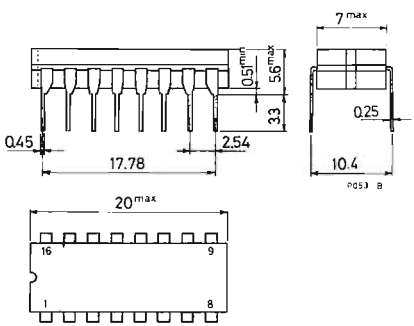
Dual in-line plastic packages: for T74H XX B1





Dual in-line ceramic packages: for T74H XX D1
for T54H XX D2





RECOMMENDED OPERATING CONDITIONS

V_{CC}*	Supply voltage: for **T54H** type	4.5 to 5.5	V
	for **T74H** types	4.75 to 5.25	V
N	Normalized fanout (each output)	max 10	
T_{op}	Temperature range: for **T54H** type	-55 to 125	°C
	for **T74H** types	0 to 70	°C

* These are measured with respect to the ground

OPERATING CONSIDERATIONS

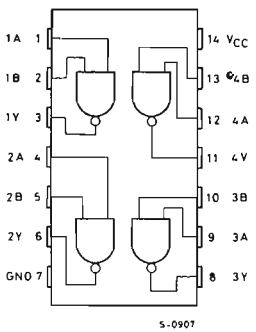
UNUSED INPUTS OF NAND AND GATES: for optimum switching times and minimum noise susceptibility unused inputs should be mantained at a positive voltage into 2.4 V and not more than 5.5 V.
FANOUT CAPABILITY: fanout (N) reflects the ability of an output to sink current from a number of Series **T54H** or **T74H** loads at logical 0 voltage level and to supply current at a logical 1 voltage level.
LOGIC DEFINITION: Series T**54H** and T**74H** logic is defined in terms of standard POSITIVE LOGIC.

TYPE DESCRIPTIONS

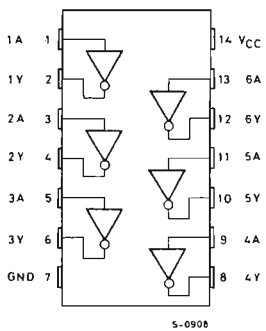
T 54/74 H 00 Quad 2-input positive NAND gate
T 54/74 H 01 Quad 2-input NAND gate with open collector
T 54/74 H 04 Hex inverter
T 54/74 H 05 Hex inverter with open collector
T 54/74 H 10 Triple 2-input positive NAND gate
T 54/74 H 11 Triple 3-input positive AND gate
T 54/74 H 20 Dual 4-input positive NAND gate
T 54/74 H 21 Dual 4-input AND gate
T 54/74 H 22 Dual 4-input NAND gate with open collector
T 54/74 H 30 8-input NAND gate
T 54/74 H 40 Dual 4-input positive NAND buffer
T 54/74 H 50 Exp. dual 2-wide 2-input AND-OR INVERT gate
T 54/74 H 51 Dual 2-wide 2-input AND-OR-INVERT gate
T 54/74 H 52 Exp. 2-2-2-3 input AND-OR gate
T 54/74 H 53 Exp. 2-2-2-3 input AND-OR-INVERT gate
T 54/74 H 54 Dual 2-wide 2-input AND-OR-INVERT gate
T 54/74 H 60 Dual 4-input expander
T 54/74 H 61 Triple 3-input expander
T 54/74 H 62 3-2-2-3 input AND-OR expander
T 54/74 H 71 JK master-slave flip-flop
T 54/74 H 72 JK master-slave flip-flop

CONNECTION DIAGRAMS

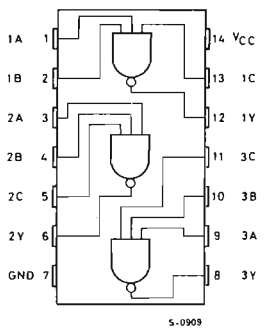
T 54/74 H 00
T 54/74 H 01



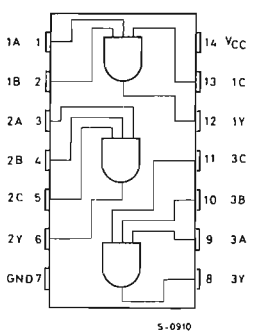
T 54/74 H 04
T 54/74 H 05



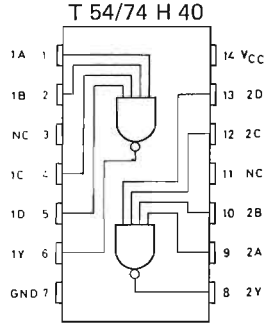
T 54/74 H 10



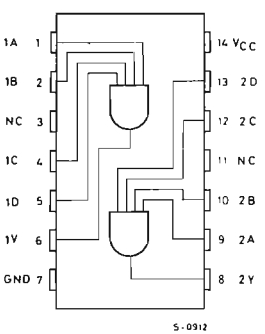
T 54/74 H 11



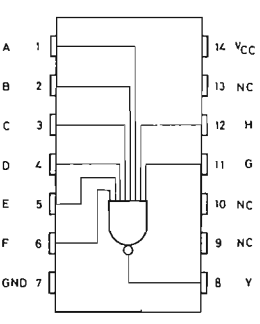
T 54/74 H 20
T 54/74 H 22
T 54/74 H 40



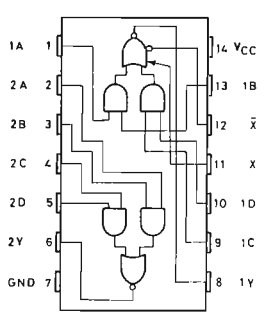
T 54/74 H 21



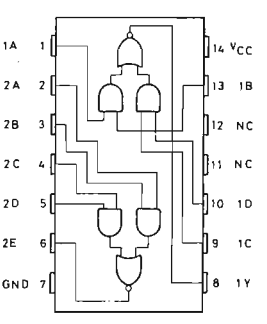
T 54/74 H 30



T 54/74 H 50

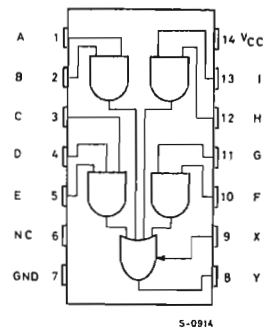


T 54/74 H 51



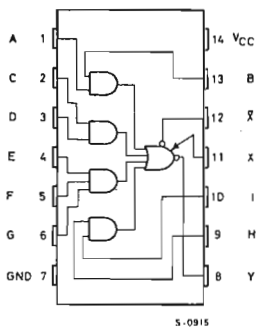
CONNECTION DIAGRAMS (continued)

T 54/74 H 52



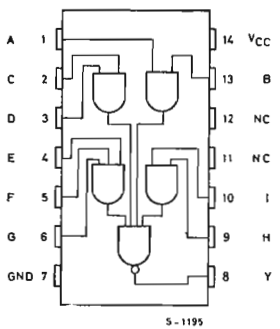
S-0914

T 54/74 H 53



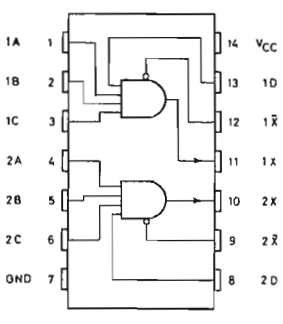
S-0915

T 54/74 H 54



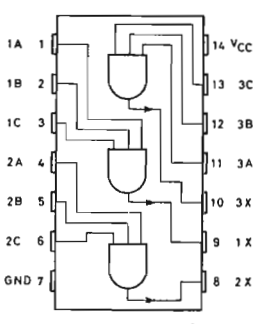
S-1195

T 54/74 H 60



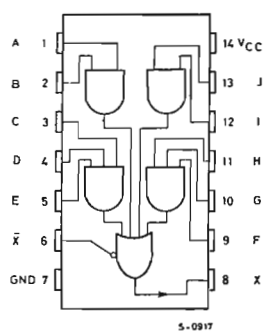
S-1196

T 54/74 H 61



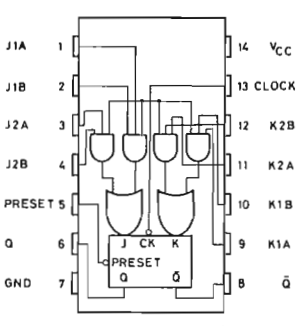
S-0916

T 54/74 H 62



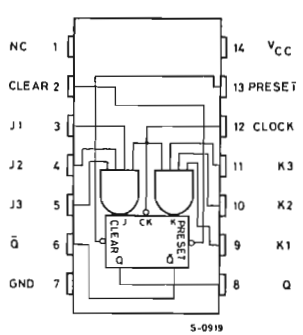
S-0917

T 54/74 H 71



S-0918

T 54/74 H 72



S-0919

HLL INTEGRATED CIRCUITS

HLL INTEGRATED CIRCUITS

E. = Extended temperature range
I. = Intermediate temperature range
S. = Standard temperature range

High level logic family

EXTENDED TEMPERATURE RANGE
-55°C to 125°C

- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY 5V (TYP.) at V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS and COS/MOS IC's

High Level Logic is a family of high threshold integrated circuits.
It offers the advantages of 5V DC noise immunity, high signal levels, large supply voltage tolerances and unusually high fan-out.
These features make the family particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.
The H100 series elements are available in the hermetically sealed ceramic dual in-line package.

ABSOLUTE MAXIMUM RATINGS

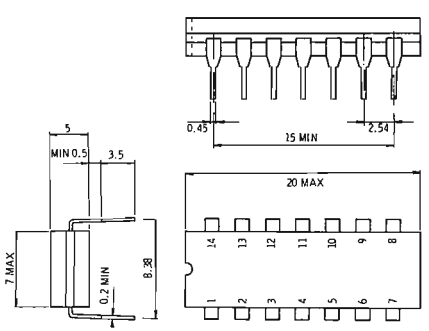
Supply Voltage (V_{CC}) continuous			18V
Input Voltage	-0.5	to	16V
Storage Temperature Range	-65°C	to	150°C

OPERATING CONDITIONS

Operating Temperature	-55°C	to	125°C
Supply Voltage	10.8V	to	16V

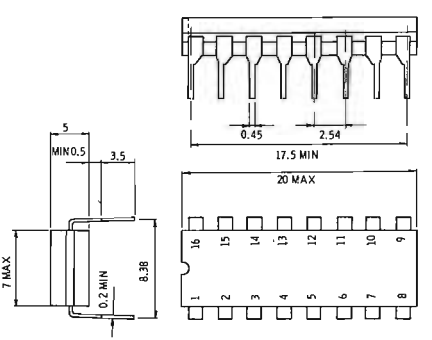
ORDERING NUMBER
H1XX D2

PHYSICAL DIMENSIONS
14-pin ceramic package



NOTE: all dimensions in mm.

PHYSICAL DIMENSIONS
16-pin ceramic package

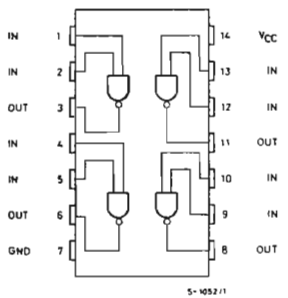


NOTE: all dimensions in mm.

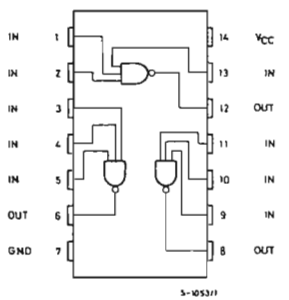
EXTENDED TEMPERATURE RANGE

CONNECTION DIAGRAMS

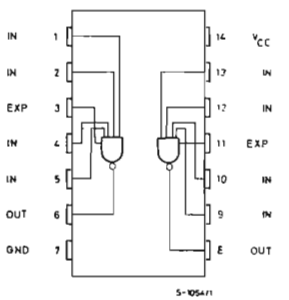
H 102/H 122



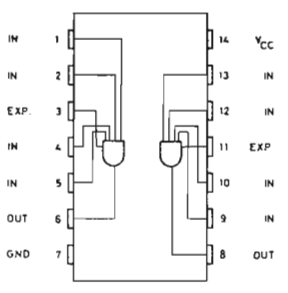
H 103



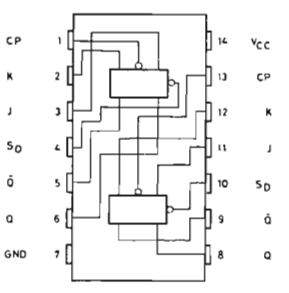
H 104/H 124



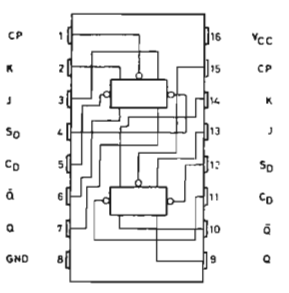
H 109



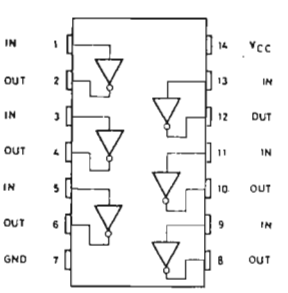
H 110



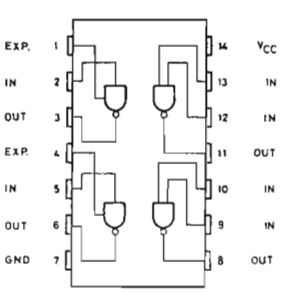
H 111



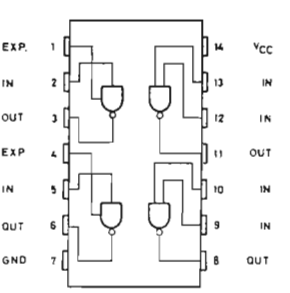
H 112



H 113

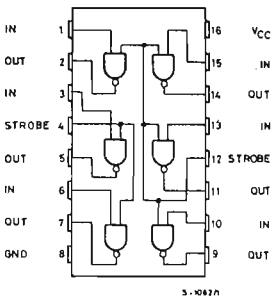


H 114

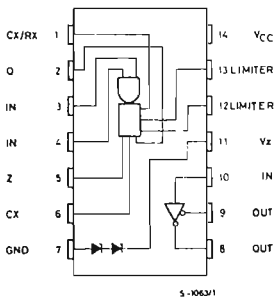


CONNECTION DIAGRAMS (continued)

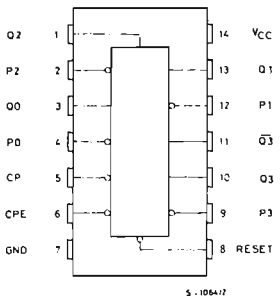
H115



H 117

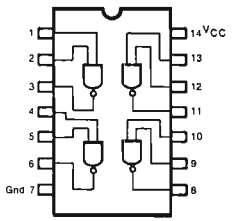


H 156/H 157

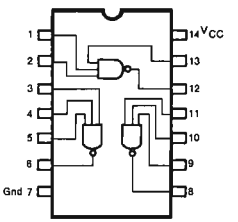


EXTENDED TEMPERATURE RANGE

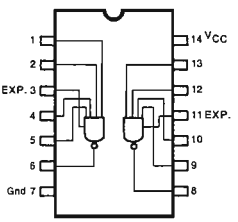
CONNECTION DIAGRAMS (top view)



H 102

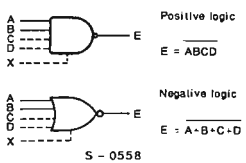


H 103



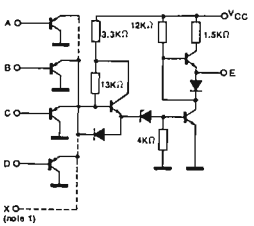
H 104

LOGIC FUNCTION



S - 0558

SCHEMATIC DIAGRAM
(one gate only)



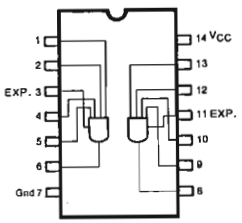
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	−55°C		25°C			125°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IL}	I_{OH} = −200μA I_{OH} = −200μA (see below)
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 1.5V
I_{FEX}	Expander Input Low Current (Note 2)		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 2V
I_R	Reverse Input Current		7		0.1	7		7	μA	V_{CC} = 16V	V_R = 16V
I_{SC}	Output Short Circuit Current	-6.5	-20	-6.5	-13.5	-20	-6.5	-20	mA	V_{CC} = 16V	Inputs and Output Grounded
I_{PDH}	High Level Power Dissipstion Current (Each Gate)		6		4.4	6		6	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gats)		2		1.2	2		2	mA	V_{CC} = 16V	Inputs Low
TPD+	Turn-Off Delay				160	250			nsec	V_{CC} = 15V	See Test Circuit
TPD−	Turn-On Delay				50	100			nsec	V_{CC} = 15V	See Test Circuit

NOTES: 1) The node can be expanded using EB383 or BAY72 diodes
2) For H 104 only

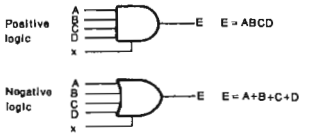
EXTENDED TEMPERATURE RANGE

CONNECTION DIAGRAM (top view)

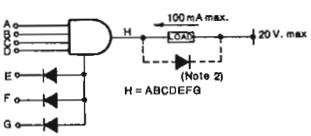


H 109

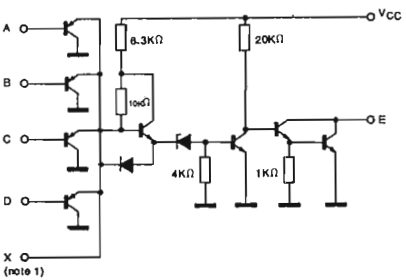
LOGIC FUNCTION



USE OF H109 POWER GATE



SCHEMATIC DIAGRAM (one gate only)

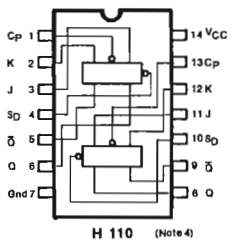


ELECTRICAL CHARACTERISTICS

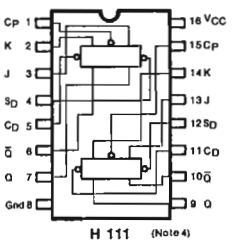
SYMBOL	CHARACTERISTIC	−55°C		25°C			125°C		UNIT	CONDITIONS
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 16V.or / V_{CC} = 10.8V ; I_{OL} = 100mA / V_{IN} = V_{IL} (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V / V_{CC} = 10.8V ; V_F = 1.5V
I_{FEX}	Expander Input Low Current		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V / V_{CC} = 10.8V ; V_{FEX} = 2V
I_R	Reverse Input Current		7		0.1	7		7	μA	V_{CC} = 16V V_R = 16V
I_{CEX}	Output Leakage Current		100			100		100	μA	V_{CC} = 16V V_{CEX} = 16V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.75		3.5	4.75		4.75	mA	V_{CC} = 16V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		3.75		2.6	3.75		3.75	mA	V_{CC} = 16V Inputs Low
TPD+	Turn-Off Delay				80	250			nsec	V_{CC} = 15V See Test Circuit
TPD−	Turn-On Delay				50	100			nsec	V_{CC} = 15V See Test Circuit

NOTES: 1) The node can be expanded using EB 383 or BAY 72 diodes
2) Use a diode when operating with an inductive load

CONNECTION DIAGRAMS (top view)

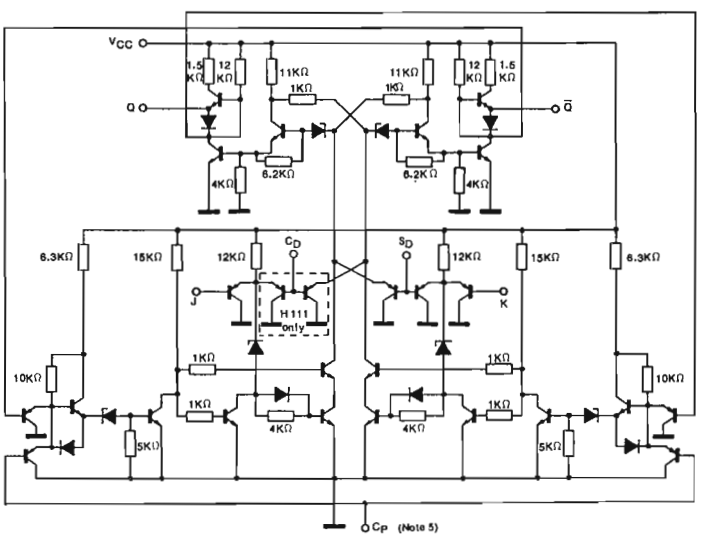


H 110 (Note 4)



H 111 (Note 4)

SCHEMATIC DIAGRAM (one flip-flop only)



TRUTH TABLES

Synchronous entry (note 1)			
time t_n		time t_n+1	
J	K	Q	$\bar{Q}$
H	H	$\bar{Q}_n$	Q_n
H	L	H	L
L	H	L	H
L	L	NC	NC

Asynchronous entry (note 2)			
inputs		outputs	
S_D	C_D (note 3)	Q	$\bar{Q}$
H	H	NC	NC
H	L	L	H
L	H	H	L
L	L	H	H

SYMBOLS:
NC = no change
Q_n = output state at time t_n

OUTPUTS:
$L = V_{OL}$
$H = V_{OH}$

INPUTS:
$L = V_{IL}$
$H = V_{IH}$

EXTENDED TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS

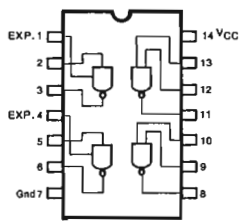
SYMBOL	CHARACTERISTIC	−55°C		25°C			125°C		UNIT	CONDITIONS
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} see truth table — I_{OH} = -200μA
V_{OL}	Output Low Voltage		1.5			1.5		1.5	V	V_{CC} = 16V I_{OL} = 12.5mA V_{CC} = 10.8V I_{OL} = 9mA V_{IN} see truth table
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current (J-K-SD-CD Inputs)		-0.65 -0.48		-0.1 -0.08	-0.65 -0.48		-0.65 -0.48	mA mA	V_{CC} = 16V V_{CC} = 10.8V — V_F = 1.5V
I_{FCP}	Input Low Current (Clock Input)		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V — V_{FCP} = 1.5V
I_R	Reverse Input Current (J-K Inputs)		7		0.1	7		7	μA	V_{CC} = 16V V_R = 16V
I_R	Reverse Input Current (CP-SD-CD Inputs)		14		0.2	14		14	μA	V_{CC} = 16V V_R = 16V
I_{SC}	Output Short Circuit Current	-6.5	-20	-6.5	-13.5	-20	-6.5	-20	mA	V_{CC} = 16V Output and Asynchronous Grounded
I_{PD}	Power Dissipation Current		24			24		24	mA	V_{CC} = 16V SD Grounded
TPD+	Turn-Off Delay				250	600			nsec	V_{CC} = 15V See Test Circuit
TPD−	Turn-On Delay				200	400			nsec	
f_{clock}	Toggle Frequency (Max Clock Frequency)			500	1000				kHz	

NOTES:
1) JK mode operation
2) Indipendent of clock and asynchronous inputs
3) Truth table for H 110. C_D not connected
4) Unused flip-flop input pins must be connected to V_{CC}
5) The fall time of the clock pulse must be lower than 1 μSEC/Volt.

EXTENDED TEMPERATURE RANGE

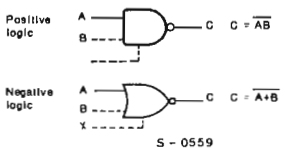
The H113 could be used as a quad high to low level converter or as a quad HLL gate with open collector output ORing function.

CONNECTION DIAGRAM (top view)



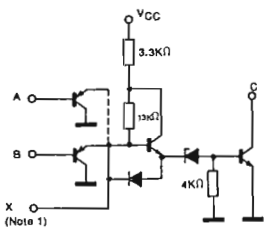
H 113

LOGIC FUNCTION



S - 0559

SCHEMATIC DIAGRAM (one gate only)



ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	-55°C		25°C			125°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OL}	Output Low Voltage		0.45		0.3	0.45		0.45	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 1.5V
I_{FEX}	Expander Input Low Current		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 2V
I_R	Reverse Input Current		7		0.1	7		7	μA	V_{CC} = 16V	V_R = 16V
I_{CEX}	Output Leakage Current		80 24			80 24		80 24	μA μA	V_{CC} = 16V V_{CC} = 16V	V_{CEX} = 16V V_{CEX} = 5.25V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		5		3.5	5		5	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2		1.2	2		2	mA	V_{CC} = 16V	Inputs Low
TPD+	Turn-Off Delay				110	250			nsec	V_{CC} = 15V See Test Circuit	
TPD-	Turn-On Delay				40	100			nsec		

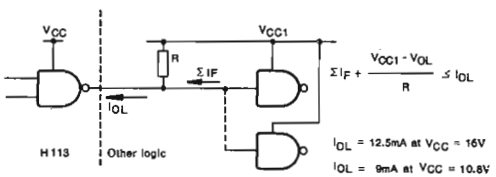
EXTENDED TEMPERATURE RANGE

USE OF H113 HIGH TO LOW LEVEL CONVERTER

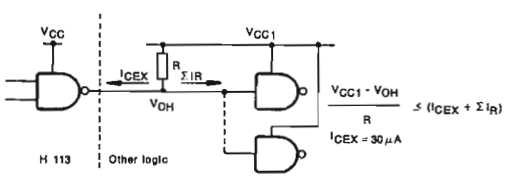
The output of H 113 is an open collector, therefore it needs a pull-up resistor.

The output swing is a function of the voltage at which the pull-up resistor is connected, so the H 113 could also be considered as an open collector HLL gate which allows the output OR-ing function.

1) OUTPUT LOW



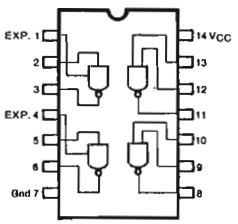
2) OUTPUT HIGH



NOTE: 1) The node can be expanded using EB 383 or BAY 72 diodes

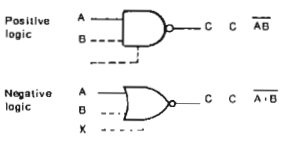
EXTENDED TEMPERATURE RANGE

CONNECTION DIAGRAM (top view)



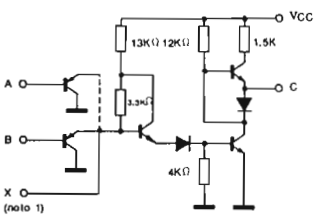
H 114

LOGIC FUNCTION



S - 0559

SCHEMATIC DIAGRAM (one gate only)



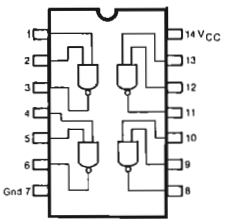
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	−55°C		25°C			125°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IL}	I_{OH} = -200μA (see below)
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	2.1		1.8			1.55		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 0.45V
I_{FEX}	Expander Input Low Current		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 0.9V
I_R	Reverse Input Current		7		0.1	7		7	μA	V_{CC} = 16V	V_R = 4.5V
I_{SC}	Output Short Circuit Current	-6.5	-20	-6.5	-13.5	-20	-6.5	-20	mA	V_{CC} = 16V	Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4		3	4		4	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation		2		1.2	2		2	mA	V_{CC} = 16V	Inputs Low
TPD+	Turn-Off Delay				160	250			nsec	V_{CC} = 15V See Test Circuit	
TPD−	Turn-On Delay				50	100			nsec		

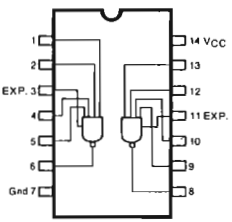
NOTE: 1) The node can be expanded using the DTL 9933 or BAY 74 diodes

EXTENDED TEMPERATURE RANGE

CONNECTION DIAGRAMS (top view)

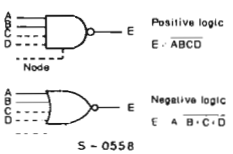


H 122



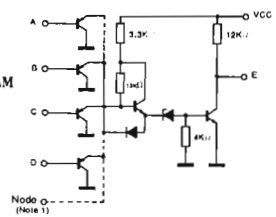
H 124

LOGIC FUNCTION



S - 0558

SCHEMATIC DIAGRAM
(one gate only)



ELECTRICAL CHARACTERISTICS

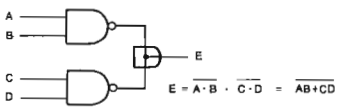
SYMBOL	CHARACTERISTIC	−55°C		25°C			125°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IL}	I_{OH} = -50μA (see below)
V_{OL}	Output Low Voltage		1.5		0.2	1.5		1.5	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 1.5V
I_{FEX}	Expander Input Low Current (H124 only)		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 2V
I_R	Reverse Input Current		7		0.1	7		7	μA	V_{CC} = 16V	V_R = 16V
I_{CEX}	Output Leakage Current		45			45		45	μA	V_{CC} = 16V	V_{CEX} = 16V
I_{SC}	Output Short Circuit Current	-0.9	-2.05	-0.9	-1.6	-2.05	-0.9	-2.05	mA	V_{CC} = 16V	Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6		4.8	6		6	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2		1,2	2		2	mA	V_{CC} = 16V	Inputs Low
TPD+	Turn-Off Delay				250	400			nsec	V_{CC} = 15V	See Test Circuit
TPD−	Turn-On Delay				40	100			nsec	V_{CC} = 15V	

NOTES: 1) The node can be expanded using diode EB 383 or BAY 72
2) For H 124 only

EXTENDED TEMPERATURE RANGE

WIRED - OR CONNECTION

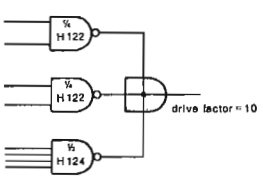
Outputs of H 122 and H 124 may be tied together for the wired - OR function.



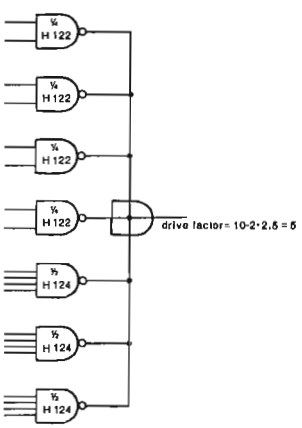
If 2, 3, 4, or 5 H 122 (or H 124) are OR-ed, the drive factor is 10.

For each additional gate over 5 a unit load of 2.5 should be subtracted from the drive factor of the gate.

EXAMPLE 1



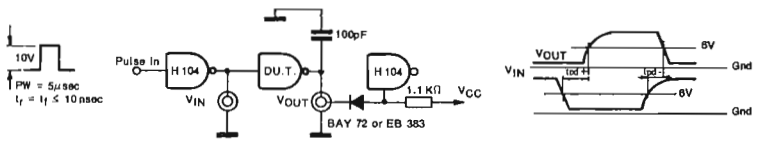
EXAMPLE 2

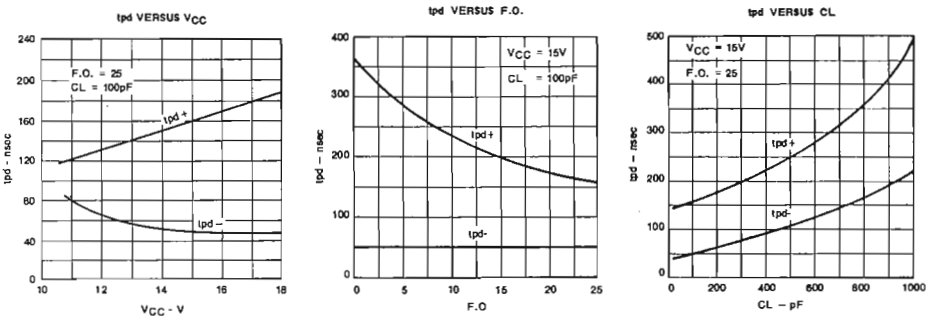


EXTENDED TEMPERATURE RANGE

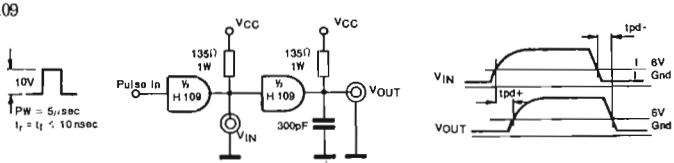
SWITCHING TIME TEST CIRCUITS

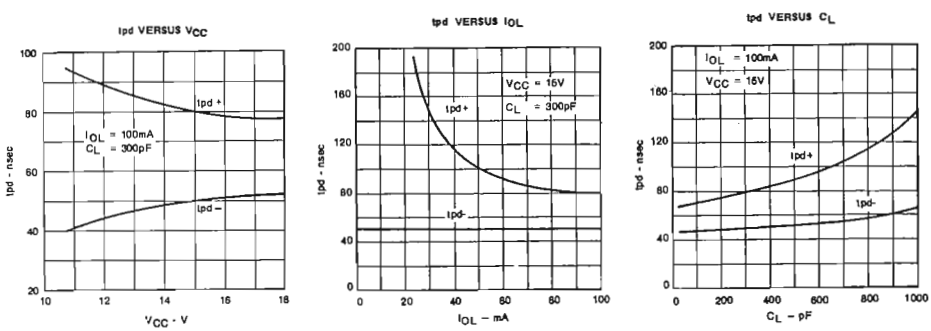
Gates H102-H103-H104



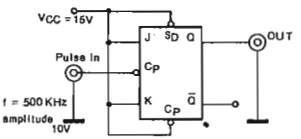


Power Gate H 109

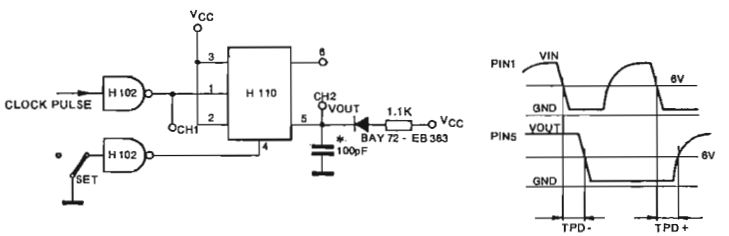




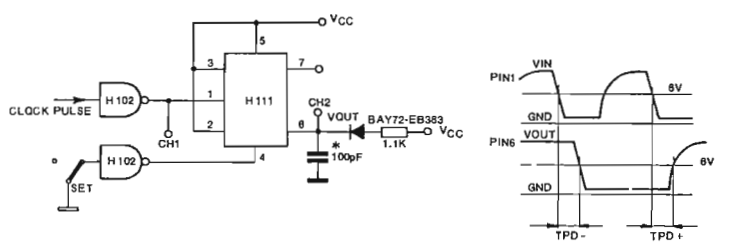
Dual J-K Flip-Flops H 110-H 111

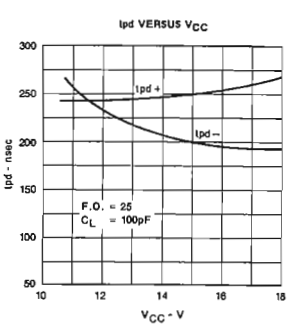


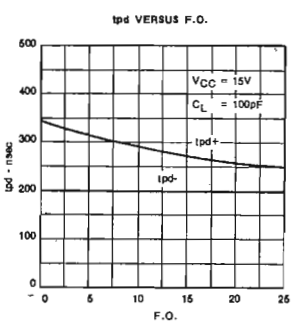
Dual J-K Flip-Flop H 110

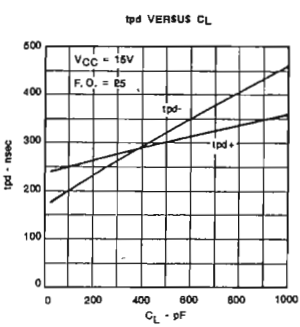


Dual J-K Flip-Flop H 111





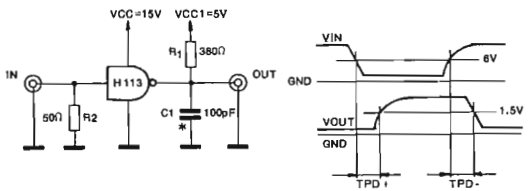


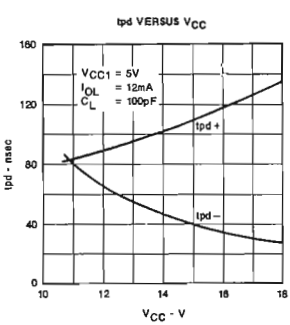


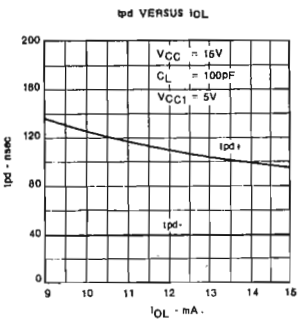
* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

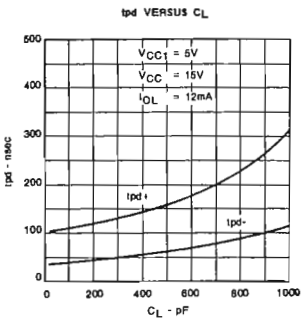
EXTENDED TEMPERATURE RANGE

High to Low Level Quad Converter H 113

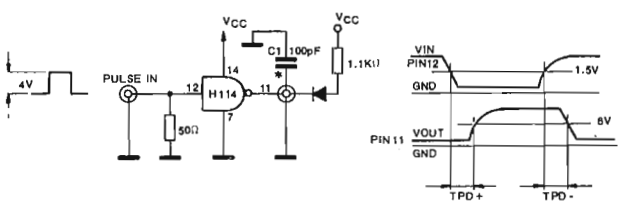


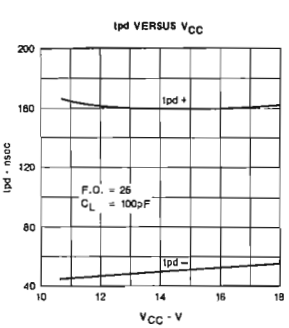


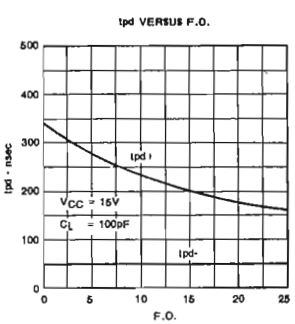


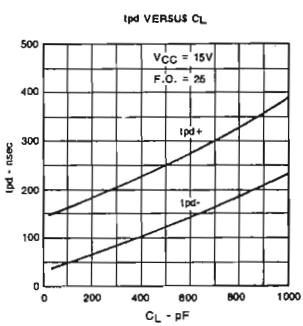


Low to High Level Quad Converter H 114



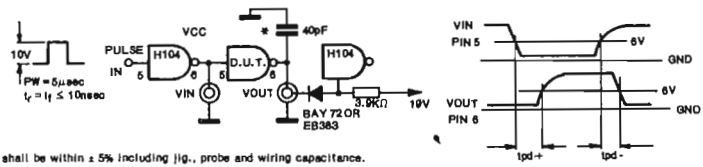




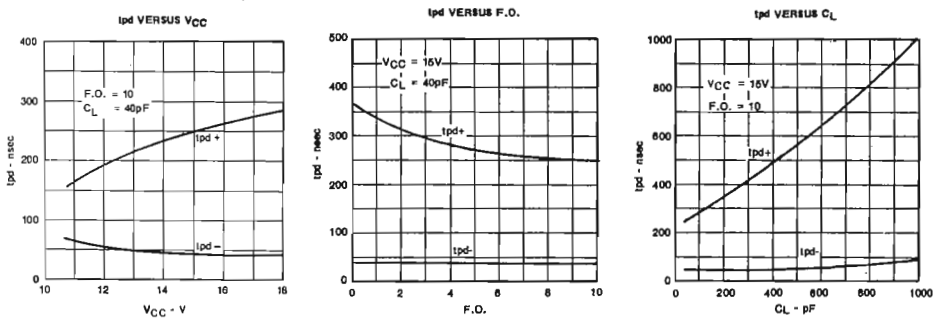


* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

Gates With Passive Pull-Up H 122 - H 124

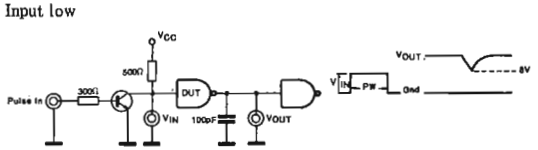


* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

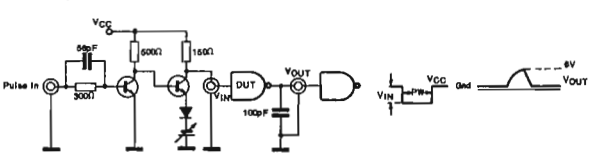


AC NOISE IMMUNITY TEST CIRCUIT (FOR GATES ONLY)

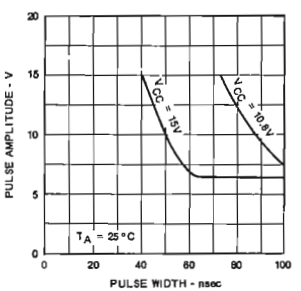
Input low



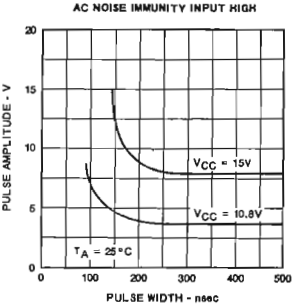
Input high



AC NOISE IMMUNITY INPUT LOW

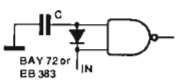


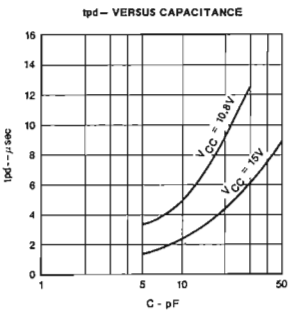
AC NOISE IMMUNITY INPUT HIGH



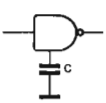
EXTENDED TEMPERATURE RANGE

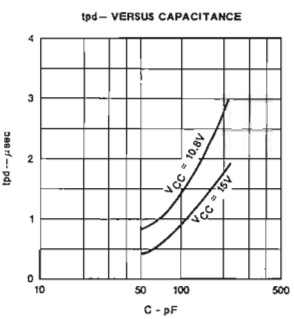
SLOW DOWN OF TPD - (FOR GATES)





SLOW DOWN OF TPD - (FOR EXPANDER)





High level logic family

INTERMEDIATE TEMPERATURE RANGE
-40° C TO 85° C

- WIDE RANGE OF SUPPLY VOLTAGE 10.8V TO 16V
- HIGH DC NOISE IMMUNITY 5V (TYP.) AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS I C's

High Level Logic is a family of high threshold integrated circuits.
It offers the advantages of 5V DC noise immunity, high signal levels, large supply voltage tolerances and unusually high fan-out.
These features make the family particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.
The H 100 series elements are available in the hermetically sealed ceramic dual in-line package.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) continuous		18V
Input Voltage	-0.5V to	16V
Storage Temperature Range	-65° C to	150° C

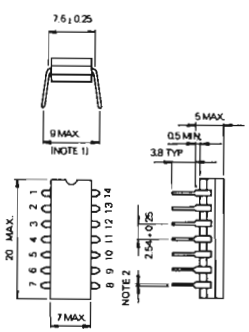
OPERATING CONDITIONS

Operating Temperature	-40° C to	85° C
Supply Voltage	10.8V to	16V

ORDERING NUMBER

H1XX D6

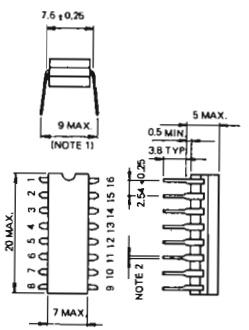
PHYSICAL DIMENSIONS
14 pin ceramic DIP



NOTES

1) Leads are intended for insertion in hole rows on 7.6 mm. centres. They are purposely shipped with "positive" (9 mm.) misalignment to facilitate insertion.
2) Board-drilling dimensions should equal your practice for a conventional 0.51 mm. diameter lead.
3) All dimensions in mm.

PHYSICAL DIMENSIONS
16 pin ceramic DIP



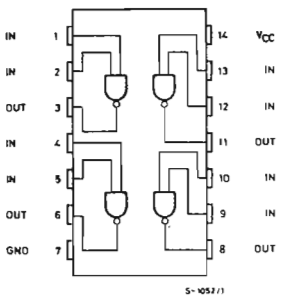
NOTES

1) Leads are intended for insertion in hole rows on 7.6 mm. centres. They are purposely shipped with "positive" (9 mm.) misalignment to facilitate insertion.
2) Board-drilling dimensions should equal your practice for a conventional 0.51 mm. diameter lead.
3) All dimensions in mm.

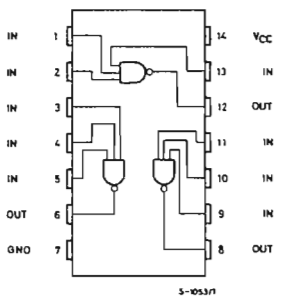
INTERMEDIATE TEMPERATURE RANGE

CONNECTION DIAGRAMS

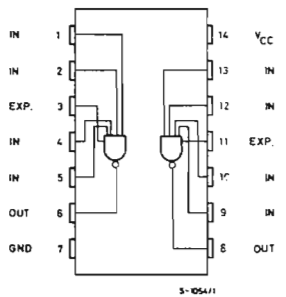
H 102/H 122



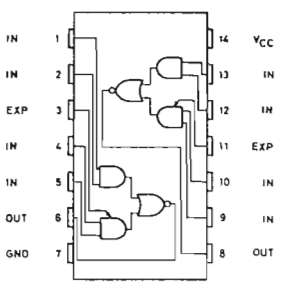
H 103



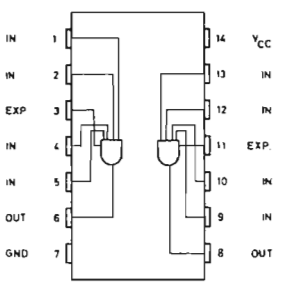
H 104/H 124



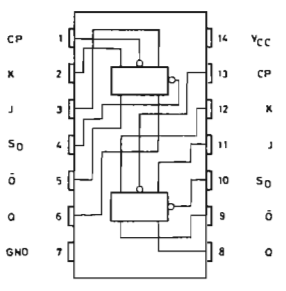
H 105



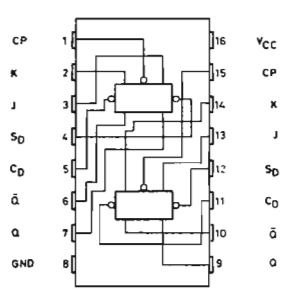
H 109



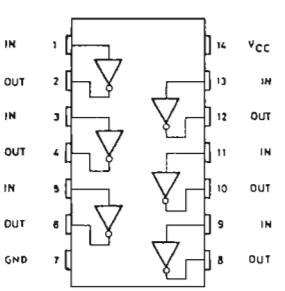
H 110



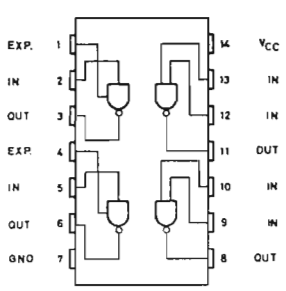
H 111



H 112/H 118

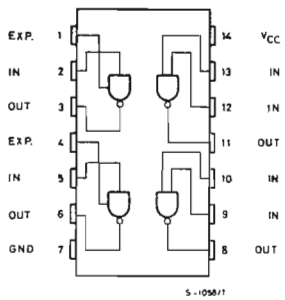


H 113

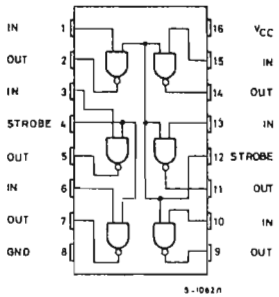


CONNECTION DIAGRAMS (continued)

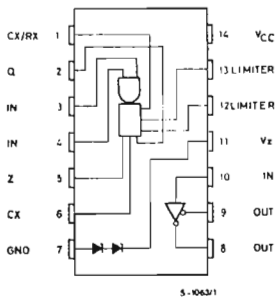
H 114



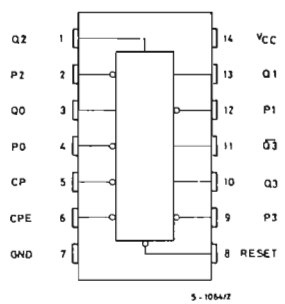
H 115/H119



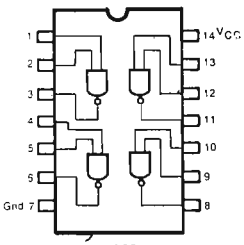
H 117



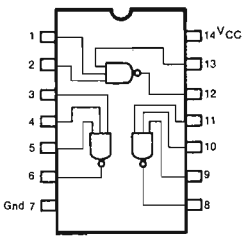
H 156



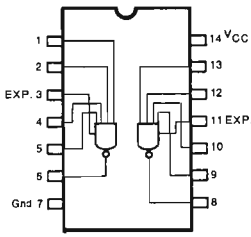
CONNECTION DIAGRAMS (Top view)



H 102

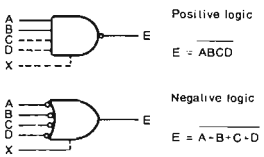


H 103

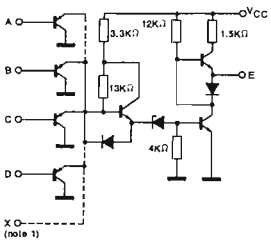


H 104

LOGIC FUNCTION



SCHEMATIC DIAGRAM
(one gate only)

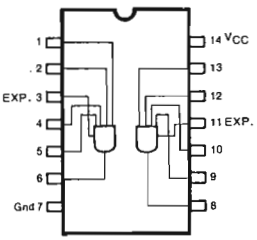


ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	−40°C		25°C			85°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IL}	I_{OH} = −200μA I_{OH} = −200μA (see below)
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 1.5V
I_{FEX}	Expander Input Low Current (Note 2)		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 2V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 16V	V_R = 16V
I_{SC}	Output Short Circuit Current	-6.5	-20	-6.5	-13.5	-20	-6.5	-20	mA	V_{CC} = 16V	Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6		4.4	6		6	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2		1.2	2		2	mA	V_{CC} = 16 V	Inputs Low
TPD_+	Turn-Off Delay				160	250			nsec	V_{CC} = 15V	See Test Circuit
TPD_-	Turn-On Delay				50	100			nsec	V_{CC} = 15V	See Test Circuit

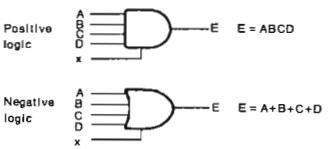
NOTES: 1) The node can be expanded using EB 383 or BAY 72 diodes
2) For H 104 only

CONNECTION DIAGRAM (top view)

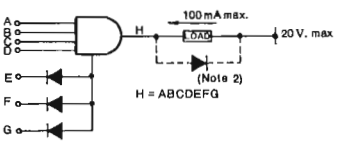


H 109

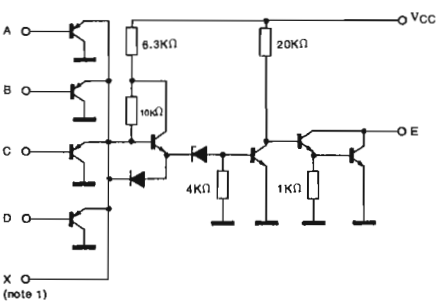
LOGIC FUNCTION



USE OF H109 POWER GATE



SCHEMATIC DIAGRAM (one gate only)

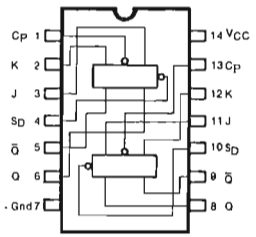


ELECTRICAL CHARACTERISTICS

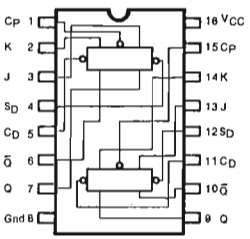
SYMBOL	CHARACTERISTIC	−40°C		25°C			85°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 16V.or V_{CC} = 10.8V	I_{OL} = 100mA V_{IN} = V_{IL} (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 1.5V
I_{FEX}	Expander Input Low Current		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 2V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 16V	V_R = 16V
I_{CEX}	Output Leakage Current		100			100		100	μA	V_{CC} = 16V	V_{CEX} = 16V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.75		3.5	4.75		4.75	mA	V_{CC} = 16V Inputs High	
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		3.75		2.6	3.75		3.75	mA	V_{CC} = 16V Inputs Low	
TPD+	Turn-Off Delay				80	250			nsec	V_{CC} = 15V	See Test Circuit
TPD−	Turn-On Delay				50	100			nsec	V_{CC} = 15V	See Test Circuit

NOTES: 1) The node can be expanded using EB 383 or BAY 72 diodes
2) Use a diode when operating with an inductive load

CONNECTION DIAGRAMS (top view)

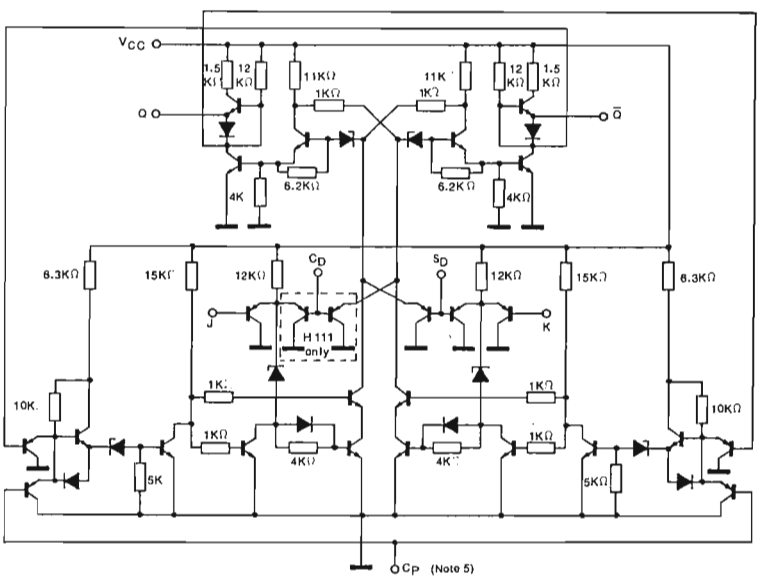


H 110 (Note 4)



H 111 (Note 4)

SCHEMATIC DIAGRAM (one flip-flop only)



TRUTH TABLES

Synchronous entry (note 1)			
time t_n		time t_n+1	
J	K	Q	$\bar{Q}$
H	H	$\bar{Q}n$	Qn
H	L	H	L
L	H	L	H
L	L	NC	NC

Asynchronous entry (note 2)			
inputs		outputs	
SD	CD (note 3)	Q	$\bar{Q}$
H	H	NC	NC
H	L	L	H
L	H	H	L
L	L	H	H

SYMBOLS:
NC = no change
Qn = output state at time t_n

OUTPUTS:
L = V_{OL}
H = V_{OH}

INPUTS:
L = V_{IL}
H = V_{IH}

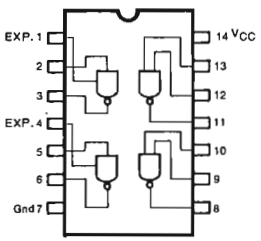
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	-40°C		25°C			85°C		UNIT	CONDITIONS
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V } I_{OH} = -200μA V_{IN} see truth table
V_{OL}	Output Low Voltage		1.5			1.5		1.5	V	V_{CC} = 16V I_{OL} = 12.5mA V_{CC} = 10.8V I_{OL} = 9mA V_{IN} see truth table
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current (J-K-SD-CD Inputs)		-0.65 -0.48		-0.1 -0.08	-0.65 -0.48		-0.65 -0.48	mA mA	V_{CC} = 16V V_{CC} = 10.8V } V_F = 1.5V
I_{FCP}	Input Low Current (Clock Input)		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V } V_{FCP} = 1.5V
I_R	Reverse Input Current (J-K Inputs)		5		0.1	5		5	μA	V_{CC} = 16V V_R = 16V
I_R	Reverse Input Current (CP-SD-CD Inputs)		10		0.2	10		10	μA	V_{CC} = 16V V_R = 16V
I_{SC}	Output Short Circuit Current	-6.5	-20	-6.5	-13.5	-20	-6.5	-20	mA	V_{CC} = 16V Output and Asynchronous Grounded
I_{PD}	Power Dissipation Current		28		22	28		28	mA	V_{CC} = 16V SD Grounded
TPD+	Turn-Off Delay				250	600			nsec	V_{CC} = 15V
TPD-	Turn-On Delay				200	400			nsec	See Test Circuit
f_{clock}	Toggle Frequency (Max Clock Frequency)			500	1000				kHz	

NOTES:
1) JK mode operation
2) Indipendent of clock and synchronous inputs
3) Truth table for H 110. C_D not connected
4) Unused flip flop input pins must be connected to V_{CC}
5) The fall time of the clock pulse must be lower than 1 μSEC/Volt.

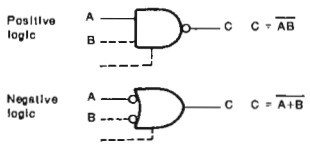
The H113 could be used as a quad high to low level converter or as a quad HLL gate with open collector output ORin function.

CONNECTION DIAGRAM (top view)

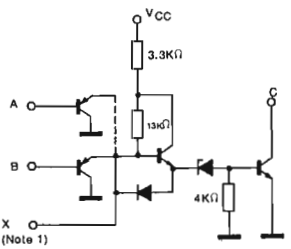


H 113

LOGIC FUNCTION



SCHEMATIC DIAGRAM (one gate only)



ELECTRICAL CHARACTERISTICS

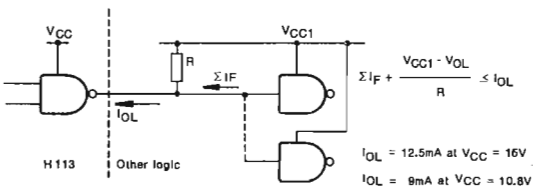
SYMBOL	CHARACTERISTIC	−40°C		25°C			85°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OL}	Output Low Voltage		0.45		0.3	0.45		0.45	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 1.5V
I_{FEX}	Expander Input Low Current		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 2V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 16V	V_R = 16V
I_{CEX}	Output Leakage Current		80 24			80 24		80 24	μA μA	V_{CC} = 16V V_{CC} = 16V	V_{CEX} = 16V V_{CEX} = 5.25V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		5		3.5	5		5	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2		1.2	2		2	mA	V_{CC} = 16V	Inputs Low
TPD+	Turn-Off Delay				110	250			nsec	V_{CC} = 15V See Test Circuit	
TPD−	Turn-On Delay				40	100			nsec		

USE OF H113 HIGH TO LOW LEVEL CONVERTER

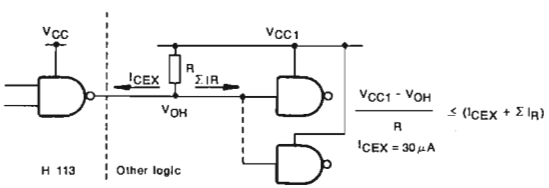
The output of H113 is an open collector, therefore it needs a pull-up resistor.

The output swing is a function of the voltage at which the pull-up resistor is connected, so the H113 could also be considered as an open collector HLL gate which allows the output OR-ing function.

1) OUTPUT LOW

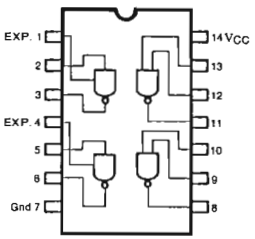


2) OUTPUT HIGH



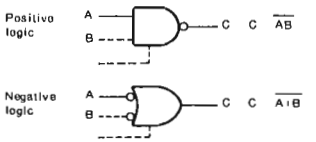
NOTE: 1) The node can be expanded using EB 383 or BAY 72 diodes

CONNECTION DIAGRAM (top view)

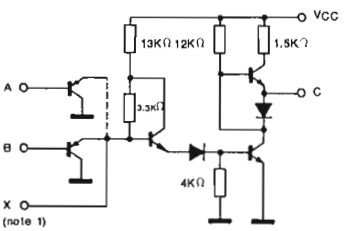


H 114

LOGIC FUNCTION



SCHEMATIC DIAGRAM (one gate only)

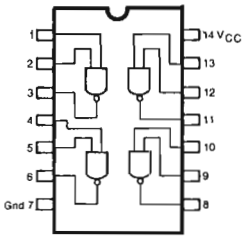


ELECTRICAL CHARACTERISTICS

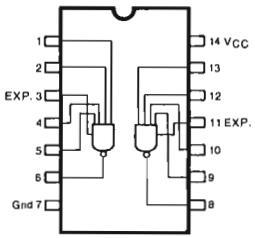
SYMBOL	CHARACTERISTIC	–40°C		25°C			85°C		UNIT	CONDITIONS
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IL} } I_{OH} = -200μA (see below)
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH} I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	2.1		1.8			1.55		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V } V_F = 0.45V
I_{FEX}	Expander Input Low Current		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V } V_{FEX} = 0.9V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 16V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-6.5	-20	-6.5	-13.5	-20	-6.5	-20	mA	V_{CC} = 16V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4		3	4		4	mA	V_{CC} = 16V Inputs High
I_{PDL}	Low Level Power Dissipation		2		1.2	2		2	mA	V_{CC} = 16V Inputs Low
TPD+	Turn-Off Delay				160	250			nsec	V_{CC} = 15V
TPD–	Turn-On Delay				50	100			nsec	See Test Circuit

NOTE: 1) The node can be expanded using the DTL 9933 or BAY 74 diodes

CONNECTION DIAGRAMS (top view)

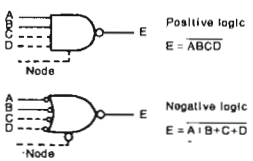


H 122

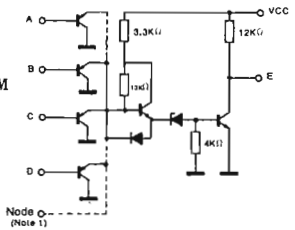


H 124

LOGIC FUNCTION



SCHEMATIC DIAGRAM
(one gate only)



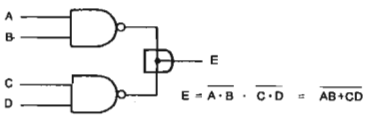
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	−40°C		25°C			85°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IL}	I_{OH} = -50μA (see below)
V_{OL}	Output Low Voltage		1.5		0.2	1.5		1.5	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 1.5V
I_{FEX}	Expander Input Low Current (H124 only)		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 2V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 16V	V_R = 16V
I_{CEX}	Output Leakage Current		45			45		45	μA	V_{CC} = 16V	V_{CEX} = 16V
I_{SC}	Output Short Circuit Current	-0.9	-2.05	-0.9	-1.6	-2.05	-0.9	-2.05	mA	V_{CC} = 16V	Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6		4.8	6		6	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2		1.2	2		2	mA	V_{CC} = 16V	Inputs Low
TPD+	Turn-Off Delay				250	400			nsec	V_{CC} = 15V	See Test Circuit
TPD−	Turn-On Delay				40	100			nsec	V_{CC} = 15V	

NOTES: 1) The node can be expanded using diode EB 383 or BAY 72
2) For H 124 only

WIRED - OR CONNECTION

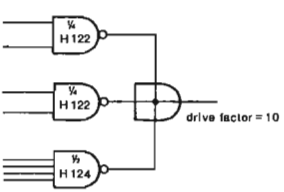
Outputs of H 122 and H 124 may be tied together for the wired - OR function.



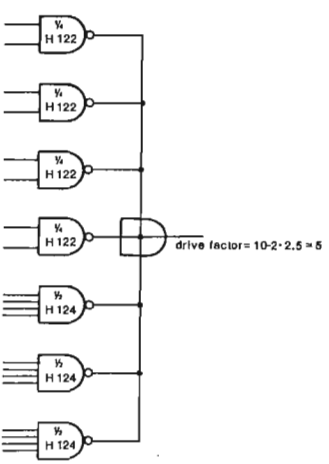
If 2, 3, 4, or 5 H122 (or H 124) are OR-ed, the drive factor is 10.

For each additional gate over 5 a unit load of 2.5 should be subtracted from the drive factor of the gate.

EXAMPLE 1

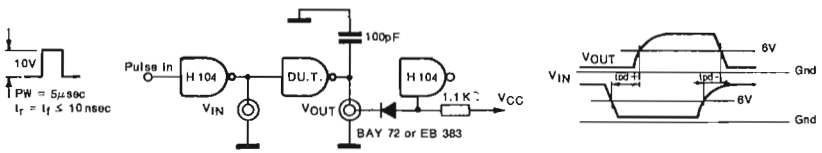


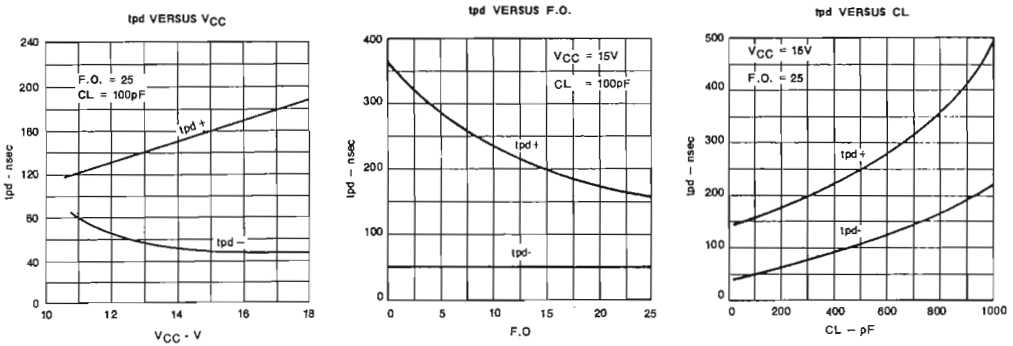
EXAMPLE 2



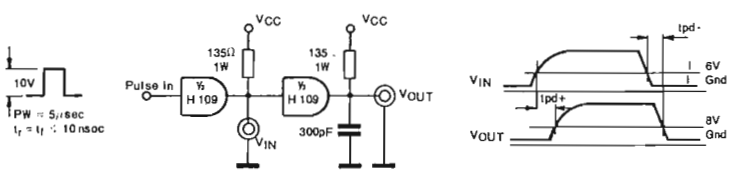
SWITCHING TIME TEST CIRCUITS

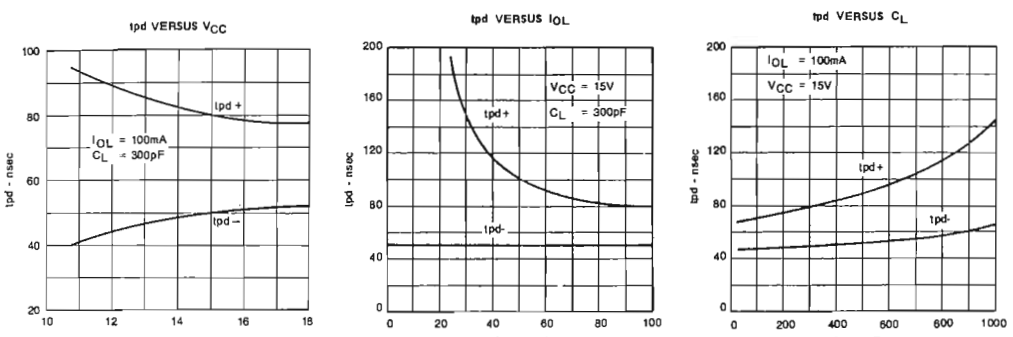
Gates H102-H103-H104



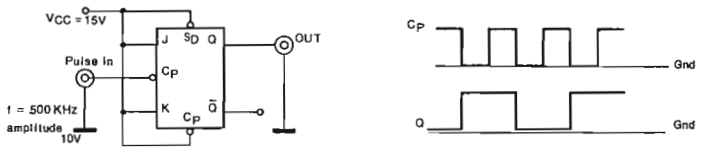


Power Gate H109

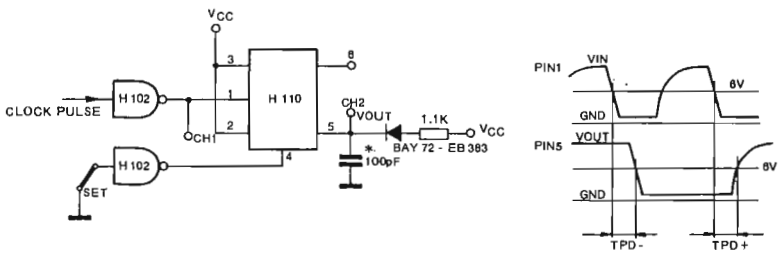




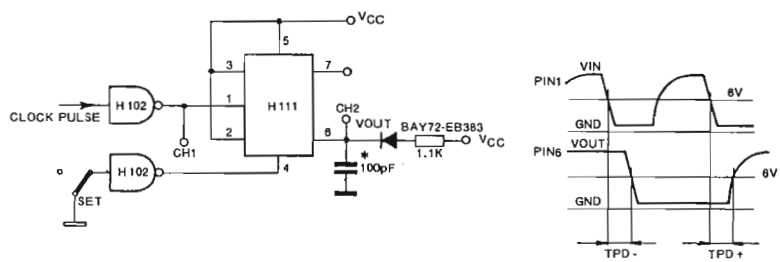
Dual J-K Flip-Flops H 110-H 111

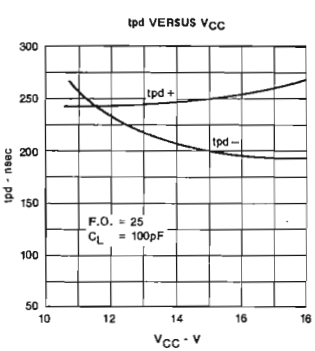


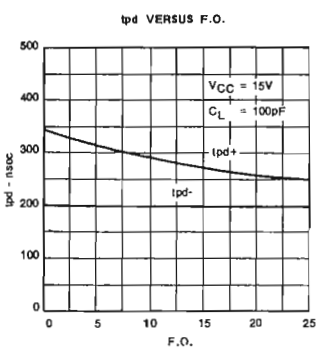
Dual J-K Flip-Flop H 110

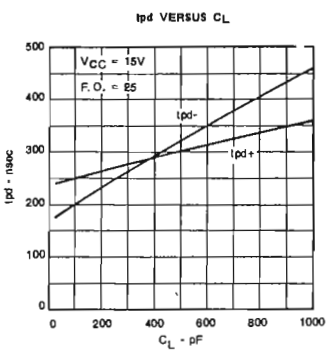


Dual J-K Flip-Flop H 111



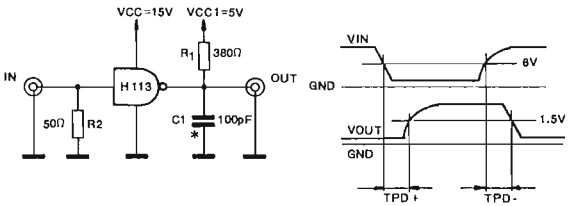


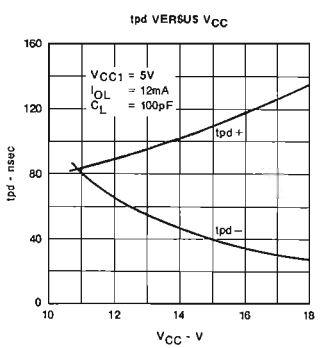


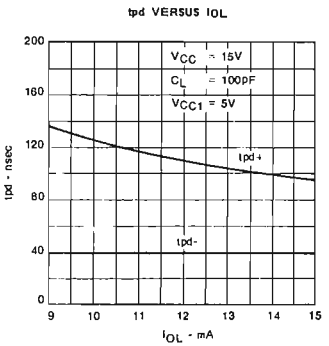


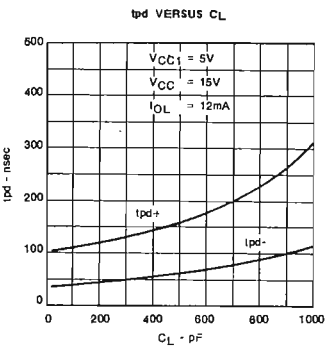
* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

High to Low Level Quad Converter H 113

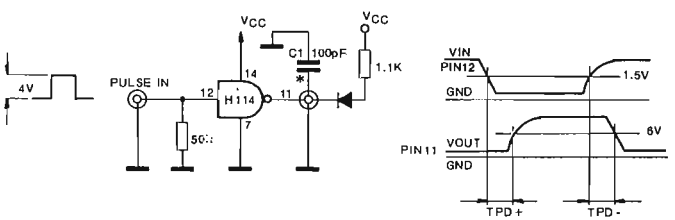


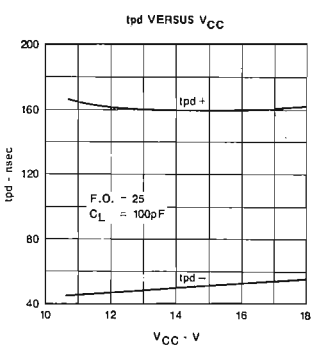


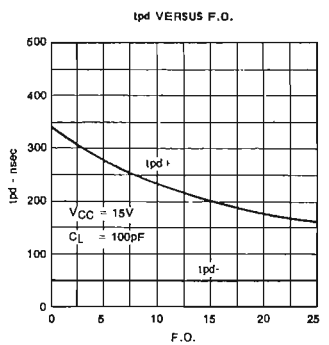


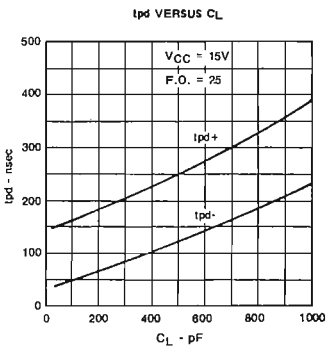


Low to High Level Quad Converter H 114



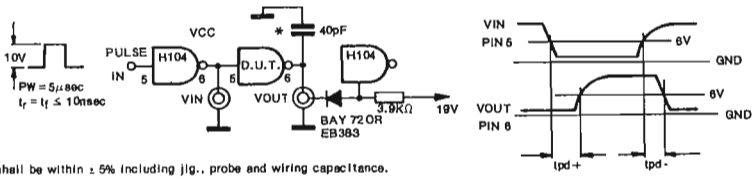




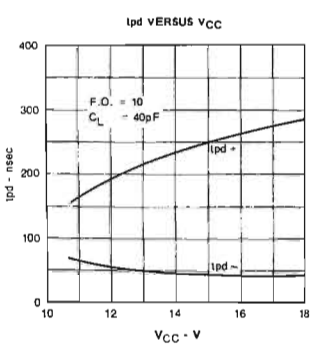


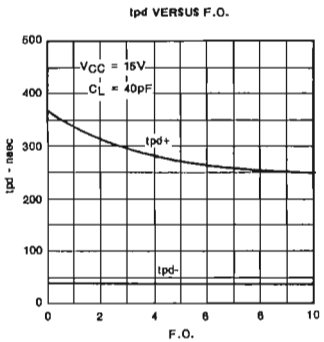
* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

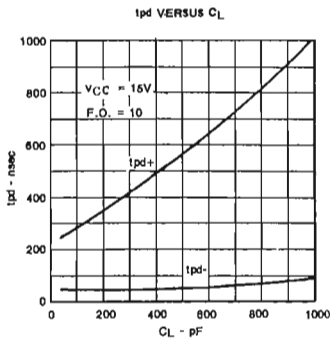
Gates With Passive Pull-Up H 122 - H 124



* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

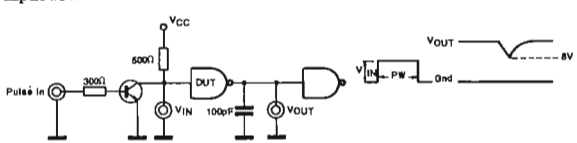


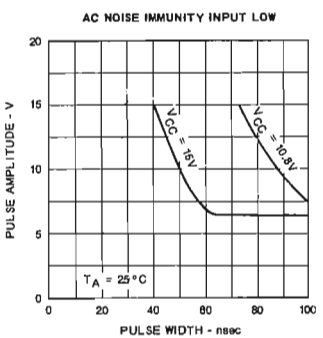




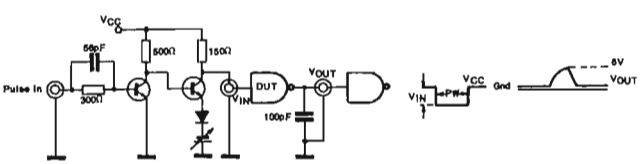
AC NOISE IMMUNITY TEST CIRCUIT (FOR GATES ONLY)

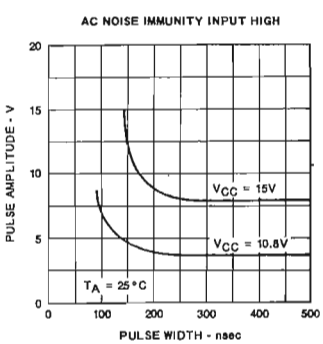
Input low



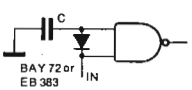


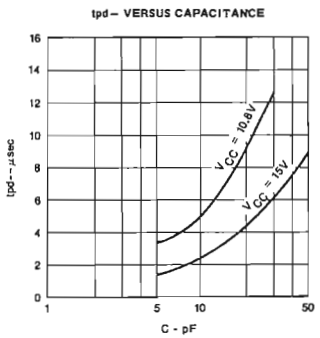
Input high



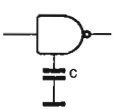


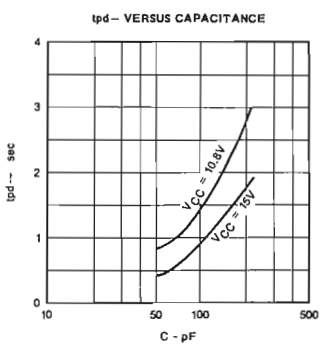
SLOW DOWN OF TPD - (FOR GATES)





SLOW DOWN OF TPD - (FOR EXPANDER)





H100 series

High level logic family

STANDARD TEMPERATURE RANGE, 0°C TO 75°C

- WIDE RANGE OF SUPPLY VOLTAGE 10.8 TO 20V
- HIGH DC NOISE IMMUNITY 5V (TYP.) AT V_{CC}=15V
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS I.C's

High Level Logic is a family of high threshold integrated circuits.
It offers the advantages of 5V DC noise immunity, high signal levels, large supply voltage tolerances and unusually high fan-out.
These features make the family particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.
The H 100 series elements are available in the hermetically sealed ceramic Dual-in-Line package.

ABSOLUTE MAXIMUM RATINGS

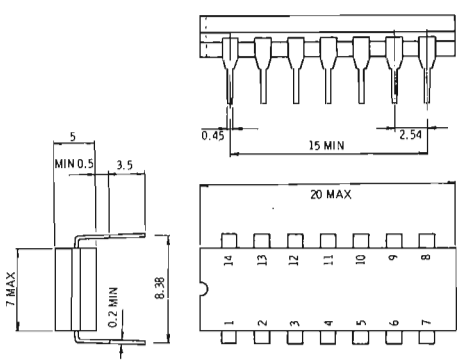
Supply Voltage (V_{CC}) continuous	22V
Input Voltage	-0.5V to 20V
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

Operating Temperature	0°C to 75°C
Supply Voltage	10.8V to 20V

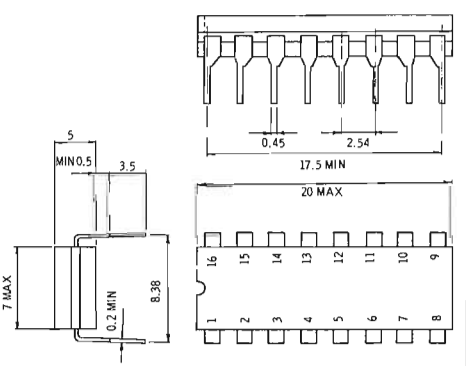
ORDERING NUMBER
H1XX D1

PHYSICAL DIMENSIONS
14-pin ceramic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
16-pin ceramic DIP

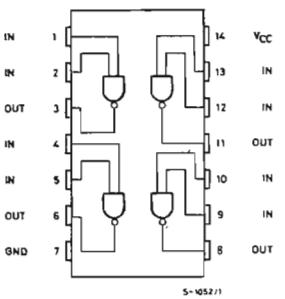


Note : all dimensions in mm.

STANDARD TEMPERATURE RANGE

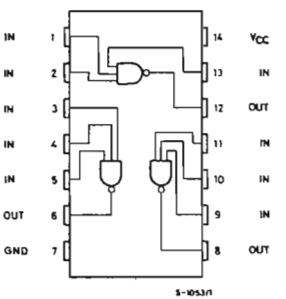
CONNECTION DIAGRAMS

H 102/H 122



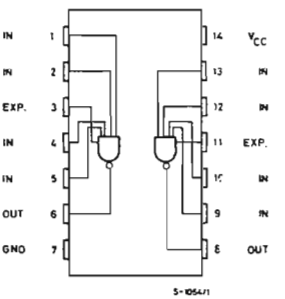
S-1052/1

H 103



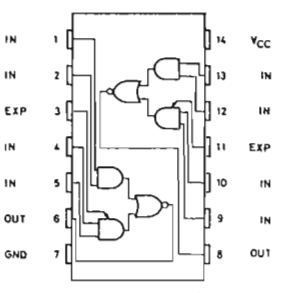
S-1053/1

H 104/H 124



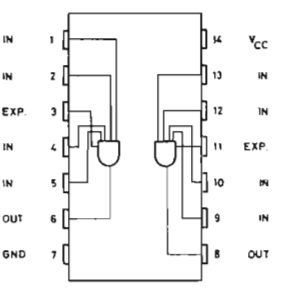
S-1054/1

H 105



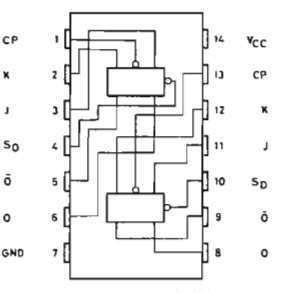
S-1060/1

H 109



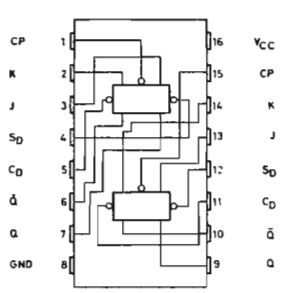
S-1055/1

H 110



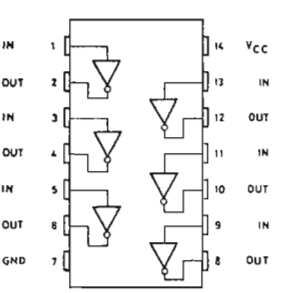
S-1056/1

H 111



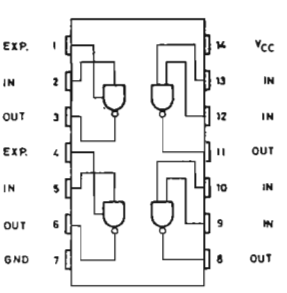
S-1057/1

H 112/H 118



S-1064/1

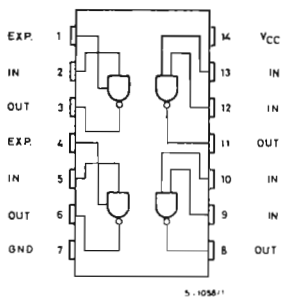
H 113



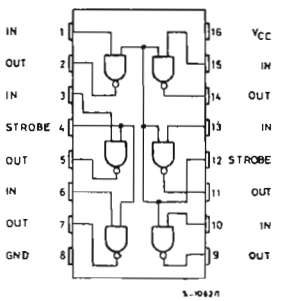
S-1058/1

CONNECTION DIAGRAMS (continued)

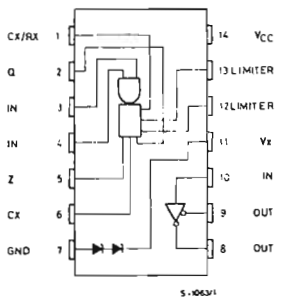
H 114



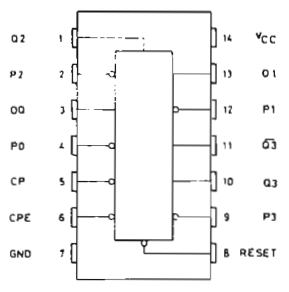
H 115/H119



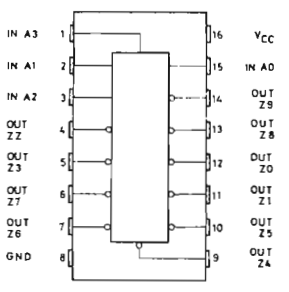
H 117



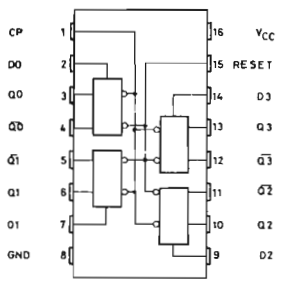
H 156/H 157



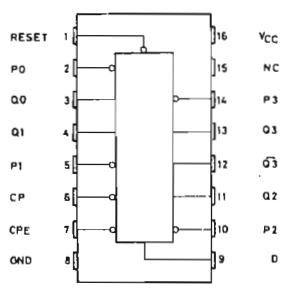
H 158



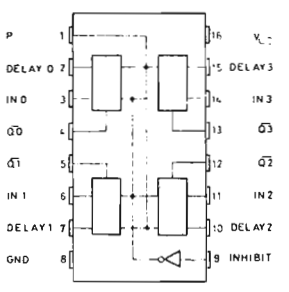
H 159



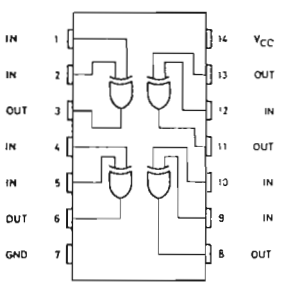
H 160



H 165/H 166

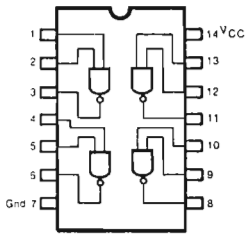


H 167/H 168

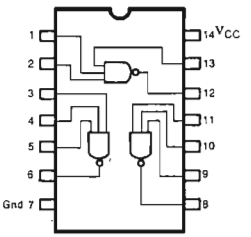


STANDARD TEMPERATURE RANGE

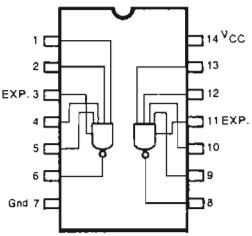
CONNECTION DIAGRAMS (Top view)



H 102

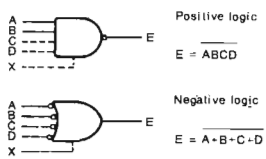


H 103

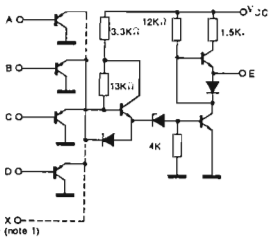


H 104

LOGIC FUNCTION



SCHEMATIC DIAGRAM
(one gate only)

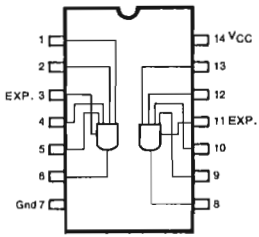


ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	18.5		18.5	19		18.5		V	V_{CC} = 20V I_{OH} - 200μA
		13.5		13.5	14		13.5		V	V_{CC} = 15V I_{OH} - 200μA
		9.3		9.3	9.8		9.3		V	V_{CC} = 10.8V I_{OH} - 200μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 20V I_{OL} = 15mA or V_{CC} = 15V I_{OL} = 12mA or V_{CC} = 10.8V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V V_F = 1.5V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_{FEX}	Expander Input Low Current (Note 2)		-1.65		-1.25	-1.65		-1.65	mA	V_{CC} = 20V
			-1.33		-0.90	-1.33		-1.33	mA	V_{CC} = 15V V_{FEX} = 2V
			-1		-0.75	-1		-1	mA	V_{CC} = 10.8V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 20V V_R = 20V
I_{SC}	Output Short Circuit Current	-9	-25	-9	-15	-25	-9	-25	mA	V_{GC} = 20V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		7.5		6	7.5		7.5	mA	V_{CC} = 20V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2.5		1.5	2.5		2.5	mA	V_{CC} = 20V Inputs Low
TPD_+	Turn-Off Delay				160	250			nS	V_{CC} = 15V See Test Circuit
TPD-	Turn-On Delay				50	100			nS	V_{CC} = 15V See Test Circuit

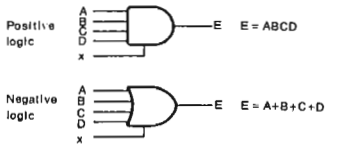
NOTES: 1) The node can be expanded using EB383 or BAY 72 diodes
2) For H 104 only

CONNECTION DIAGRAM (top view)

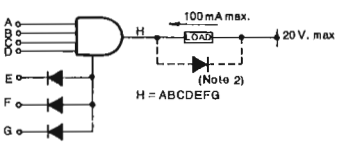


H 109

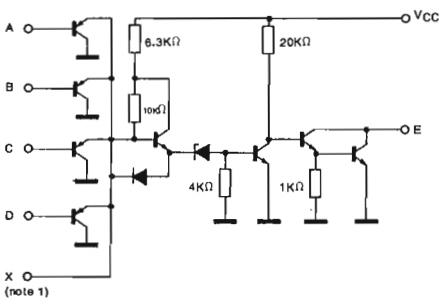
LOGIC FUNCTION



USE OF H 109 POWER GATE



SCHEMATIC DIAGRAM (one gate only)

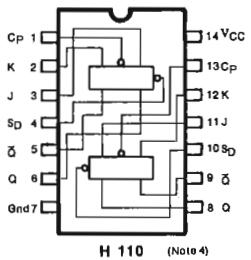


ELECTRICAL CHARACTERISTICS

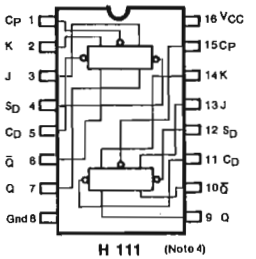
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	Unit	CONDITIONS
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 20V or 15V or 10.8V; I_{OL} = 100mA; V_{IN} = V_{IL} (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V; V_F = 1.5V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_{FEX}	Expander Input Low Current		-1.65		-1.25	-1.65		-1.65	mA	V_{CC} = 20V
			-1.33		-0.90	-1.33		-1.33	mA	V_{CC} = 15V; V_{FEX} = 2V
			-1		-0.75	-1		-1	mA	V_{CC} = 10.8V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 20V; V_R = 20V
I_{CEX}	Output Leakage Current		100			100		100	μA	V_{CC} = 20V; V_{CEX} = 20V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6		4.5	6		6	mA	V_{CC} = 20V; Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		4.5		3.5	4.5		4.5	mA	V_{CC} = 20V; Inputs Low
TPD+	Turn-Off Delay				80	250			nS	V_{CC} = 15V; See Test Circuit
TPD-	Turn-On Delay				50	100			nS	V_{CC} = 15V; See Test Circuit

NOTES: 1) The node can be expanded using EB 383 or BAY 72 diodes
2) Use a diode when operating with an inductive load

CONNECTION DIAGRAMS (top view)

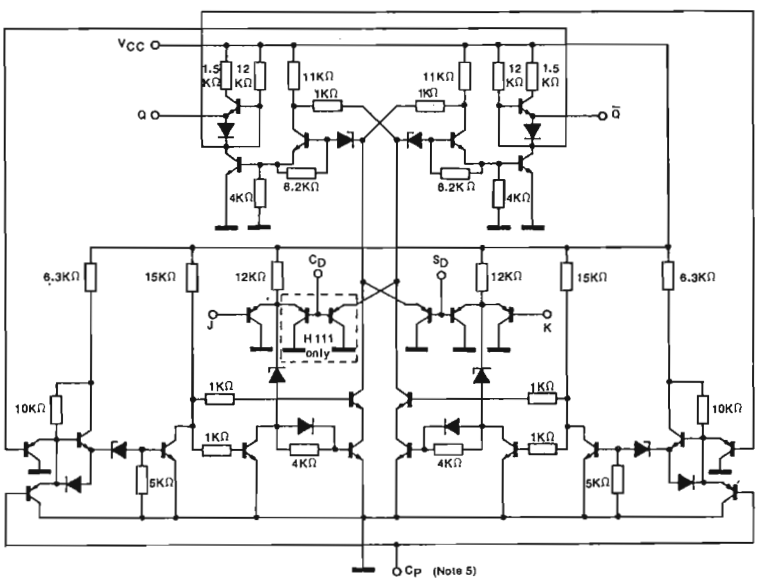


H 110 (Note 4)



H 111 (Note 4)

SCHEMATIC DIAGRAM (one flip-flop only)



TRUTH TABLES

Synchronous entry (note 1)			
time t_n		time t_n+1	
J	K	Q	$\bar{Q}$
H*	H	$\bar{Q}_n$	Q_n
H	L	H	L
L	H	L	H
L	L	NC	NC

Asynchronous entry (note 2)			
inputs		outputs	
S_D	C_D (note 3)	Q	$\bar{Q}$
H	H	NC	NC
H	L	L	H
L	H	H	L
L	L	H	H

SYMBOLS:
NC = no change
Q_n = output state at time t_n

OUTPUTS:
L = V_{OL}
H = V_{OH}

INPUTS:
L = V_{IL}
H = V_{IH}

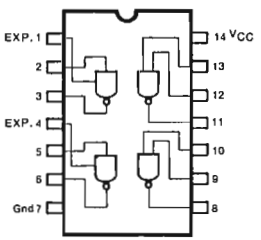
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	18.5		18.5	19		18.5		V	V_{CC} = 20V
		13.5		13.5	14		13.5		V	V_{CC} = 15V } I_{OH} = -200μA
		9.3		9.3	9.8		9.3		V	V_{CC} = 10.8V
										V_{IN} see truth table
V_{OL}	Output Low Voltage		1.5			1.5		1.5	V	V_{CC} = 20V I_{OL} = 15mA or V_{CC} = 15V I_{OL} = 12mA or V_{CC} = 10.8V I_{OL} = 9mA V_{IN} see truth table
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.8		-0.130	-0.8		-0.8	mA	V_{CC} = 20V
	(J-K-SD-CD Inputs)		-0.64		-0.100	-0.64		-0.64	mA	V_{CC} = 15V } V_F = 1.5V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 10.8V
I_{FCP}	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
	(Clock Input)		-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V } V_{FCP} = 1.5V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_R	Reverse Input Current (J-K Inputs)		5		0.1	5		5	μA	V_{CC} = 20V V_R = 20V
I_R	Reverse Input Current (CP, SD, CD Inputs)		10		0.2	10		10	μA	V_{CC} = 20V V_R = 20V
I_{SC}	Output Short Circuit Current	-9	-25	-9	-15	-25	-9	-25	mA	V_{CC} = 20V Output and Asynchronous Grounded
I_{PD}	Power Dissipation Current		35		24	35		35	mA	V_{CC} = 20V SD Grounded
TPD+	Turn-Off Delay				250	600			nS	V_{CC} = 15V
TPD-	Turn-On Delay				200	400			nS	See Test Circuit
f	Toggle Frequency			500	1000				KHz	

NOTES :
1) J-K mode operation
2) Independent of clock and synchronous inputs
3) Truth table for H 110. C_D not connected
4) Unused flip-flop input pins must be connected to V_{CC}
5) The fall time of the clock pulse must be lower than 1 µSEC/Volt.

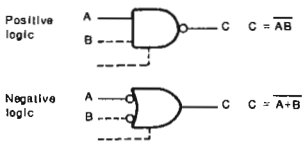
The H113 could be used as a quad high to low level converter or as a quad HLL gate with open collector output ORing function.

CONNECTION DIAGRAM (top view)

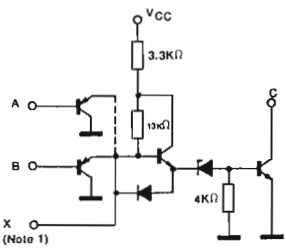


H 113

LOGIC FUNCTION



SCHEMATIC DIAGRAM (one gate only)



ELECTRICAL CHARACTERISTICS

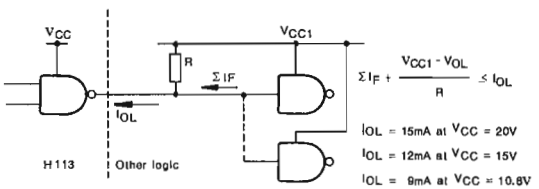
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	Unit	CONDITIONS
V_{OL}	Output Low Voltage		0.45		0.3	0.45		0.45	V	V_{CC} = 20V I_{OL} = 15mA or V_{CC} = 15V I_{OL} = 12mA or V_{CC} = 10.8V I_{OL} = 9mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V V_F = 1.5V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_{FEX}	Expander Input Low Current		-1.65		-1.21	-1.65		-1.65	mA	V_{CC} = 20V
			-1.33		-0.90	-1.33		-1.33	mA	V_{CC} = 15V V_{FEX} = 2V
			-1		-0.75	-1		-1	mA	V_{CC} = 10.8V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 20V V_R = 20V
I_{CEX}	Output Leakage Current		100			100		100	μA	V_{CC} = 20V V_{CEX} = 20V
			30			30		30	μA	V_{CC} = 20V V_{CEX} = 5.25V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6		4.5	6		6	mA	V_{CC} = 20V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2.5		1.5	2.5		2.5	mA	V_{CC} = 20V Inputs Low
TPD+	Turn-Off Delay				110	250			nS	V_{CC} = 15V
TPD-	Turn-On Delay				40	100			nS	See Test Circuit

USE OF H113 HIGH TO LOW LEVEL CONVERTER

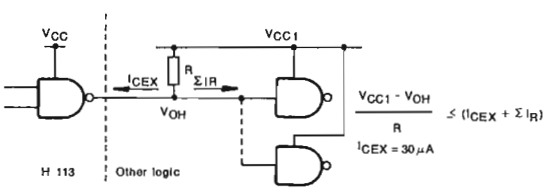
The output of H 113 is an open collector therefore it needs a pull-up resistor.

The output swing is a function of the voltage at which the pull-up resistor is connected, so the H 113 could also be considered as an open collector HLL gate which allows the output OR-ing function.

1) OUTPUT LOW

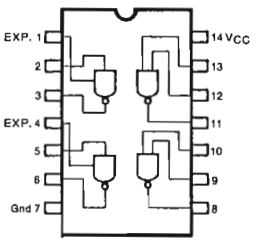


2) OUTPUT HIGH



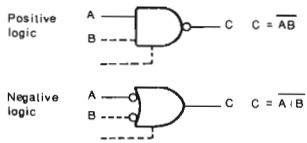
NOTE: 1) The node can be expanded using EB 383 or BAY 72 diodes

CONNECTION DIAGRAM (top view)

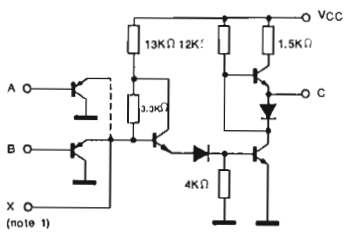


H 114

LOGIC FUNCTION



SCHEMATIC DIAGRAM (one gate only)

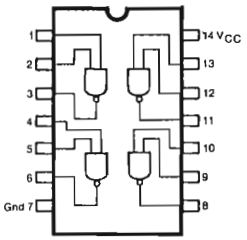


ELECTRICAL CHARACTERISTICS

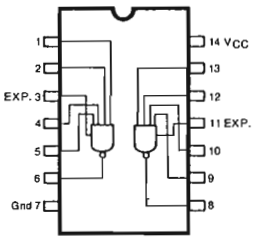
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	18.5		18.5	19		18.5		V	V_{CC} = 20V
		13.5		13.5	14		13.5		V	V_{CC} = 15V
		9.3		9.3	9.8		9.3		V	V_{CC} = 10.8V
										I_{OH} = -200μA
										V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 20V I_{OL} = 15mA or
										V_{CC} = 15V I_{OL} = 12mA or
										V_{CC} = 10.8V I_{OL} = 9mA
										V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
										V_F = 0.45V
I_{FEX}	Expander Input Low Current		-1.65		-1.25	-1.65		-1.65	mA	V_{CC} = 20V
			-1.33		-0.90	-1.33		-1.33	mA	V_{CC} = 15V
			-1		-0.75	-1		-1	mA	V_{CC} = 10.8V
										V_{FEX} = 0.9V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 20V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-9	-25	-9	-15	-25	-9	-25	mA	V_{CC} = 20V Inputs and Outputs Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		5		4	5		5	mA	V_{CC} = 20V Inputs High
I_{PDL}	Low Level Power Dissipation		2.5		1.5	2.5		2.5	mA	V_{CC} = 20V Inputs Low
TPD+	Turn-Off Delay				160	250			nS	V_{CC} = 15V
TPD-	Turn-On Delay				50	100			nS	See Test Circuit

NOTE: 1) The node can be expanded using the DTL 9933 or BAY 74 diodes

CONNECTION DIAGRAMS (top view)

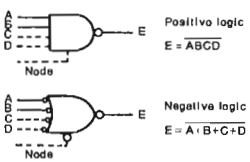


H 122

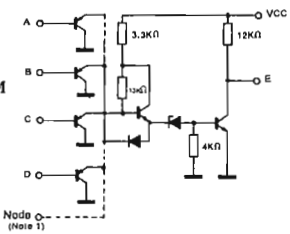


H 124

LOGIC FUNCTION



SCHEMATIC DIAGRAM
(one gate only)



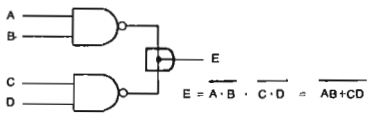
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	18.5		18.5	18		18.5		V	V_{CC} = 20V
		13.5		13.5	14		13.5		V	V_{CC} = 15V } I_{OH} = -50μA
		9.3		9.3	9.8		9.3		V	V_{CC} = 10.8V
										V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1.5		0.2	1.5		1.5	V	V_{CC} = 20V I_{OL} = 15mA or V_{CC} = 15V I_{OL} = 12mA or V_{CC} = 10.8V I_{OL} = 9mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V } V_F = 1.5V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_{FEX}	Expander Input Low Current (H 124 only)		-1.65		-1.25	-1.65		-1.65	mA	V_{CC} = 20V
			-1.33		-0.90	-1.33		-1.33	mA	V_{CC} = 15V } V_{FEX} = 2V
			-1		-0.75	-1		-1	mA	V_{CC} = 10.8V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 20V V_R = 20V
I_{CEX}	Output Leakage Current		45			45		45	μA	V_{CC} = 20V V_{CEX} = 20V
I_{SC}	Output Short Circuit Current	-1.15	-2.5	-1.15	-2	-2.5	-1.15	-2.5	mA	V_{CC} = 20V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		7.5		6	7.5		7.5	mA	V_{CC} = 20V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2.5		1.5	2.5		2.5	mA	V_{CC} = 20V Inputs Low
TPD+	Turn-Off Delay				250	400			nS	V_{CC} = 15V } See Test Circuit
TPD-	Turn-On Delay				40	100			nS	V_{CC} = 15V

NOTES: 1) The node can be expanded using diode EB 383 or BAY 72
2) For H 124 only

WIRED - OR CONNECTION

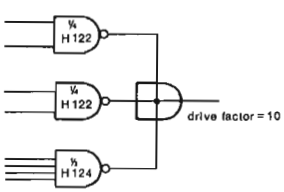
Outputs of H 122 and H 124 may be tied together for the wired - OR function.



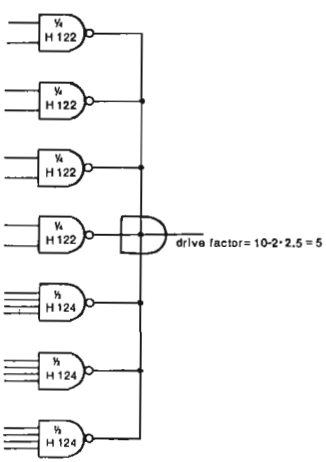
If 2, 3, 4, or 5 H 122 (or H 124) are OR-ed, the drive factor is 10.

For each additional gate over 5 a unit load of 2.5 should be subtracted from the drive factor of the gate.

EXAMPLE 1

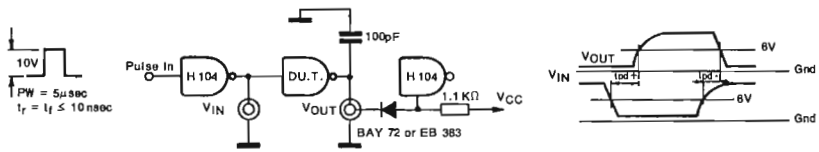


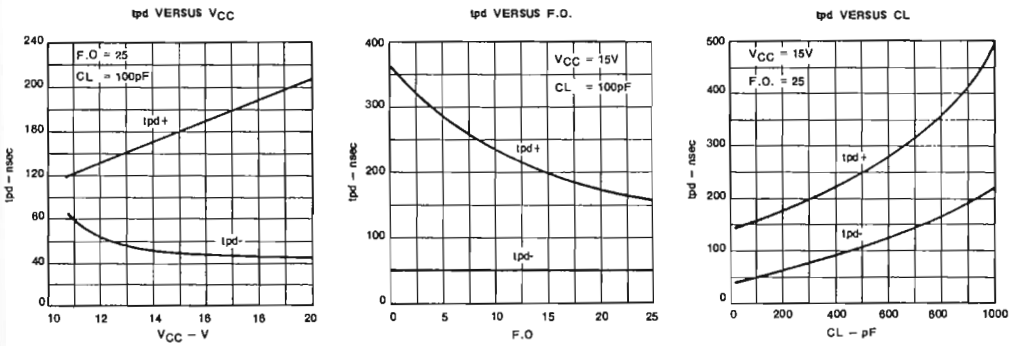
EXAMPLE 2



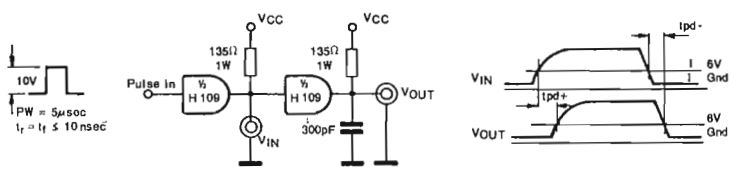
SWITCHING TIME TEST CIRCUITS

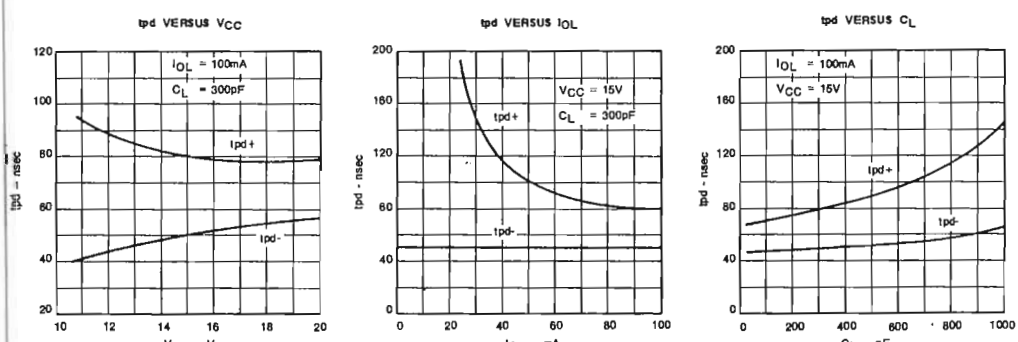
Gates H102-H103-H104



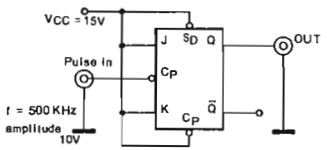


Power Gate H 109

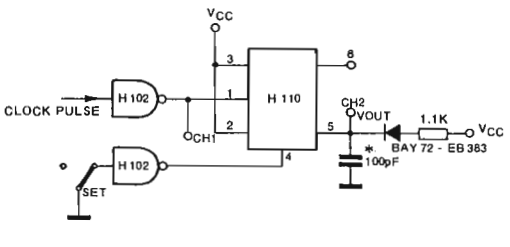




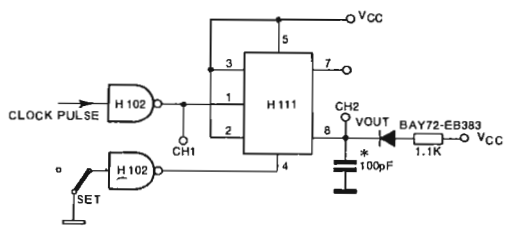
Dual J-K Flip-Flops H 110-H 111

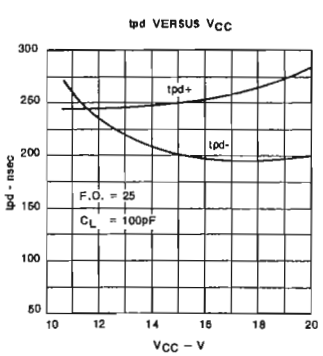


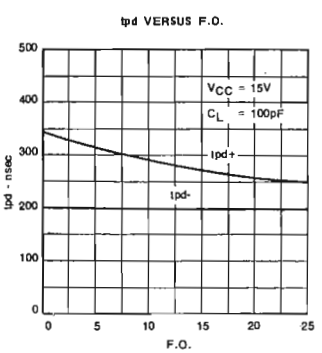
Dual J-K Flip-Flop H 110

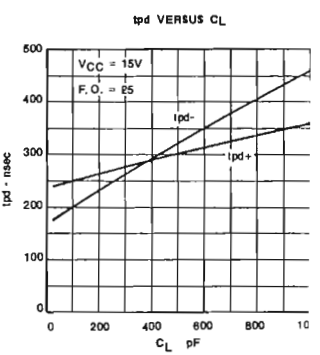


Dual J-K Flip-Flop H 111



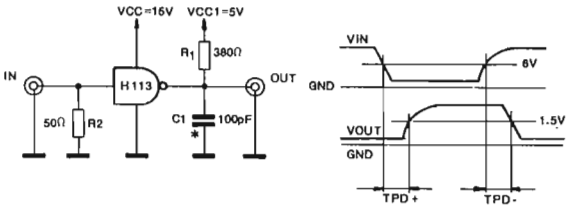


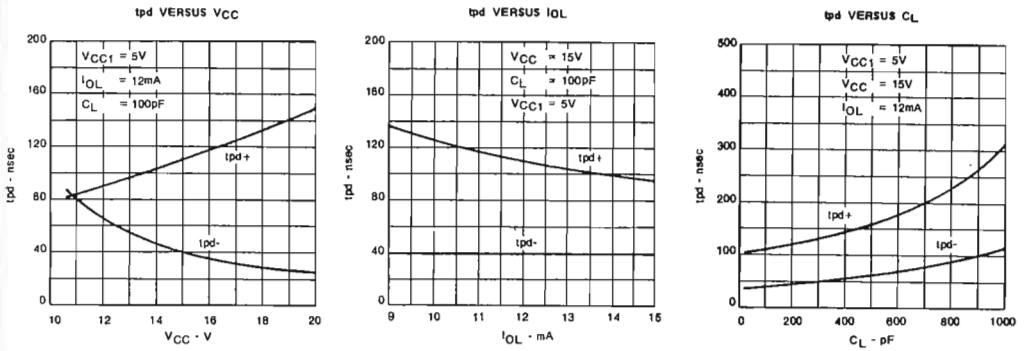




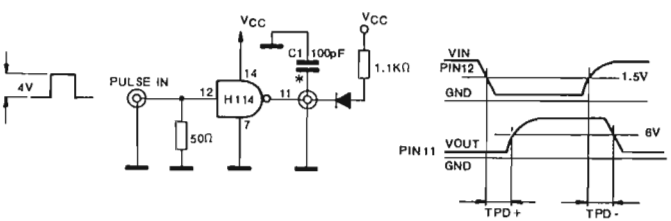
* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

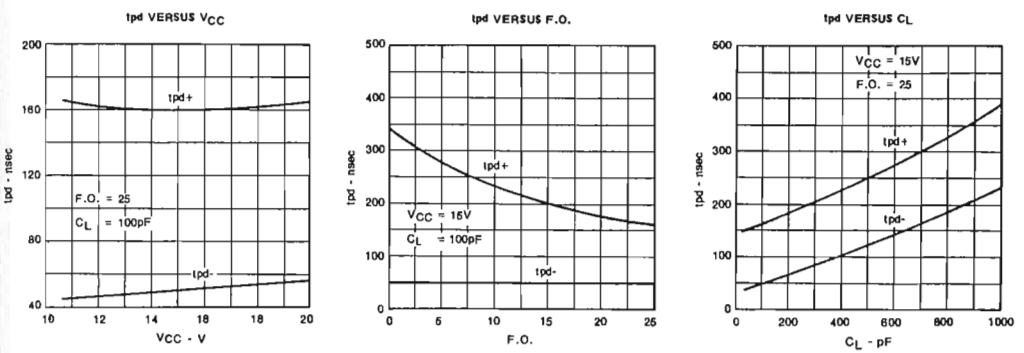
High to Low Level Quad Converter H113





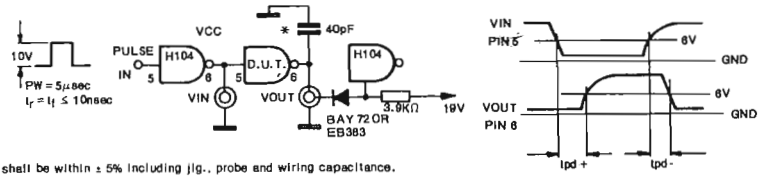
Low to High Level Quad Converter H114





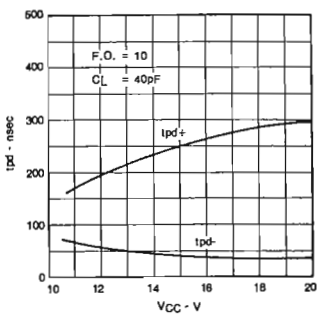
* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

Gates With Passive Pull-Up H 122 - H 124

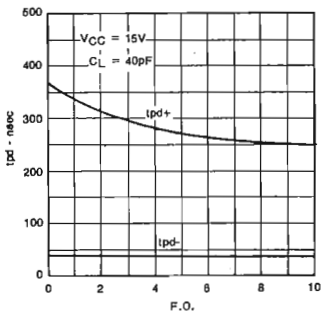


* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

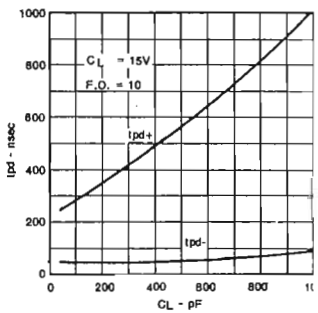
tpd VERSUS V_{CC}



tpd VERSUS F.O.

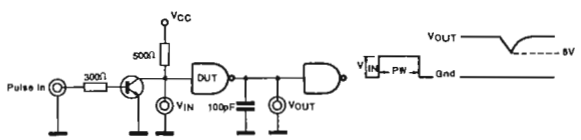


tpd VERSUS C_L

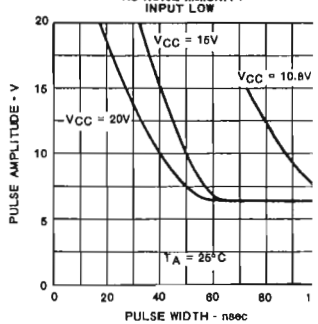


AC NOISE IMMUNITY TEST CIRCUIT

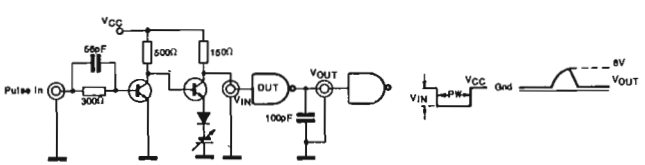
Input low



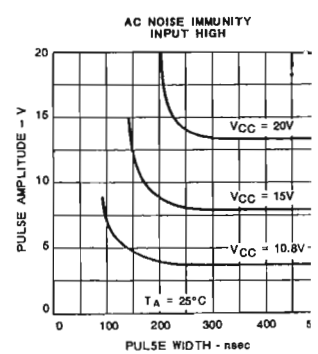
AC NOISE IMMUNITY INPUT LOW



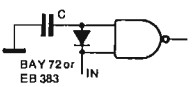
Input high



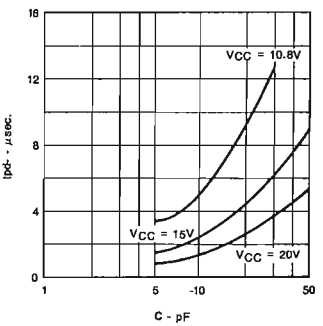
AC NOISE IMMUNITY INPUT HIGH

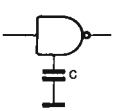


SLOW DOWN OF TPD-

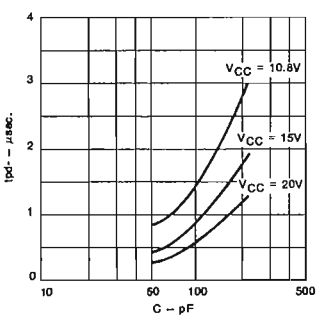


tpd- VERSUS CAPACITANCE





tpd- VERSUS CAPACITANCE



Expandable dual 2-wide 2-input AND-OR-INVERT gate

STANDARD TEMPERATURE RANGE
0° C to 75° C
INTERMEDIATE TEMPERATURE RANGE
-40° C to 85° C

- ACTIVE PULL-UP OUTPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- 14-PIN CERAMIC DIP

ORDERING NUMBERS

H105 D1 (Standard Temperature Range)
H105 D6 (Intermediate Temperature Range)

The H105 is a dual unit with each unit consisting of two-2 input AND gates (one with an input expander node available) that are internally ORed together into an inverting output configuration.
In accordance with the High Level Logic family characteristics, it offers the advantages of 5V DC noise immunity, high segnal levels, wide supply voltage tolerances and unusually low fan-in. These features make the H105 particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.

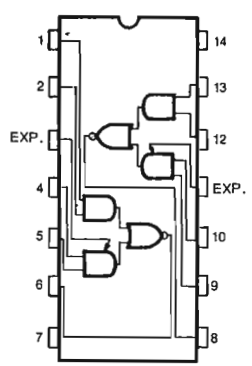
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	H105 D1	22V
	H105 D6	18V
Input Voltage	H105 D1	-0.5V to 20V
	H105 D6	-0.5V to 16V
Storage Temperature Range		-65° C to 150° C

OPERATING CONDITIONS

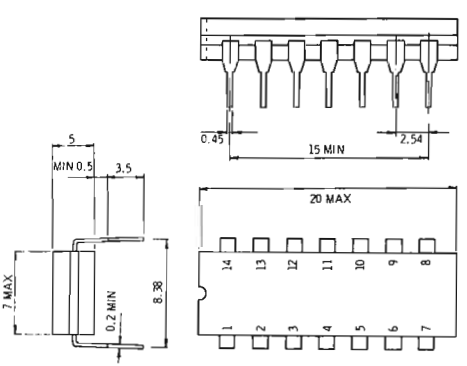
Temperature Range	H105 D1	0° C to 75° C
	H105 D6	-40° C to 85° C
Supply Voltage	H105 D1	10.8V to 20V
	H105 D6	10.8V to 16V

CONNECTION DIAGRAM



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14 pin ceramic DIP



Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8 V to 20 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	18.5 13.5 9.3	19 14 9.8		V V V	V_{CC} = 20 V I_{OH} = -200 μA V_{CC} = 15 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 20 V I_{OL} = 15 mA or V_{CC} = 15 V I_{OL} = 12 mA or V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guarsnteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.1 -0.08 -0.06	-0.6 -0.48 -0.36	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_F = 1.5 V
I_{FEX}	Expander Input Low Current		-1.25 -0.90 -0.75	-1.65 -1.33 -1	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_{FEX} = 2 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 20 V V_R = 20 V
I_{SC}	Output Short Circuit Current	-9	-15	-25	mA	V_{CC} = 20 V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		9.5	12.5	mA	V_{CC} = 20 V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		3.0	5	mA	V_{CC} = 20 V Inputs Low
t_{pd1}	Turn-Off Delay		160		ns	V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	

ELECTRICAL CHARACTERISTICS (T_A = -40°C to 85°C. V_{CC} = 10.8 V to 16 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5 9.3	15 9.8		V V	V_{CC} = 16 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16 V I_{OL} = 12.5 mA V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
I_{FEX}	Expander Input Low Current		-0.9 -0.75	-1.4 -1	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_{FEX} = 2 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 16 V V_R = 16 V
I_{SC}	Output Short Circuit Current	-6.5	-13.5	-20	mA	V_{CC} = 16 V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6.2	8.7	mA	V_{CC} = 16 V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2.8	4	mA	V_{CC} = 16 V Inputs Low
t_{pd1}	Turn-Off Delay		180		ns	V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	

HLL INTEGRATED CIRCUIT

H112

Hex inverter open collector output

EXTENDED TEMPERATURE RANGE
-55°C to 125°C

- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY 5V at V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS and COS/MOS IC's (NOTE)
- 14-PIN CERAMIC PACKAGE

The H112 hex inverter is designed to drive low current lamps, interface with discrete components, and facilitate the implementation of the Wired Collector function with minimum power dissipation.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

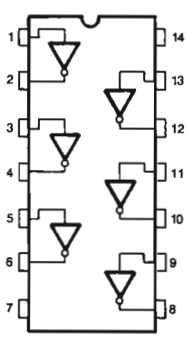
Supply Voltage V_{CC}, continuous			18V
Input Voltage	-0.5V	to	16V
Storage Temperature Range	-65°C	to	150°C

OPERATING CONDITIONS

Temperature Range	-55°C	to	125°C
Supply Voltage	10.8V	to	16V

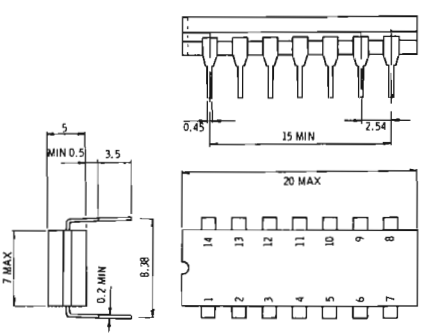
ORDERING NUMBER
H112 D2

CONNECTION DIAGRAM



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14-pin ceramic package



NOTE: all dimensions in mm.

NOTE: For details please refer to MOS IC's data sheets

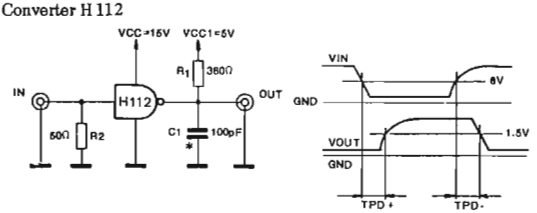
Hex inverter open collector output **H112**

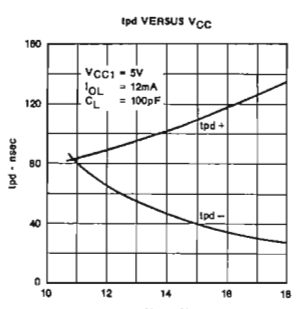
EXTENDED TEMPERATURE RANGE

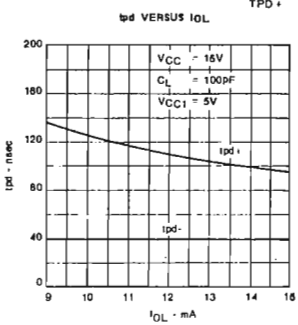
ELECTRICAL CHARACTERISTICS (T_A = -55°C to 125°C, V_{CC} = 10.8 V to 16 V)

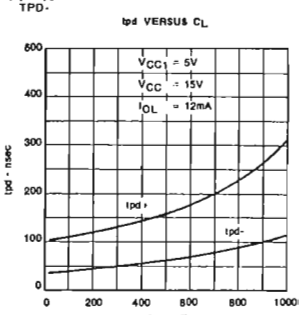
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL}	Output Low Voltage		0.2	1.5	V	V_{CC} = 16 V I_{OL} = 12.5 mA V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
I_R	Reverse Input Current		0.1	7	μA	V_{CC} = 16 V V_R = 16 V
I_{CEX}	Output Leakage Current			80	μA	V_{CC} = 16 V V_{CEX} = 16 V
I_{PDH}	High Level Power Dissipation Current (Each Gate)			4	mA	V_{CC} = 16 V Input High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)			2	mA	V_{CC} = 16 V Input Low
t_{pd1}	Turn-Off Delay		110		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		40		ns	}

High to Low Level Quad Converter H 112









Hex inverter open collector output

STANDARD TEMPERATURE RANGE
0° C to 75° C
INTERMEDIATE TEMPERATURE RANGE
-40° C to 85° C

- OPEN COLLECTOR OUTPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- HIGH FAN–OUT 25 (WORST CASE)
- 14–PIN CERAMIC DIP

ORDERING NUMBERS

H112 D1 (Standard Temperature Range)
H112 D6 (Intermediate Temperature Range)

The H112 hex inverter is designed to drive low current lamps, interface with discrete components, and facilitate the implementation of the Wired Collector function with minimum power dissipation.
Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H112 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

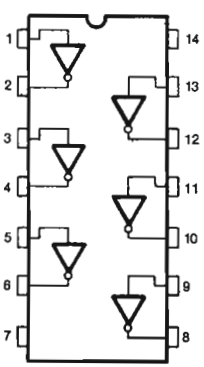
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	H112D1	22V
	H112D6	18V
Input Voltage	H112D1	-0.5V to 20V
	H112D6	-0.5V to 16V
Storage Temperature Range		-65° C to 150° C

OPERATING CONDITIONS

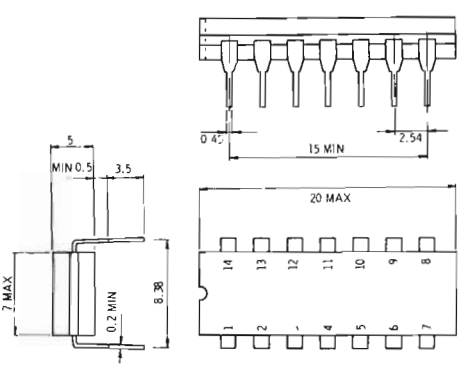
Temperature Range	H112D1	0° C to 75° C
	H112D6	-40° C to 85° C
Supply Voltage	H112D1	10.8V to 20V
	H112D6	10.8V to 16V

CONNECTION DIAGRAM



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14 pin ceramic DIP



Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8 V to 20 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL}	Output Low Voltage		0.2	1.5	V	V_{CC} = 20 V, I_{OL} = 15 mA or V_{CC} = 15 V, I_{OL} = 12 mA or V_{CC} = 10.8 V, I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.1 -0.08 -0.06	-0.6 -0.48 -0.36	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_F = 1.5 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 20 V, V_R = 20 V
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 20 V, V_{CEX} = 20 V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.5	6	mA	V_{CC} = 20 V, Input High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.5	2.5	mA	V_{CC} = 20 V, Input Low
t_{pd1}	Turn-Off Delay		110		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		40		ns	}

ELECTRICAL CHARACTERISTICS (T_A = -40°C to 85°C, V_{CC} = 10.8 V to 16 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL}	Output Low Voltage		0.2	1.5	V	V_{CC} = 16 V, I_{OL} = 12.5 mA V_{CC} = 10.8 V, I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 16 V, V_R = 16 V
I_{CEX}	Output Leakage Current			80	μA	V_{CC} = 16 V, V_{CEX} = 16 V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		3.5	5	mA	V_{CC} = 16 V, Input High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.2	2	mA	V_{CC} = 16 V, Input Low
t_{pd1}	Turn-Off Delay		110		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		40		ns	}

Strobed hex inverter open collector output

EXTENDED TEMPERATURE RANGE
-55°C to 125°C

- ENABLE AND STROBE INPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY 5V at V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS and COS/MOS IC's (NOTE)
- 16-PIN CERAMIC PACKAGE

The H115 hex inverter is designed to drive low-current lamps, interface with discrete components, and facilitate the implementation of the Wired Collector function with minimum power dissipation.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous			18V
Input Voltage	-0.5V	to	16V
Storage Temperature Range	-65°C	to	150°C

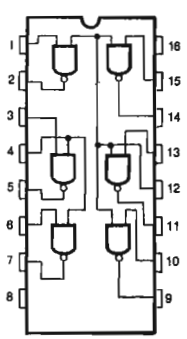
OPERATING CONDITIONS

Temperature Range	-55°C	to	125°C
Supply Voltage	10.8V	to	16V

ORDERING NUMBER

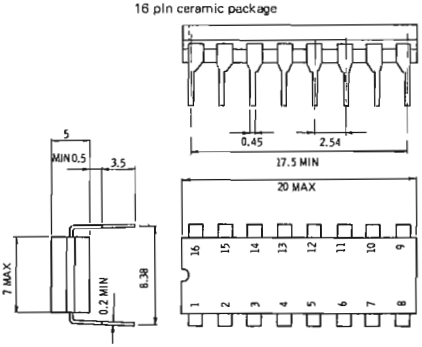
H115 D2

CONNECTION DIAGRAM



GND = PIN 8
V_{CC} = PIN 16

PHYSICAL DIMENSIONS
16 pin ceramic package



NOTE: all dimensions in mm.

NOTE: For details please refer to MOS IC's data sheets

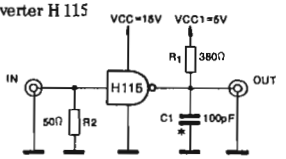
Strobed hex inverter open collector output **H115**

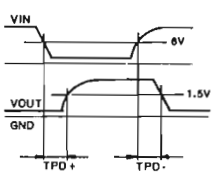
EXTENDED TEMPERATURE RANGE

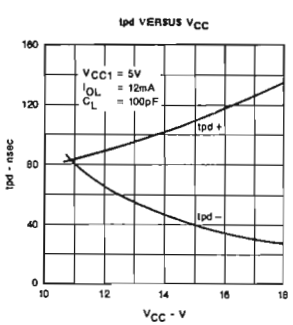
ELECTRICAL CHARACTERISTICS (T_A = -55°C to 125°C V_{CC} = 10.8 V to 16 V)

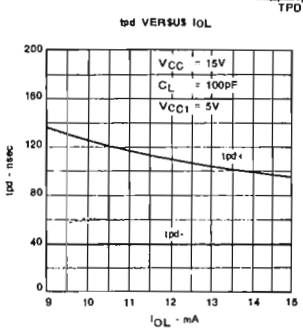
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL}	Output Low Voltage		0.2	1.5	V	V_{CC} = 16 V I_{OL} = 12.5 mA V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
I_R	Reverse Input Current		0.1	7	μA	V_{CC} = 16 V V_R = 16 V
I_{CEX}	Output Leakage Current			80	μA	V_{CC} = 16 V V_{CEX} = 16 V
I_{PDH}	High Level Power Dissipation Current (Each Gate)			4	mA	V_{CC} = 16 V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)			2	mA	V_{CC} = 16 V Inputs Low
t_{pd1}	Turn-Off Delay		110		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		40		ns	}

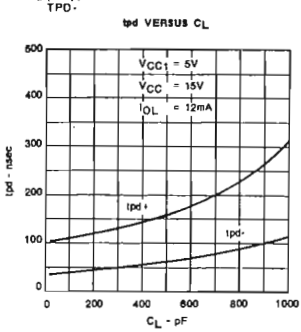
High to Low Level Quad Converter H 115











Strobed hex inverter open collector output

STANDARD TEMPERATURE RANGE
0° C to 75° C
INTERMEDIATE TEMPERATURE RANGE
-40° C to 85° C

- OPEN COLLECTOR OUTPUT
- ENABLE AND STROBE INPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- 16–PIN CERAMIC DIP

ORDERING NUMBERS

H115 D1 (Standard Temperature Range)
H115 D6 (Intermediate Temperature Range)

The H115 hex inverter is designed to drive low-current lamps, interface with discrete components, and facilitate the implementation of the Wired Collector function with minimum power dissipation.
Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H115 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

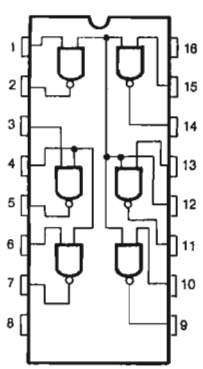
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	H115D1	22V
	H115D6	18V
Input Voltage	H115D1	-0.5V to 20V
	H115D6	-0.5V to 16V
Storage Temperature Range		-65° C to 150° C

OPERATING CONDITIONS

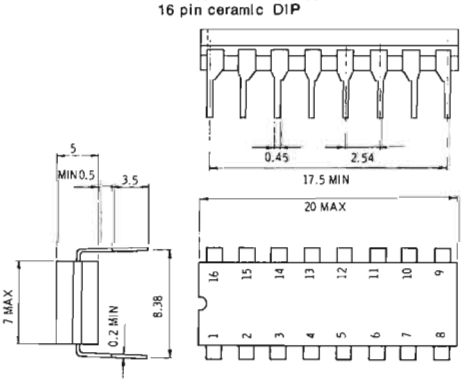
Temperature Range	H115D1	0° C to 75° C
	H115D6	-40° C to 85° C
Supply Voltage	H115D1	10.8V to 20V
	H115D6	10.8V to 16V

CONNECTION DIAGRAM



GND = PIN 8
V_{CC} = PIN 16

PHYSICAL DIMENSIONS
16 pin ceramic DIP



NOTE.
1) Board-drilling dimensions should equal your practice for a conventional 0,51 mm. diameter lead.
2) All dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8 V to 20 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL}	Output Low Voltage		0.2	1.5	V	V_{CC} = 20 V, I_{OL} = 15 mA or V_{CC} = 15 V, I_{OL} = 12 mA or V_{CC} = 10.8 V, I_{OL} = 9 mA, $V_{IN} = V_{IH}$ (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Thereshold for All Inputs
*I_F	Input Low Current		-0.1	-0.6	mA	V_{CC} = 20 V
			-0.08	-0.48	mA	V_{CC} = 15 V
			-0.06	-0.36	mA	V_{CC} = 10.8 V } V_F = 1.5 V
**I_R	Reverse Input Current		0.1	5	µA	V_{CC} = 20 V, V_R = 20 V
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 20 V, V_{CEX} = 20 V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.5	6	mA	V_{CC} = 20 V, Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.5	2.5	mA	V_{CC} = 20 V, Inputs Low
t_{pd1}	Turn-Off Delay		110		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		40		ns	}

ELECTRICAL CHARACTERISTICS (T_A = -40°C to 85°C, V_{CC} = 10.8 V to 16 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL}	Output Low Voltage		0.2	1.5	V	V_{CC} = 16 V, I_{OL} = 12.5 mA or V_{CC} = 10.8 V, I_{OL} = 9 mA, $V_{IN} = V_{IH}$ (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
*I_F	Input Low Current		-0.08	-0.5	mA	V_{CC} = 16 V
			-0.06	-0.36	mA	V_{CC} = 10.8 V } V_F = 1.5 V
**I_R	Reverse Input Current		0.1	5	µA	V_{CC} = 16 V, V_R = 16 V
I_{CEX}	Output Leakage Current			80	µA	V_{CC} = 16 V, V_{CEX} = 16 V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		3.5	5	mA	V_{CC} = 16 V, Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.2	2	mA	V_{CC} = 16 V, Inputs Low
t_{pd1}	Turn-Off Delay		110		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		40		ns	}

* Input Low Current : at pin 4 is equal to 2 · I_F; at pin 12 is equal to 4 · I_F
** Reverse Input Current : at pin 4 is equal to 2 · I_R; at pin 12 is equal to 4 · I_R

HLL INTEGRATED CIRCUIT

One-shot multivibrator

EXTENDED TEMPERATURE RANGE
-55°C to 125°C

- MONOSTABLE AND ASTABLE FUNCTIONING
- VERY WIDE DURATION RANGE (FROM 1 μsec TO MORE THAN 100 sec.)
- OUTPUT PULSE WIDTH DEFINED ONLY BY EXTERNAL TIMING NETWORK
- PULSE TRIGGERING LARGELY INDEPENDENT OF THE INPUT PULSE WIDTH AND FORM
- EXTREMELY STABLE OPERATION WITH RESPECT TO POWER SUPPLY AND TEMPERATURE
- COMPLEMENTARY OUTPUTS
- POSSIBILITY OF DRIVING TTL AND DTL CIRCUITS
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY 5V at V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS and COS/MOS IC's (NOTE)
- 14-PIN CERAMIC PACKAGE

The H 117 is a monostable multivibrator designed for a wide range of pulse duration, practically independent of variation in ambient temperature and power supply voltage.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous			18V
Input Voltage	-0.5V	to	16V
Storage Temperature Range	-55°C	to	150°C

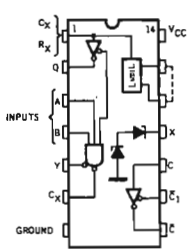
OPERATING CONDITIONS

Temperature range	-55°C	to	125°C
Supply Voltage	10.8V	to	16V

ORDERING NUMBER

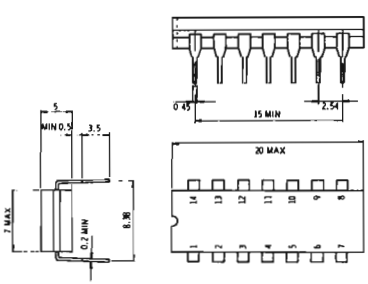
H 117 D2

CONNECTION DIAGRAM
(Top view)



X = Pre-limiter connection

PHYSICAL DIMENSIONS
14-pin ceramic package



NOTE: all dimensions in mm.

NOTE: For details please refer to MOS IC's data sheets

one-shot multivibrator **H117**

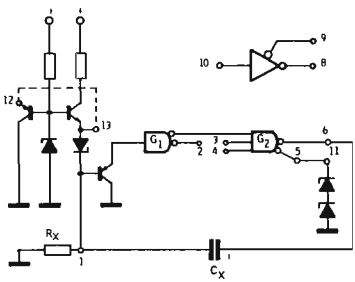
EXTENDED TEMPERATURE RANGE

DESCRIPTION

This monolithic HLL monostable multivibrator features DC triggering from gated negative going input. Both positive and negative going output pulses are provided, with the customary large HLL family fan-out. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Input pulses, with transition time as slow as 0.2 V/ms, allow jitter-free output. DC noise immunity, both V_{CC} and ground, as high as 5V at V_{CC} = 15V is guaranteed. Once fired the output is independent of further transition of the inputs and is a function only of the external timing components. Input pulses may be of any duration relative to the output pulse. Output pulse duration may vary from 1 µsec to more than 100 sec by choosing appropriate timing components. Output rise and fall times are independent of pulse length. Pulse width is virtually independent of V_{CC} (*1) and temperature (*2); in most applications pulse stability will only be determined by C_X and R_X stability. Jitter-free operation is maintained over the full temperature and V_{CC} range, for nearly six decades of timing capacitance and one decade of timing resistance. Throughout these ranges, pulse width is defined by the relationship $T_{PW} \simeq 0.83\ C_X\ R_X$. Duty cycles as high as 95 % are achieved when using R_X = 100 kΩ and C_X = 100 µF at V_{CC} = 15V.

*1) With a typical variation of 0.1% per Volt
*2) With a typical variation of 0.02% per °C for R_X = 100kΩ and $C_X \geq 1000$pF.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC} = 10.8V to 16V, T_A = - 55°C to 125°C)

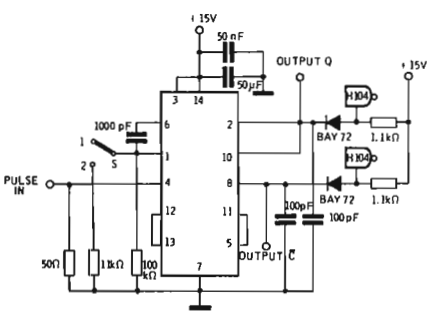
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5 9.3	15 9.8		V V	V_{CC} = 16V V_{CC} = 10.8V } I_{OH} = - 200 µA
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16V I_{OL} = 12 mA or V_{CC} = 10.8V I_{OL} = 9 mA
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold at inputs A, B and C.
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold at inputs A, B and C.
I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V } V_F = 1,5V at pins A, B and C.
I_R	Reverse Input Current		0.1	7	µA	V_{CC} = 16V V_R = 16V at pins A, B and C.
I_{SC}	Output Short Circuit Current	-9		-25	mA	V_{CC} = 16V at pins Q and $\overline{C}$.
I_{PD}	Power Dissipation Current		15	25	mA	V_{CC} = 16V all inputs high.

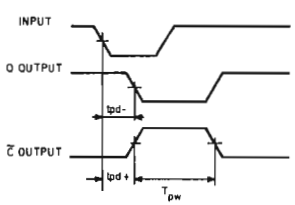
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
t_{pd+}	Turn-Off Delay Inputs 3 and 4 to Output 8		700	1000	ns	C_X = 1000pF R_X = 10kΩ V_{CC} = 15V
t_{pd-}	Turn-On Delay Inputs 3 and 4 to Output 2		500	800	ns	C_X = 1000pF R_X = 10kΩ V_{CC} = 15V
t_{PW}	Duration of Trigger Pulse	1			µs	C_X = 1000pF R_X = 10 kΩ
R_X	Maximum Timing Resistance	100			kΩ	
C_X	Timing Capacitance					No limit if trigger pulse is shorter than output pulse. Otherwise $C_X \leq$ 200 µF.
T_{PW}	Output Pulse Width (See note)	75	83	91	µs	C_X = 1000pF R_X = 100 kΩ

Note : Output pulse width calculation : $T_{PW} \simeq 0.83\ R_X\ C_X$

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



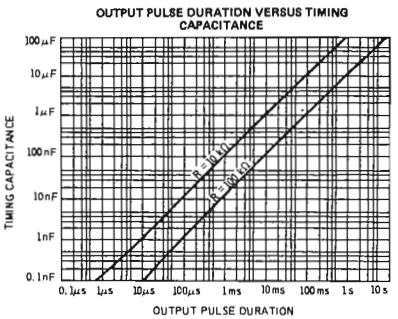


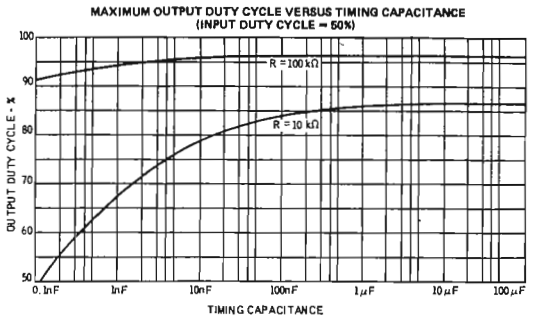
NOTES :

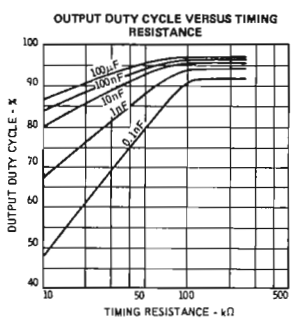
1) When testing t_{pd} switch S must be in position 2.
2) When testing T_{pw} switch S must be in position 1.

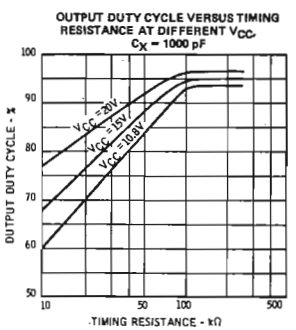
EXTENDED TEMPERATURE RANGE

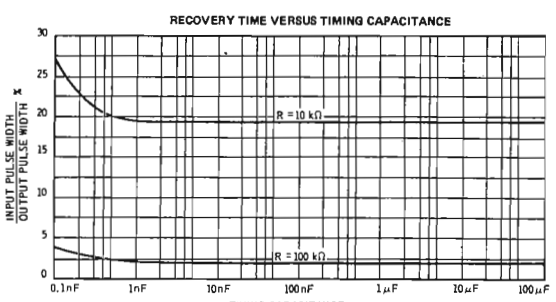
TYPICAL ELECTRICAL CHARACTERISTICS (V_{CC}=15V, T_A=25°C unless otherwise noted)





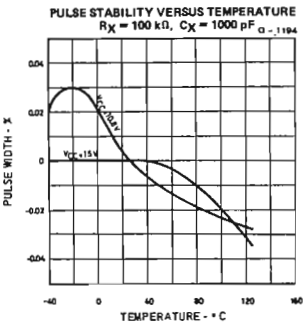


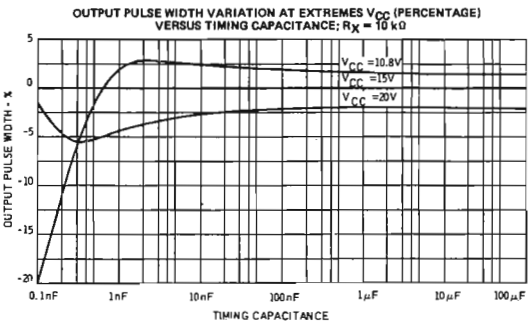


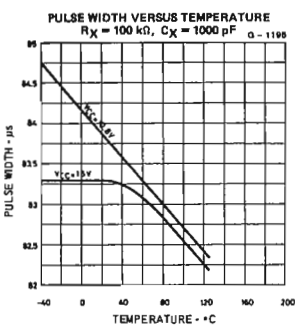


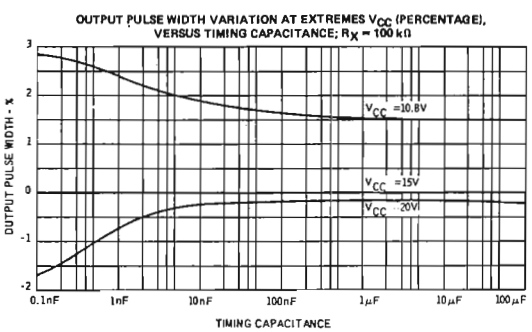
EXTENDED TEMPERATURE RANGE

TYPICAL ELECTRICAL CHARACTERISTICS (V_{CC} = 15V, T_A =25°C unless otherwise noted)









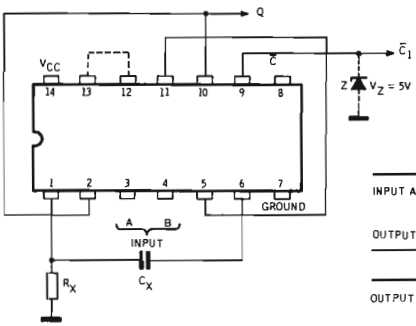
EXTENDED TEMPERATURE RANGE

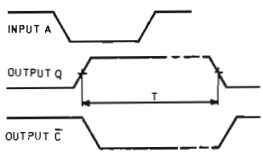
APPLICATIONS

MONOSTABLE MULTIVIBRATOR TRIGGERING ON PULSE TRAILING EDGE, COMPLEMENTARY OUTPUTS

t_n input		t_{n+1} input		Output
A	B	A	B	Q $\overline{Q}$
1	1	0	1	one shot
1	0	0	0	inhibit
1	1	1	0	one shot
0	1	0	0	inhibit

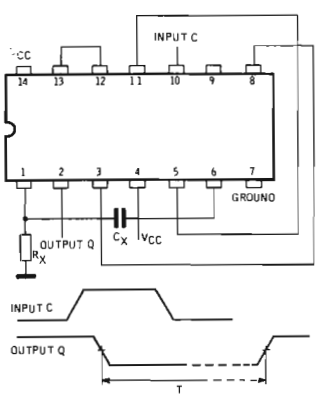
t_n = time before input transition
t_{n+1} = time after input transition



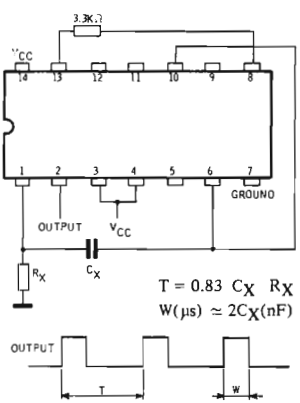


NOTES :
- If pin 5 is connected to pin 11 and pin 12 is connected to pin 13, $T = 0.83\ C_X\ R_X$ at V_{CC} = 10.8V to 20V. If pins 5, 11, 12, 13 are not connected, $T = 1.2\ R_X\ C_X$ at V_{CC} = 16V to 20V.
- If diode Z is connected, C_1 may drive TTL or DTL circuits.

MONOSTABLE MULTIVIBRATOR TRIGGERING ON PULSE LEADING EDGE

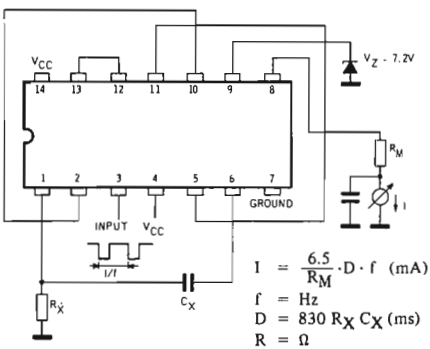


HIGH STABILITY CLOCK



APPLICATIONS (Contd.)

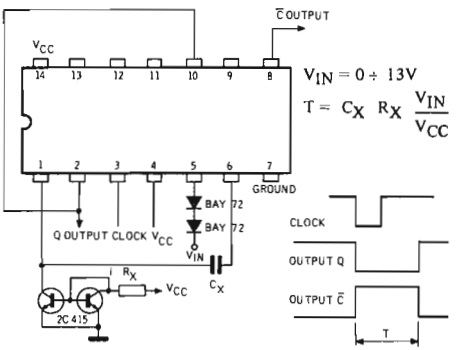
FREQUENCY TO CURRENT CONVERTER



$$I = \frac{6.5}{R_M} \cdot D \cdot f \ (mA)$$

f = Hz
D = 830 $R_X C_X$ (ms)
R = Ω
C_X = F

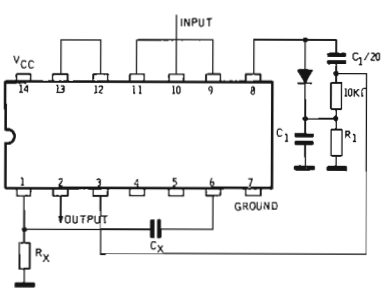
VOLTAGE TO PULSE WIDTH CONVERTER

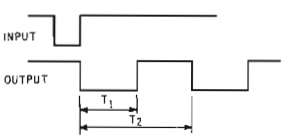


$V_{IN} = 0 \div 13V$

$$T = C_X R_X \frac{V_{IN}}{V_{CC}}$$

DOUBLE PULSE GENERATOR





V_{CC} = 14.5 to 17V
$T_1 = 0.83\ R_X\ C_X$
$T_2 = 0.55\ R_1\ C_1$

One-shot multivibrator

STANDARD TEMPERATURE RANGE,
0°C to 75°C
INTERMEDIATE TEMPERATURE RANGE,
- 40°C to 85°C

- MONOSTABLE AND ASTABLE FUNCTIONING
- VERY WIDE DURATION RANGE (FROM 1 μsec TO MORE THAN 100 sec.)
- OUTPUT PULSE WIDTH DEFINED ONLY BY EXTERNAL TIMING NETWORK
- PULSE TRIGGERING LARGELY INDEPENDENT OF THE INPUT PULSE WIDTH AND FORM
- EXTREMELY STABLE OPERATION WITH RESPECT TO POWER SUPPLY AND TEMPERATURE
- COMPLEMENTARY OUTPUTS
- POSSIBILITY OF DRIVING TTL AND DTL CIRCUITS
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC}=15V
- HIGH FAN-OUT, 25 MINIMUM
- 14-PIN CERAMIC DIP

ORDERING NUMBERS

H 117 D1 (Standard Temperature Range)
H 117 D6 (Intermediate Temperature Range)

The H 117 is a monostable multivibrator designed for a wide range of pulse duration, practically independent of variation in ambient temperature and power supply voltage. Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC ground and supply voltage noise immunity at V_{CC} = 15V, high signal levels, wide supply voltage tolerances and unusually high fan-out. These features make the family particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.

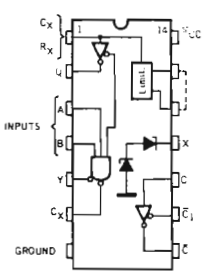
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	
H 117 D1	22V
H 117 D6	18V
Input Voltage	
H 117 D1	- 0.5V to 20V
H 117 D6	- 0.5V to 16V
Storage Temperature Range	- 55°C to 150°C

OPERATING CONDITIONS

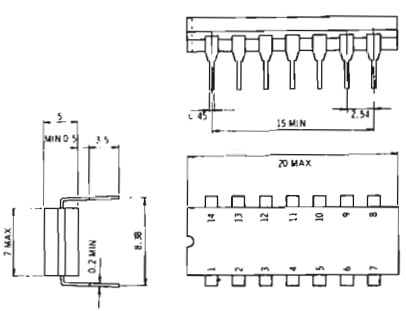
Temperature range	
H 117 D1	0°C to 75°C
H 117 D6	- 40°C to 85°C
Supply Voltage	
H 117 D1	10.8V to 20V
H 117 D6	10.8V to 16V

CONNECTION DIAGRAM
(Top view)



X = Pre-limiter connection

PHYSICAL DIMENSIONS
14-pin ceramic DIP



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS (V_{CC} = 10.8V to 20V, T_A = 0°C to 75°C)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
V_{OH}	Output High Voltage	18.5	19		V	V_{CC} = 20V
		13.5	14		V	V_{CC} = 15V } I_{OH} = - 200 µA
		9.3	9.8		V	V_{CC} = 10.8V
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 20V I_{OL} = 15 mA or
						V_{CC} = 15V I_{OL} = 12 mA or
						V_{CC} = 10.8V I_{OL} = 9 mA
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold at inputs A, B and C.
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold at inputs A, B and C.
I_F	Input Low Current		-0.1	-0.6	mA	V_{CC} = 20V
			-0.08	-0.48	mA	V_{CC} = 15V } V_F = 1.5V at pins A, B and C.
			-0.06	-0.36	mA	V_{CC} = 10.8V
I_R	Reverse Input Current		0.1	5	µA	V_{CC} = 20V V_R = 20V at pins A, B and C.
I_{SC}	Output Short Circuit Current	-9		-25	mA	V_{CC} = 20V at pins Q and $\overline{C}$.
I_{PD}	Power Dissipation Current		15	25	mA	V_{CC} = 20V all inputs high.

ELECTRICAL CHARACTERISTICS (V_{CC} = 10.8V to 16V, T_A = - 40°C to 85°C)

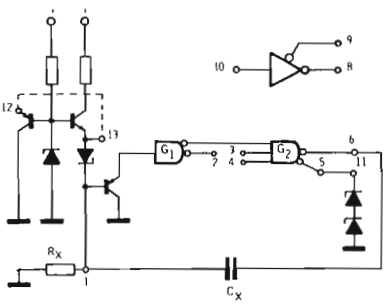
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5	15		V	V_{CC} = 16V } I_{OH} = - 200 µA
		9.3	9.8		V	V_{CC} = 10.8V
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16V I_{OL} = 12 mA or
						V_{CC} = 10.8V I_{OL} = 9 mA
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold at inputs A, B and C.
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold at inputs A, B and C.
I_F	Input Low Current		-0.08	-0.5	mA	V_{CC} = 16V } V_F = 1,5V at
			-0.06	-0.36	mA	V_{CC} = 10.8V } pins A, B and C.
I_R	Reverse Input Current		0.1	5	µA	V_{CC} = 16V V_R = 16V at pins A, B and C.
I_{SC}	Output Short Circuit Current	-9		-25	mA	V_{CC} = 16V at pins Q and $\overline{C}$.
I_{PD}	Power Dissipation Current		15	25	mA	V_{CC} = 16V all inputs high.

DESCRIPTION

This monolithic HLL monostable multivibrator features DC triggering from gated negative going input. Both positive and negative going output pulses are provided, with the customary large HLL family fan-out. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Input pulses with transition time as slow as 0.2 V/ms, allow jitter-free output. DC noise immunity both V_{CC} and ground,as high as 5V at V_{CC} 15V is guaranteed. Once fired the output is independent of further transition of the inputs and is a function only of the external timing components. Input pulses may be of any duration relative to the output pulse. Output pulse duration may vary from 1 µsec to more than 100 sec by choosing appropriate timing components. Output rise and fall times are independent of pulse length. Pulse width is virtually independent of V_{CC} (*1) and temperature (*2); in most applications pulse stability will only be determined by C_X and R_X stability. Jitter-free operation is maintained over the full temperature and V_{CC} range, for nearly six decades of timing capacitance and one decade of timing resistance. Throughout these ranges, pulse width is defined by the relationship $T_{PW} \simeq 0.83\ C_X\ R_X$. Duty cycles as high as 95 % are achieved when using R_X = 100 kΩ and C_X 100 uF at V_{CC} = 15V.

*1) With a typical variation of 0.1% per Volt
*2) With a typical variation of 0.02% per °C for R_X 100k Ω and C_X =1000pF.

LOGIC DIAGRAM

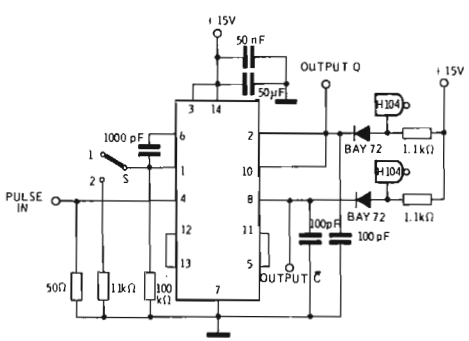


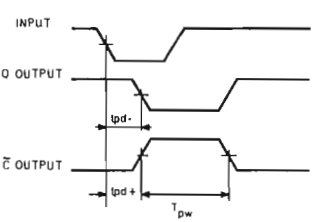
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
t_{pd+}	Turn-Off Delay Inputs 3 and 4 to Output 8		700	1000	ns	C_X = 1000pF, R_X = 10kΩ, V_{CC} = 15V
t_{pd-}	Turn-On Delay Inputs 3 and 4 to Output 2		500	800	ns	C_X = 1000pF, R_X = 10kΩ, V_{CC} = 15V
t_{PW}	Duration of Trigger Pulse	1			us	C_X = 1000pF, R_X = 10 kΩ
R_X	Maximum Timing Resistance	100			kΩ	
C_X	Timing Capacitance					No limit if trigger pulse is shorter than output pulse. Otherwise $C_X \leq$ 200 µF.
T_{PW}	Output Pulse Width (See note)	75	83	91	µs	C_X = 1000pF, R_X = 100 kΩ

Note : Output pulse width calculation : $T_{PW} \simeq 0.83\ R_X\ C_X$

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

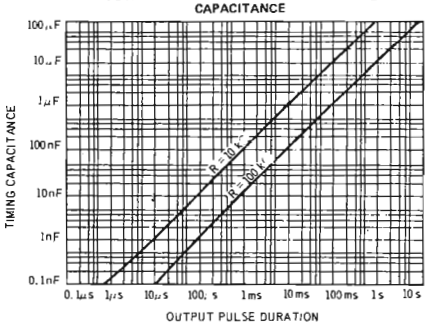




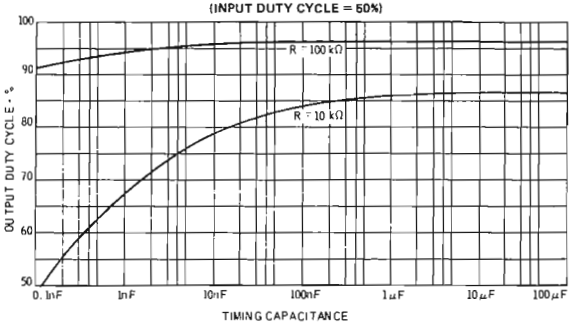
NOTES :
1) When testing t_{pd} switch S must be in position 2.
2) When testing T_{pw} switch S must be in position 1.

TYPICAL ELECTRICAL CHARACTERISTICS (V_{CC} =15V, T_A=25°C unless otherwise noted)

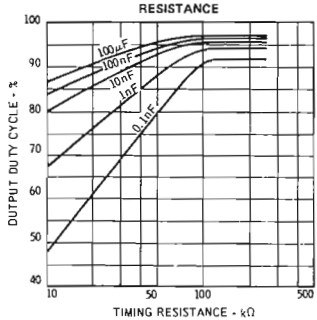
OUTPUT PULSE DURATION VERSUS TIMING CAPACITANCE



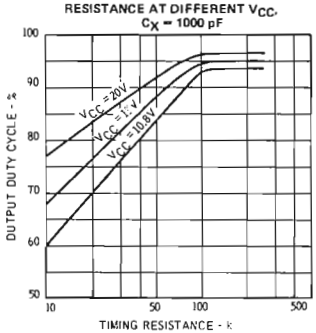
MAXIMUM OUTPUT DUTY CYCLE VERSUS TIMING CAPACITANCE (INPUT DUTY CYCLE = 50%)



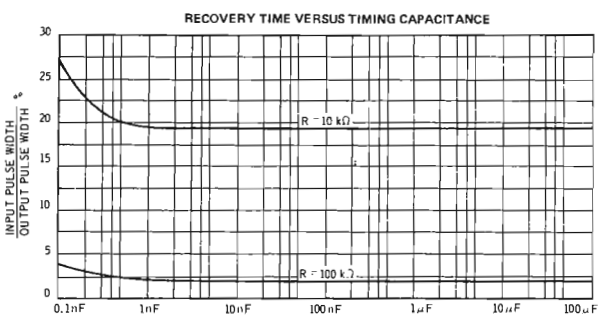
OUTPUT DUTY CYCLE VERSUS TIMING RESISTANCE



OUTPUT DUTY CYCLE VERSUS TIMING RESISTANCE AT DIFFERENT V_{CC}, C_X = 1000 pF

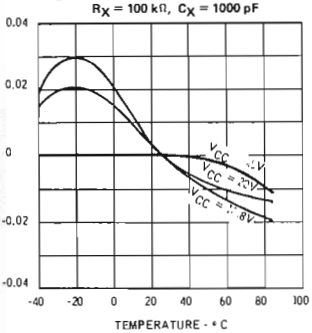


RECOVERY TIME VERSUS TIMING CAPACITANCE

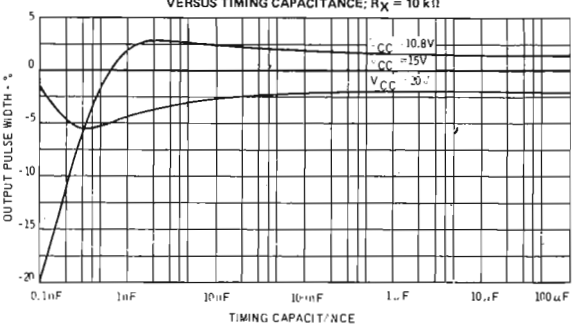


TYPICAL ELECTRICAL CHARACTERISTICS (V_{CC} = 15V, T_A = 25°C unless otherwise noted)

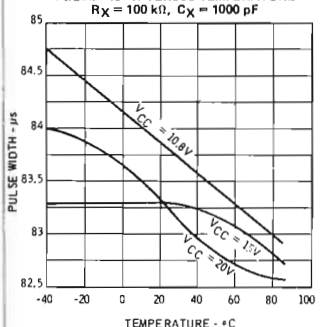
PULSE STABILITY VERSUS TEMPERATURE
R_X = 100 kΩ, C_X = 1000 pF



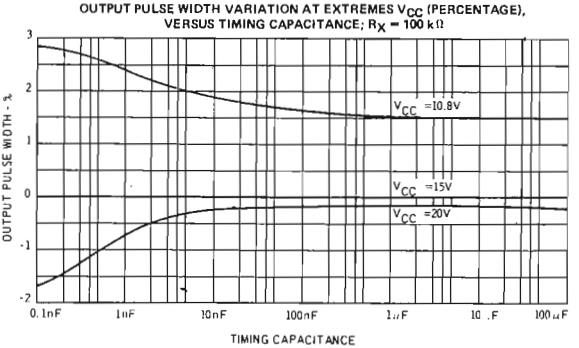
OUTPUT PULSE WIDTH VARIATION AT EXTREMES V_{CC} (PERCENTAGE) VERSUS TIMING CAPACITANCE; R_X = 10 kΩ



PULSE WIDTH VERSUS TEMPERATURE
R_X = 100 kΩ, C_X = 1000 pF



OUTPUT PULSE WIDTH VARIATION AT EXTREMES V_{CC} (PERCENTAGE), VERSUS TIMING CAPACITANCE; R_X = 100 kΩ

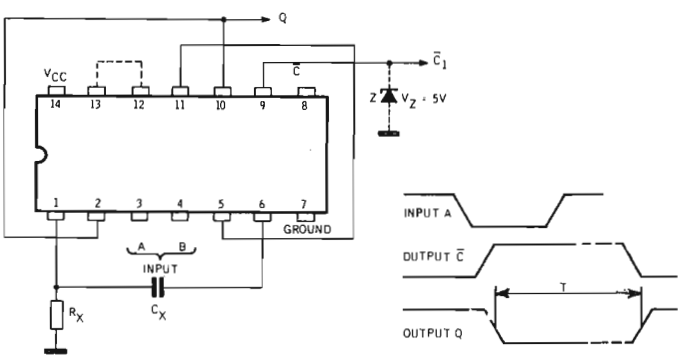


APPLICATIONS

MONOSTABLE MULTIVIBRATOR TRIGGERING ON PULSE TRAILING EDGE, COMPLEMENTARY OUTPUTS

t_n input		t_{n+1} input		Output	
A	B	A	B	Q	$\overline{C}$
1	1	0	1	one shot	
1	0	0	0	inhibit	
1	1	1	0	one shot	
0	1	0	0	inhibit	

t_n = time before input transition
t_{n+1} = time after input transition

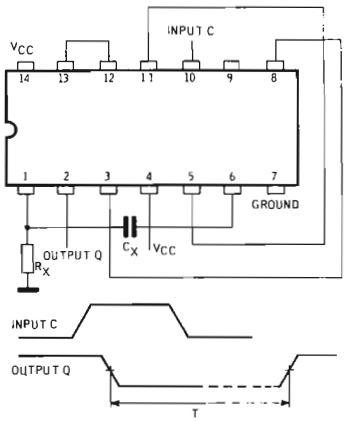


NOTES :

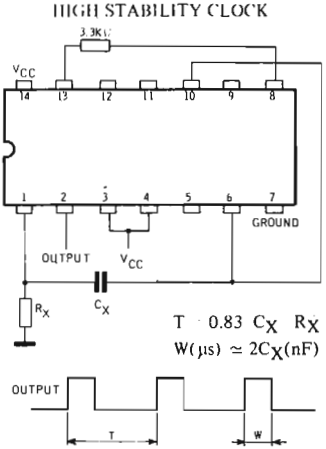
1) If pin 5 is connected to pin 11 and pin 12 is connected to pin 13, $T = 0.83\ C_X\ R_X$ at V_{CC} = 10.8V to 20V. If pins 5, 11, 12, 13 are not connected, $T = 1.2\ R_X\ C_X$ at V_{CC} = 16V to 20V.
2) If diode Z is connected, $\overline{C}_1$ may drive TTL or DTL circuits.

APPLICATIONS (Contd)

MONOSTABLE MULTIVIBRATOR
TRIGGERING ON PULSE LEADING EDGE



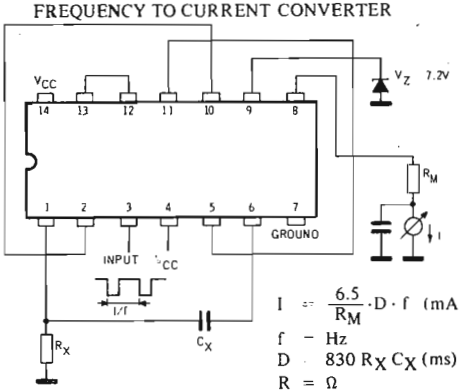
HIGH STABILITY CLOCK



$T = 0.83\ C_X\ R_X$

$W(\mu s) \simeq 2C_X(nF)$

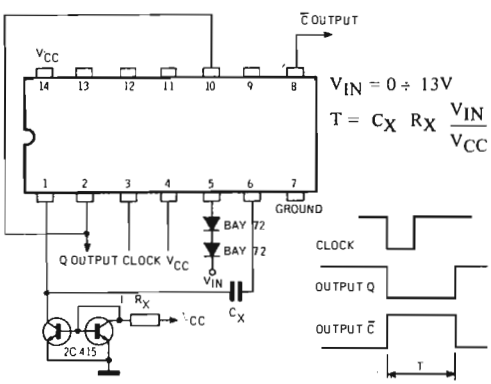
FREQUENCY TO CURRENT CONVERTER



$$I = \frac{6.5}{R_M} \cdot D \cdot f \ (mA)$$

f = Hz
D = $830\ R_X\ C_X$ (ms)
R = Ω
C_X = F

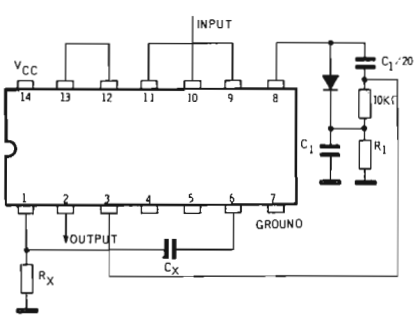
VOLTAGE TO PULSE WIDTH CONVERTER

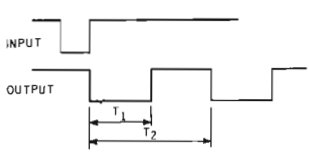


$V_{IN} = 0 \div 13V$

$$T = C_X\ R_X\ \frac{V_{IN}}{V_{CC}}$$

DOUBLE PULSE GENERATOR





V_{CC} = 14.5 to 17V

$T_1 = 0.83\ R_X\ C_X$

$T_2 = 0.55\ R_1\ C_1$

Hex inverter active pull-up output

STANDARD TEMPERATURE RANGE
0°C to 75°C
INTERMEDIATE TEMPERATURE RANGE
-40°C to 85°C

- ACTIVE PULL-UP OUTPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- 14-PIN CERAMIC DIP

ORDERING NUMBERS

H118 D1 (Standard Temperature Range)
H118 D6 (Intermediate Temperature Range)

The H 118 hex inverter performs the function $B=\overline{A}$ and utilizes an active pull-up to minimize output impendance. Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H 118 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

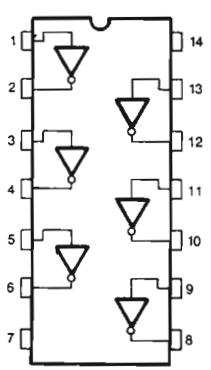
ABSOLUTE MAXIMUM RATINGS
(above which the usefull life may be impaired)

Supply Voltage V_{CC}, continuous	H118 D1	22V
	H118 D6	18V
Input Voltage	H118 D1	-0.5V to 20V
	H118 D6	-0.5V to 16V
Storage Temperature Range		-65°C to 150°C

OPERATING CONDITIONS

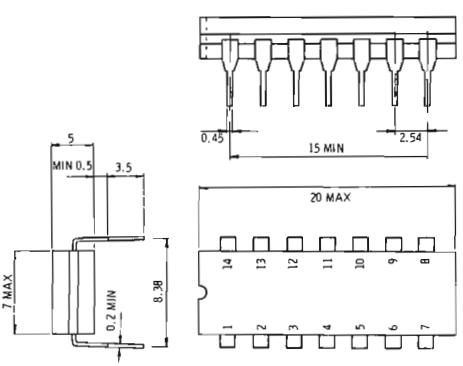
Temperature Range	H118 D1	0°C to 75°C
	H118 D6	40°C to 85°C
Supply Voltage	H118 D1	10.8V to 20V
	H118 D6	10.8V to 16V

CONNECTION DIAGRAM



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14 pin ceramic DIP



Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8 to 20 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	18.5 13.5 9.3	19 14 9.8		V V V	V_{CC} = 20 V I_{OH} = -200 μA V_{CC} = 15 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 20 V I_{OL} = 15 mA or V_{CC} = 15 V I_{OL} = 12 mA or V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.1 -0.08 -0.06	-0.6 -0.48 -0.36	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_F = 1.5 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 20 V V_R = 20 V
I_{SC}	Output Short Circuit Current	-9	-15	-25	mA	V_{CC} = 20 V Input and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6	7.5	mA	V_{CC} = 20 V Input High
I_{PDL}	Low Level Power Dissipation		1.5	2.5	mA	V_{CC} = 20 V Input Low
t_{pd1}	Turn-Off Delay		160		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	

ELECTRICAL CHARACTERISTIC (T_A = -40°C to 85°C, V_{CC} = 10.8 to 16 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5 9.3	15 9.8		V V	V_{CC} = 16 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16 V I_{OL} = 12.5 mA V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 16 V V_R = 16 V
I_{SC}	Output Short Circuit Current	-6.5	-13.5	-20	mA	V_{CC} = 16 V Input and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.4	6	mA	V_{CC} = 16 V Input High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.2	2	mA	V_{CC} = 16 V Input Low
t_{pd1}	Turn-Off Delay		160		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	

Strobed hex inverter active pull-up output

STANDARD TEMPERATURE RANGE
0°C to 75°C
INTERMEDIATE TEMPERATURE RANGE
-40°C to 85°C

- ACTIVE PULL-UP OUTPUT
- ENABLE AND STROBE INPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- 16-PIN CERAMIC DIP

The H 119 hex inverter can replace 1-1/2 quad two - input NAND gate packages in several applications through use of the enable or strobe inputs. The device consist of six two-input NAND gates with one input common to four gates and another common to two gates. Active Pull-up are utilize to minimize output impendance.
Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H119 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	H119 D1	22V
	H119 D6	18V
Input Voltage	H119 D1	-0.5V to 20V
	H119 D6	-0.5V to 16V
Storage Temperature Range		-65°C to 150°C

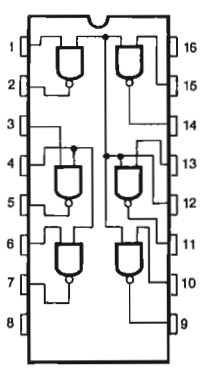
OPERATING CONDITIONS

Temperature Range	H119 D1	0°C to 75°C
	H119 D6	-40°C to 85°C
Supply Voltage	H119 D1	10.8V to 20V
	H119 D6	10.8V to 16V

ORDERING NUMBERS

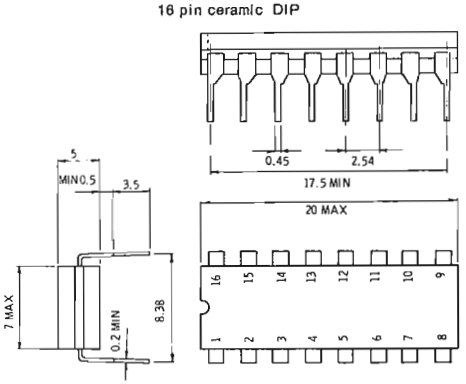
H119 D1 (Standard Temperature Range)
H119 D6 (Intermediate Temperature Range)

CONNECTION DIAGRAM



GND = PIN 8
V_{CC} = PIN 16

PHYSICAL DIMENSIONS
16 pin ceramic DIP



NOTE:
1) Board-drilling dimensions should equal your practice for a conventional 0.61 mm. diameter lead.
2) All dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8 V to 20 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	18.5 13.5 9.3	19 14 9.8		V V V	V_{CC} = 20 V I_{OH} = -200 μA V_{CC} = 15 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 20 V I_{OL} = 15 mA or V_{CC} = 15 V I_{OL} = 12 mA or V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
*I_F	Input Low Current		-0.1 -0.08 -0.06	-0.6 -0.48 -0.36	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_F = 1.5 V
*I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 20 V V_R = 20 V
I_{SC}	Output Short Circuit Current	-9	- 15	- 25	mA	V_{CC} = 20 V Inputs and Outputs Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6	7.5	mA	V_{CC} = 20 V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.5	2.5	mA	V_{CC} = 20 V Inputs Low
t_{pd1}	Turn-Off Delay		160		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	

ELECTRICAL CHARACTERISTICS (T_A = -40°C to 85°C, V_{CC} = 10.8 V to 16)V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5 9.3	15 9.8		V V	V_{CC} = 16 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16 V I_{OL} = 12.5 mA V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
*I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
**I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 16 V V_R = 16 V
I_{SC}	Output Short Circuit Current	-6.6	-13.5	-20	mA	V_{CC} = 16 V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.4	6	mA	V_{CC} = 16 V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.2	2	mA	V_{CC} = 16 V Inputs Low
t_{pd1}	Turn-Off Delay		160		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	

* Input Low Current : at pin 4 is equal to 2 · I_F; at pin 12 is equal to 4 · I_F
** Reverse Input Current : at pin 4 is equal to 2 · I_R; at pin 12 is equal to 4 · I_R

HLL INTEGRATED CIRCUIT

H156

Binary counter

EXTENDED TEMPERATURE RANGE
-55°C to 125°C

- SYNCHRONOUS COUNTING
- ASYNCHRONOUS PRESET
- ASYNCHRONOUS RESET
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY 5V at V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS and COS/MOS IC's (NOTE)
- 14-PIN CERAMIC PACKAGE

The H 156 is a synchronous binary counter. It is an asynchronously presentable, multifunctional building block usable in a large number of counting applications.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous			18V
Input Voltage	-0.5V	to	16V
Storage Temperature Range	-65°C	to	150°C

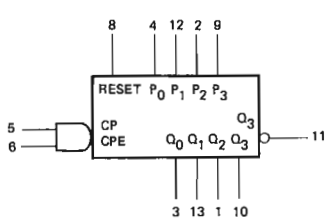
OPERATING CONDITIONS

Temperature Range	-55° C	to	125°C
Supply Voltage	10.8V	to	16V

ORDERING NUMBER

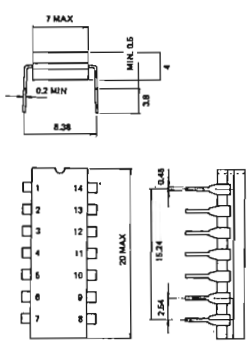
H 156 D2

CONNECTION DIAGRAM



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14-pin ceramic package



NOTE: all dimensions in mm.

NOTE: For details please refer to MOS IC's data sheets

Binary counter **H156**

EXTENDED TEMPERATURE RANGE

GENERAL DESCRIPTION

A clock buffer drives the four JK master slave flip-flops in parallel, so that synchronous operation is obtained. The information contained in the master is transferred to the slave flip-flops during the clock pulse high-to-low transition; the information contained in the slaves is available on their outputs Q_0, Q_1, Q_2 and Q_3.

Four asynchronous preset (P) inputs are provided, allowing the counter to be positioned to any counting number from 0 to 15. In order to preset the counter the following operations are necessary:

1) Disable the counter by applying a low level to CPE input;
2) Reset the counter by applying a low level to Reset input;
3) Insert in the counter the desired output configuration by applying to Preset inputs the levels shown in the Preset Count truth table (for example: if the desired preset is the count position 7, required preset inputs are $P_0=P_1=P_2=L$ $P_3=H$);
4) Apply a high level to Reset input;
5) Apply high levels to Preset inputs;
6) Enable the counter by applying a high level to CPE input; at this point of the example outputs are: $Q_0=Q_1=Q_2=H$, $Q_3=L$; that is a count of 7. The next CP high-to-low transition sets the counter on $Q_0=Q_1=Q_2=L$, $Q_3=H$; that is the count position 8.

Counter disabling by low level on CPE, operation N°1, is not strictly required: it is recommended in order to avoid spike generation on the first stage due to CP transition during reset operations.

From the above it can be seen that zero reset during count sequence, when P inputs are already high, can be accomplished by the simplified operation sequence:

1) CPE H to L
2) Reset H to L
4) Reset L to H
6) CPE L to H

TRUTH TABLES

COUNT SEQUENCE (see note)				
OUTPUTS				COUNT
Q0	Q1	Q2	Q3	
L	L	L	L	0
H	L	L	L	1
L	H	L	L	2
H	H	L	L	3
L	L	H	L	4
H	L	H	L	5
L	H	H	L	6
H	H	H	L	7
L	L	L	H	8
H	L	L	H	9
L	H	L	H	10
H	H	L	H	11
L	L	H	H	12
H	L	H	H	13
L	H	H	H	14
H	H	H	H	15
L	L	L	L	0

Note: CPE, R, P_0, P_1, P_2, and P_3 inputs are all High; transition from a count position to the following one is attained through a high – to – low CP input transition.

PRESET COUNT								
INPUTS				OUTPUTS				COUNT
P0	P1	P2	P3	Q0	Q1	Q2	Q3	
H	H	H	H	L	L	L	L	0
L	H	H	H	H	L	L	L	1
H	L	H	H	L	H	L	L	2
L	L	H	H	H	H	L	L	3
H	H	L	H	L	L	H	L	4
L	H	L	H	H	L	H	L	5
H	L	L	H	L	H	H	L	6
L	L	L	H	H	H	H	L	7
H	H	H	L	L	L	L	H	8
L	H	H	L	H	L	L	H	9
H	L	H	L	L	H	L	H	10
L	L	H	L	H	H	L	H	11
H	H	L	L	L	L	H	H	12
L	H	L	L	H	L	H	H	13
H	L	L	L	L	H	H	H	14
L	L	L	L	H	H	H	H	15
H	H	H	H	L	L	L	L	0

OUTPUTS: $L = V_{OL}$, $H = V_{OH}$

INPUTS: $L = V_{IL}$, $H = V_{IH}$

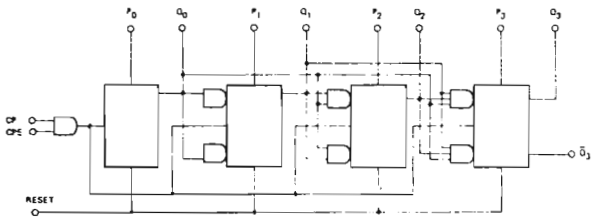
EXTENDED TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (V_{CC}=10.8V to 16V, T_A= -55°C to 125°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5	15		V	V_{CC} = 16V I_{OH} = - 200μA
		9.3	9.8		V	V_{CC} = 10.8V I_{OH} = - 200μA
						V_{IN} (async.) = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16V I_{OL} = 12.5mA or
						V_{CC} = 10.8V I_{OL} = 9mA
						$V_{IN}(P_0,P_1,P_2,P_3)=V_{IH}$; $V_{IN(R)}=V_{IL}$
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold for all inputs
I_F	Input Low Current					
	P_0, P_1, P_2, P_3 Inputs		-0.1	-0.7	mA	V_{CC} = 16V V_F = 1.5V
			-0.05	-0.48	mA	V_{CC} = 10.8V V_F = 1.5V
						Reset input grounded
	Reset Input		-0.4	-2.8	mA	V_{CC} = 16V V_F = 1.5V
			-0.2	-1.92	mA	V_{CC} = 10.8V V_F = 1.5V
						Preset inputs grounded
I_{FCP}	Input Low Current Clock		-0.07	-0.5	mA	V_{CC} = 16V V_F = 1.5V
	Inputs		-0.04	-0.36	mA	V_{CC} = 10.8V V_F = 1.5V
						V_{CC} on the clock input not under test
I_R	Reverse Input Current					
	P_0, P_1, P_2, P_3 Inputs		1	7	μA	V_{CC} = 16V V_R = 16V
						V_{CC} on reset and clock inputs
	Reset Input		5	28	μA	V_{CC} = 16V V_R = 16V
						V_{CC} on preset and clock inputs
I_{RCP}	Reverse Input Current Clock		1	7	μA	V_{CC} = 16V V_R = 16V
	Inputs					Ground on the clock input not under test
I_{SC}	Output Short Circuit Current	-6.5	-13.5	-20	mA	V_{CC} = 16V
						Output and proper asynchronous inputs grounded
I_{PD}	Power Dissipation Current			22	mA	V_{CC} = 16V
						Reset grounded

EXTENDED TEMPERATURE RANGE

LOGIC DIAGRAM



LOADING RULES (1 U.L. = 1 HLL gate input unit load)

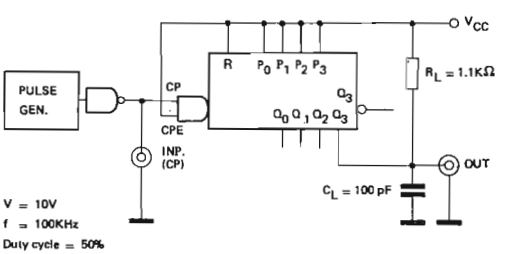
INPUTS:	CP, CPE	LOADING FACTOR	= 1 U.L.
	P_0, P_1, P_2, P_3		= 1.4 U.L.
	R		= 5.6 U.L.
OUTPUTS:	$Q_0, Q_1, Q_2, Q_3, \bar{Q}_3$	DRIVING FACTOR	= 25 U.L.

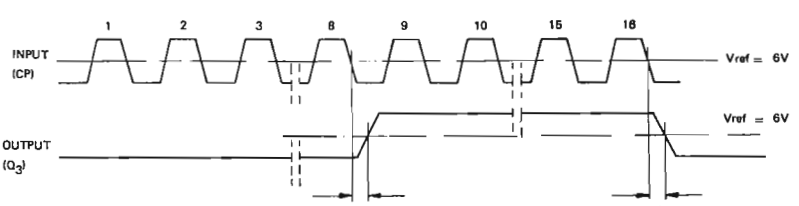
SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{pd1}	Turn-Off Delay		350	600	nsec	V_{CC} = 15V R_L = 1.1KΩ
t_{pd0}	Turn-On Delay		220	400	nsec	C_L = 100pF
f	Max. Input Clock Frequency	0.5	1		MHz	See test circuit

Notes: The rise and fall times of the clock pulse must be lower than 5 μsec/V.
The clock pulse width at high level must be higher than 300 ns.

tpd TEST CIRCUIT





Binary counter

The H 156 is a synchronous binary counter. It is an asynchronously presettable, multifunctional building block usable in a large number of counting applications.
Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H 156 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

STANDARD TEMPERATURE RANGE
0°C to 75°C
INTERMEDIATE TEMPERATURE RANGE
-40°C to 85°C

- SYNCHRONOUS COUNTING
- ASYNCHRONOUS PRESET
- ASYNCHRONOUS RESET
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC}=15V
- HIGH FAN-OUT 25 (WORST CASE)
- 14-PIN CERAMIC DIP

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	
H 156 D1	22V
H 156 D6	18V
Input Voltage	
H 156 D1	-0.5V to 20V
H 156 D6	-0.5V to 16V
Storage Temperature Range	-65°C to 150°C

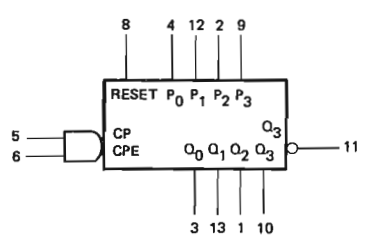
OPERATING CONDITIONS

Temperature Range	
H 156 D1	0°C to 75°C
H 156 D6	-40°C to 85°C
Supply Voltage	
H 156 D1	10.8V to 20V
H 156 D6	10.8V to 16V

ORDERING NUMBERS

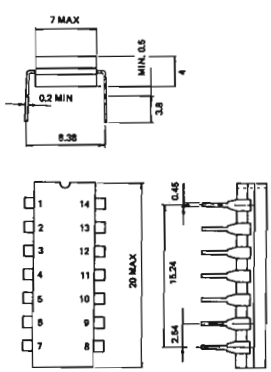
H 156 D1 (Standard Temperature Range)
H 156 D6 (Intermediate Temperature Range)

CONNECTION DIAGRAM



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14 pin ceramic DIP



Note: all dimensions in mm.

SEPTEMBER 1971

ELECTRICAL CHARACTERISTICS (V_{CC}=10.8V to 20V, T_A= 0°C to 75°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	18.5	19		V	V_{CC} = 20V I_{OH} = - 200 μA
		13.5	14		V	V_{CC} = 15V I_{OH} = - 200 μA
		9.3	9.8		V	V_{CC} = 10.8V I_{OH} = - 200 μA
						V_{IN} (async.) = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 20V I_{OL} = 15mA or
						V_{CC} = 15V I_{OL} = 12mA or
						V_{CC} = 10.8V I_{OL} = 9mA
						$V_{IN}(P_0,P_1,P_2,P_3) = V_{IH}$; $V_{IN(R)} = V_{IL}$
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold for all inputs
I_F	Input Low Current		-0.15	-0.8	mA	V_{CC} = 20V V_F = 1.5V
	P_0, P_1, P_2, P_3 Inputs		-0.1	-0.64	mA	V_{CC} = 15V V_F = 1.5V
			-0.05	-0.48	mA	V_{CC} = 10.8V V_F = 1.5V
						Reset input grounded
	Reset Input		-0.6	-3.2	mA	V_{CC} = 20V V_F = 1.5V
			-0.4	-2.56	mA	V_{CC} = 15V V_F = 1.5V
			-0.2	-1.92	mA	V_{CC} = 10.8V V_F = 1.5V
						Preset inputs grounded
I_{FCP}	Input Low Current Clock		-0.1	-0.6	mA	V_{CC} = 20V V_F = 1.5V
	Inputs		-0.07	-0.48	mA	V_{CC} = 15V V_F = 1.5V
			-0.04	-0.36	mA	V_{CC} = 10.8V V_F = 1.5V
						V_{CC} on the clock input not under test
I_R	Reverse Input Current					
	P_0, P_1, P_2, P_3, Inputs		1	5	μA	V_{CC} = 20V V_R = 20V
						V_{CC} on reset and clock inputs
	Reset Input		5	20	μA	V_{CC} = 20V V_R = 20V
						V_{CC} on preset and clock inputs
I_{RCP}	Reverse Input Current Clock Inputs		1	5	μA	V_{CC} = 20V V_R = 20V
						Ground on the clock input not under test
I_{SC}	Output Short Circuit Current	-9	-16	-25	mA	V_{CC} = 20V
						Output and proper asynchronous inputs grounded
I_{PD}	Power Dissipation Current		28	36	mA	V_{CC} = 20V
						Reset grounded

ELECTRICAL CHARACTERISTICS (V_{CC}=10.8V to 16V, T_A= -40°C to 85°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5	15		V	V_{CC} = 16V I_{OH} = - 200μA
		9.3	9.8		V	V_{CC} = 10.8V I_{OH} = - 200μA
						V_{IN} (async.) = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16V I_{OL} = 12.5mA or
						V_{CC} = 10.8V I_{OL} = 9mA
						$V_{IN}(P_0,P_1,P_2,P_3)=V_{IH}$; $V_{IN(R)}=V_{IL}$
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold for all inputs
I_F	Input Low Current					
	P_0, P_1, P_2, P_3 Inputs		-0.1	-0.7	mA	V_{CC} = 16V V_F = 1.5V
			-0.05	-0.48	mA	V_{CC} = 10.8V V_F = 1.5V
						Reset input grounded
	Reset Input		-0.4	-2.8	mA	V_{CC} = 16V V_F = 1.5V
			-0.2	-1.92	mA	V_{CC} = 10.8V V_F = 1.5V
						Preset inputs grounded
I_{FCP}	Input Low Current Clock		-0.07	-0.5	mA	V_{CC} = 16V V_F = 1.5V
	Inputs		-0.04	-0.36	mA	V_{CC} = 10.8V V_F = 1.5V
						V_{CC} on the clock input not under test
I_R	Reverse Input Current					
	P_0, P_1, P_2, P_3 Inputs		1	5	μA	V_{CC} = 16V V_R = 16V
						V_{CC} on reset and clock inputs
	Reset Input		5	20	μA	V_{CC} = 16V V_R = 16V
						V_{CC} on preset and clock inputs
I_{RCP}	Reverse Input Current Clock		1	5	μA	V_{CC} = 16V V_R = 16V
	Inputs					Ground on the clock input not under test
I_{SC}	Output Short Circuit Current	-6.5	-13.5	-20	mA	V_{CC} = 16V
						Output and proper asynchronous inputs grounded
I_{PD}	Power Dissipation Current		20	29	mA	V_{CC} = 16V
						Reset grounded

GENERAL DESCRIPTION

A clock buffer drives the four JK master slave flip-flops in parallel, so that synchronous operation is obtained. The information contained in the master is transferred to the slave flip-flops during the clock pulse high-to-low transition; the information contained in the slaves is available on their outputs Q_0, Q_1, Q_2 and Q_3.

Four asynchronous preset (P) inputs are provided, allowing the counter to be positioned to any counting number from 0 to 15. In order to preset the counter the following operations are necessary:

1) Disable the counter by applying a low level to CPE input;
2) Reset the counter by applying a low level to Reset input;
3) Insert in the counter the desired output configuration by applying to Preset inputs the levels shown in the Preset Count truth table (for example: if the desired preset is the count position 7, required preset inputs are $P_0=P_1=P_2=L$ $P_3=H$);
4) Apply a high level to Reset input;
5) Apply high levels to Preset inputs;
6) Enable the counter by applying a high level to CPE input; at this point of the example outputs are: $Q_0=Q_1=Q_2=H$, $Q_3=L$; that is a count of 7. The next CP high-to-low transition sets the counter on $Q_0=Q_1=Q_2=L$, $Q_3=H$; that is the count position 8.

Counter disabling by low level on CPE, operation N°1, is not strictly required: it is recommended in order to avoid spike generation on the first stage due to CP transition during reset operations.

From the above it can be seen that zero reset during count sequence, when P inputs are already high, can be accomplished by the simplified operation sequence:

1) CPE H to L
2) Reset H to L
4) Reset L to H
6) CPE L to H

TRUTH TABLES

COUNT SEQUENCE (see note)				
OUTPUTS				COUNT
Q0	Q1	Q2	Q3	
L	L	L	L	0
H	L	L	L	1
L	H	L	L	2
H	H	L	L	3
L	L	H	L	4
H	L	H	L	5
L	H	H	L	6
H	H	H	L	7
L	L	L	H	8
H	L	L	H	9
L	H	L	H	10
H	H	L	H	11
L	L	H	H	12
H	L	H	H	13
L	H	H	H	14
H	H	H	H	15
L	L	L	L	0

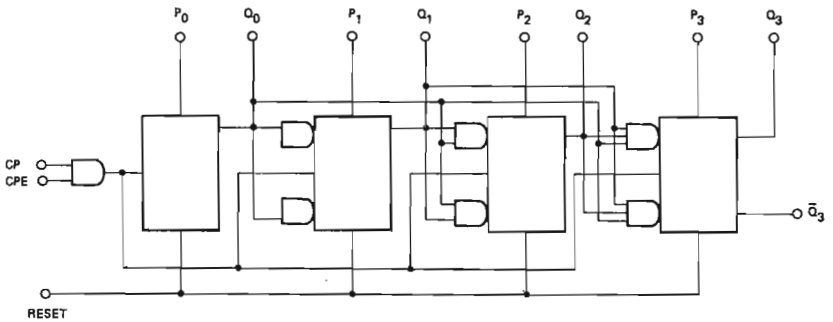
PRESET COUNT								
INPUTS				OUTPUTS				COUNT
P0	P1	P2	P3	Q0	Q1	Q2	Q3	
H	H	H	H	L	L	L	L	0
L	H	H	H	H	L	L	L	1
H	L	H	H	L	H	L	L	2
L	L	H	H	H	H	L	L	3
H	H	L	H	L	L	H	L	4
L	H	L	H	H	L	H	L	5
H	L	L	H	L	H	H	L	6
L	L	L	H	H	H	H	L	7
H	H	H	L	L	L	L	H	8
L	H	H	L	H	L	L	H	9
H	L	H	L	L	H	L	H	10
L	L	H	L	H	H	L	H	11
H	H	L	L	L	L	H	H	12
L	H	L	L	H	L	H	H	13
H	L	L	L	L	H	H	H	14
L	L	L	L	H	H	H	H	15
H	H	H	H	L	L	L	L	0

Note: CPE, R, P_0, P_1, P_2, and P_3 inputs are all High; transition from a count position to the following one is attained through a high – to – low CP input transition.

OUTPUTS: $L = V_{OL}$, $H = V_{OH}$

INPUTS: $L = V_{IL}$, $H = V_{IH}$

LOGIC DIAGRAM



LOADING RULES (1 U.L. = 1 HLL gate input unit load)

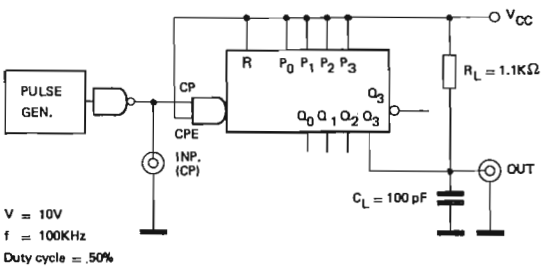
INPUTS:	CP, CPE	LOADING FACTOR	= 1 U.L.
	P_0, P_1, P_2, P_3		= 1.4 U.L.
	R		= 5.4 U.L.
OUTPUTS:	$Q_0, Q_1, Q_2, Q_3, \bar{Q}_3$	DRIVING FACTOR	= 25 U.L.

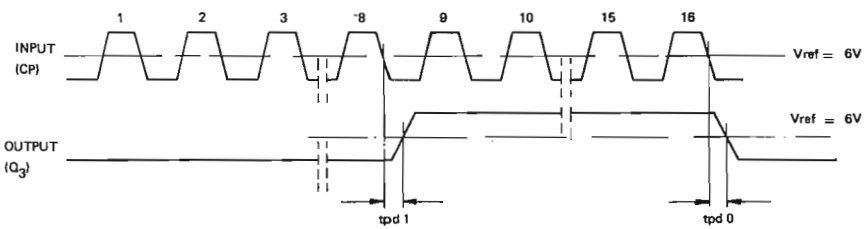
SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{pd1}	Turn-Off Delay		350	600	nsec	V_{CC} = 15V R_L = 1.1KΩ
t_{pd0}	Turn-On Delay		220	400	nsec	C_L = 100pF
f	Max. Input Clock Frequency	0.5	1		MHz	See test circuit

Notes: The rise and fall times of the clock pulse must be lower than 5 μsec/V.
The clock pulse width at high level must be higher than 300 ns.

tpd TEST CIRCUIT





H157

Decade counter

EXTENDED TEMPERATURE RANGE
-55°C to 125°C

- SYNCHRONOUS COUNTING
- ASYNCHRONOUS PRESET
- ASYNCHRONOUS RESET
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY 5V at V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS and COS/MOS IC's (NOTE)
- 14-PIN CERAMIC PACKAGE

The H157 is a synchronous 8421 BCD Counter. It is an asynchronously presettable, multifunctional building block usable in a large number of counting applications.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous			16V
Input Voltage	-0.5V	to	16V
Storage Temperature Range	-55°C	to	150°C

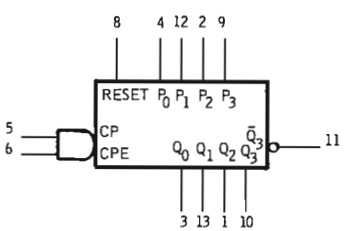
OPERATING CONDITIONS

Temperature Range	-55°C	to	125°C
Supply Voltage	10.8 V	to	16V

ORDERING NUMBER

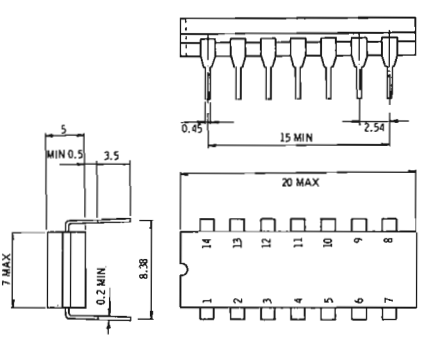
H157 D2

LOGIC DIAGRAM AND PIN CONNECTION



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14-pin ceramic package



NOTE: all dimensions in mm.

NOTE: For details please refer to MOS IC's data sheets

Decade counter H 157

EXTENDED TEMPERATURE RANGE

FUNCTIONAL DESCRIPTION

A clock buffer drives the four JK master slave flip-flops in parallel,so that synchronous operation is obtained.
The information contained in the master is transferred to the slave flip-flops during the clock pulse high-to-low transition; the information contained in the slaves is available on their outputs Q_0, Q_1, Q_2, and Q_3.
Four asynchronous preset (P) inputs are provided, allowing the counter to be positioned to any counting number from 0 to 9.
In order to preset the counter the following operations are necessary :

1. Disable the counter by applying a low level to CPE input,
2. Reset the counter by applying a low level to Reset input,
3. Insert in the counter the desired output configuration by applying to Preset inputs the levels shown in the Preset Count truth table (for example : if the desired preset is the count position 7, required preset inputs are $P_0 = P_1 = P_2 = L$, $P_3 = H$),
4. Apply a high level to Reset input,
5. Apply high levels to Preset inputs,
6. Enable the counter by applying a high level to CPE input; at this point of the example outputs are :
   $Q_0 = Q_1 = Q_2 = H$, $Q_3 = L$, that is a count of 7. The next CP high-to-low transition sets the counter on $Q_0 = Q_1 = Q_2 = L$, $Q_3 = H$,that is the count position 8.

Counter disabling by low level on CPE, operation N°. 1, is not strictly required : it is recommended in order to avoid spike generation on the first stage due to CP transition during reset operations.
From the above it can be seen that zero reset during BCD count sequence, when P inputs are already high, can be accomplished by the simplified operation sequence:

1. CPE H to L,
2. Reset H to L,
4. Reset L to H,
6. CPE L to H.

TRUTH TABLES

BCD COUNT SEQUENCE (see note)

OUTPUTS				COUNT
Q_0	Q_1	Q_2	Q_3	
L	L	L	L	0
H	L	L	L	1
L	H	L	L	2
H	H	L	L	3
L	L	H	L	4
H	L	H	L	5
L	H	H	L	6
H	H	H	L	7
L	L	L	H	8
H	L	L	H	9
L	L	L	L	0

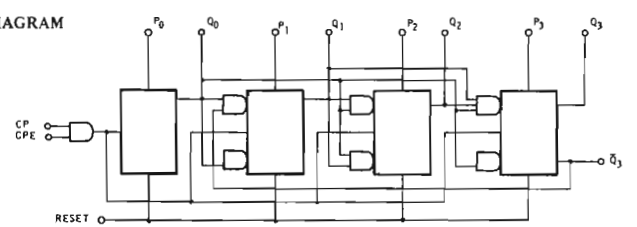
Note: CPE, R, P_0, P_1, P_2 and P_3 inputs are all H; transition from a count position to the following one is attained through a high-to-low CP input transition.

PRESET COUNT

INPUTS				OUTPUTS				COUNT
P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	
H	H	H	H	L	L	L	L	0
L	H	H	H	H	L	L	L	1
H	L	H	H	L	H	L	L	2
L	L	H	H	H	H	L	L	3
H	H	L	H	L	L	H	L	4
L	H	L	H	H	L	H	L	5
H	L	L	H	L	H	H	L	6
L	L	L	H	H	H	H	L	7
H	H	H	L	L	L	L	H	8
L	H	H	L	H	L	L	H	9

OUTPUTS : L = V_{OL}, H = V_{OH}
INPUTS : L = V_{IL}, H = V_{IH}

LOGIC DIAGRAM



EXTENDED TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (V_{CC}=10.8V to 16V, T_A= -55°C to 125°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5	15		V	V_{CC} = 16V I_{OH} = - 200μA
		9.3	9.8		V	V_{CC} = 10.8V I_{OH} = - 200μA
						V_{IN} (async.) V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16V I_{OL} = 12.5mA or
						V_{CC} = 10.8V I_{OL} = 9mA
						$V_{IN}(P_0,P_1,P_2,P_3)=V_{IH}$; $V_{IN(R)}=V_{IL}$
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold for all inputs
I_F	Input Low Current					
	P_0, P_1, P_2, P_3 Inputs		-0.1	-0.7	mA	V_{CC} = 16V V_F = 1.5V
			-0.05	-0.48	mA	V_{CC} = 10.8V V_F = 1.5V
						Reset input grounded
	Reset Input		-0.4	-2.8	mA	V_{CC} 16V V_F = 1.5V
			-0.2	-1.92	mA	V_{CC} = 10.8V V_F = 1.5V
						Preset inputs grounded
I_{FCP}	Input Low Current Clock		-0.07	-0.5	mA	V_{CC} = 16V V_F = 1.5V
	Inputs		-0.04	-0.36	mA	V_{CC} = 10.8V V_F = 1.5V
						V_{CC} on the clock input not under test
I_R	Reverse Input Current					
	P_0, P_1, P_2, P_3 Inputs		1	7	μA	V_{CC} = 16V V_R = 16V
						V_{CC} on reset and clock inputs
	Reset Input		5	20	μA	V_{CC} = 16V V_R = 16V
						V_{CC} on preset and clock inputs
I_{RCP}	Reverse Input Current Clock		1	7	μA	V_{CC} = 16V V_R = 16V
	Inputs					Ground on the clock input not under test
I_{SC}	Output Short Circuit Current	-6.5	-13.5	-20	mA	V_{CC} = 16V
						Output and proper asynchronous inputs grounded
I_{PD}	Power Dissipation Current		5	22	mA	V_{CC} 16V
						Reset grounded

Decade counter **H 157**

EXTENDED TEMPERATURE RANGE

LOADING RULES (1 U.L. = 1 HLL gate input unit load)

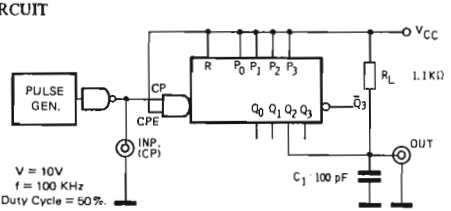
INPUTS :	CP, CPE	LOADING FACTOR	= 1 U.L.
	P0, P1, P2, P3		= 1.4 U.L.
	R		= 5.4 U.L.
OUTPUTS :	Q0, Q1, Q2, Q3, $\bar{Q}3$	DRIVING FACTOR	= 25 U.L.

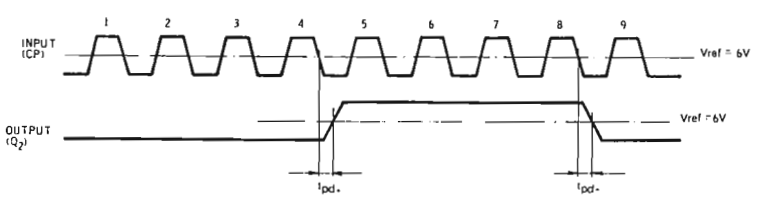
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	UNIT	CONDITIONS
t_{pd} +	Turn-off Delay		350	600	nsec	V_{CC} = 15 V
t_{pd} -	Turn-on Delay		220	400	nsec	C_L = 100 pF
						R_L = 1.1 KΩ
f	Max. Input Clock Frequency	0.5	1		MHz	See test circuit

NOTES : The rise and fall times of the clock pulse must be lower than 5 µsec/V.
The clock pulse width at high level must be higher than 300 nS.

t_{pd} TEST CIRCUIT





decade counter

STANDARD TEMPERATURE RANGE, 0°C TO 75°C

- SYNCHRONOUS COUNTING
- ASYNCHRONOUS PRESET
- ASYNCHRONOUS RESET
- WIDE RANGE OF SUPPLY VOLTAGE 10.8 TO 20 V
- HIGH DC NOISE IMMUNITY, 5 V AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- 14 PIN CERAMIC DIP

The H 157 is a synchronous 8421 BCD Counter. It is an asynchronously presettable, multifunctional building block usable in a large number of counting applications. Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H 157 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage (V_{CC}) continuous	22 V
Input Voltage	- 0.5 V to 20V
Storage Temperature Range	-55°C to 150°C

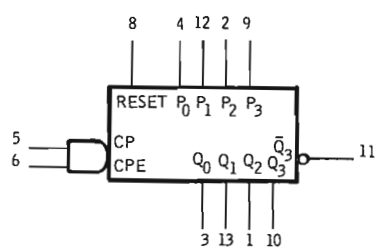
OPERATING CONDITIONS

Temperature Range	0°C to 75°C
Supply Voltage	10.8 V to 20 V

ORDERING NUMBER

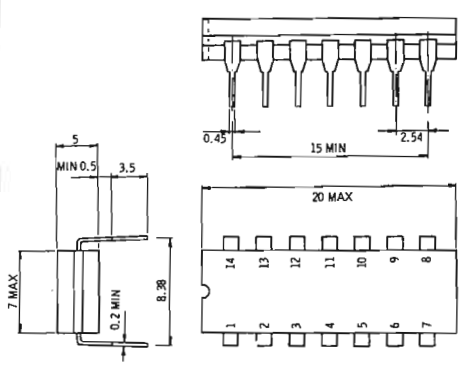
H157 D1

LOGIC DIAGRAM AND PIN CONNECTION



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14-pin ceramic DIP



Note : all dimensions in mm.

NOVEMBER 1970

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8V to 20 V)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS
V_{OH}	Output High Voltage	18.5		18.5		18.5		V	V_{CC}= 20V I_{OH} =-200 µA
		13.5		13.5		13.5		V	V_{CC}= 15V I_{OH} =-200 µA
		9.3		9.3		9.3		V	V_{CC}= 10.8V I_{OH} =-200 µA
									$V_{IN(async.)}$= V_{IL} (see below)
V_{OL}	Output Low Voltage		1.5		1.5		1.5	V	V_{CC}= 20V I_{OL} = 15 mA or
									V_{CC}= 15V I_{OL} = 12 mA or
									V_{CC}= 10.8V I_{OL} = 9 mA
									$V_{IN(async.)}$ = V_{IH} (see below)
V_{IL}	Input Low Voltage		6		6		6	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	8		8		8		V	Guaranteed input high threshold for all inputs
I_F	Input Low Current		-0.8		-0.8		-0.8	mA	V_{CC}= 20V V_F = 1.5 V
	P_0, P_1, P_2, P_3 Inputs		-0.64		-0.64		-0.64	mA	V_{CC}= 15V V_F = 1.5 V
			-0.48		-0.48		-0.48	mA	V_{CC}= 10.8V V_F = 1.5 V
									Reset grounded
	Reset Input		-3.2		-3.2		-3.2	mA	V_{CC}= 20V V_F = 1.5V
			-2.56		-2.56		-2.56	mA	V_{CC}= 15V V_F = 1.5V
			-1.92		-1.92		-1.92	mA	V_{CC}= 10.8V V_F = 1.5 V
									Preset inputs grounded
I_{FCP}	Input Low Current		-0.6		-0.6		-0.6	mA	V_{CC}= 20V V_F = 1.5V
	Clock Inputs		-0.48		-0.48		-0.48	mA	V_{CC}= 15V V_F = 1.5V
			-0.36		-0.36		-0.36	mA	V_{CC}= 10.8V V_F = 1.5V
									V_{CC} on the clock input not under test
I_R	Reverse Input Current								
	P_0, P_1, P_2, P_3 Inputs		5		5		5	µA	V_{CC}= 20V V_R = 20V
									V_{CC} on reset and clock inputs
	Reset Input		20		20		20	µA	V_{CC}= 20V V_R = 20V
									V_{CC} on preset and clock inputs
I_{RCP}	Reverse Input Current		5		5		5	µA	V_{CC}= 20V V_R = 20V
	Clock Inputs								Ground on the clock input not under test
I_{SC}	Output Short Circuit Current	-9	-25	-9	-25	-9	-25	mA	V_{CC}= 20V
									Output and proper asynchronous inputs grounded
I_{PD}	Power Dissipation Current		36		36		36	mA	V_{CC}= 20V
									Reset grounded

FUNCTIONAL DESCRIPTION

A clock buffer drives the four JK master slave flip-flops in parallel,so that synchronous operation is obtained.
The information contained in the master is transferred to the slave flip-flops during the clock pulse high-to-low transition; the information contained in the slaves is available on their outputs Q_0, Q_1, Q_2, and Q_3.
Four asynchronous preset (P) inputs are provided, allowing the counter to be positioned to any counting number from 0 to 9.
In order to preset the counter the following operations are necessary :

1. Disable the counter by applying a low level to CPE input,
2. Reset the counter by applying a low level to Reset input,
3. Insert in the counter the desired output configuration by applying to Preset inputs the levels shown in the Preset Count truth table (for example : if the desired preset is the count position 7, required preset inputs are $P_0 = P_1 = P_2 = L$, $P_3 = H$),
4. Apply a high level to Reset input,
5. Apply high levels to Preset inputs,
6. Enable the counter by applying a high level to CPE input; at this point of the example outputs are : $Q_0 = Q_1 = Q_2 = H$, $Q_3 = L$, that is a count of 7. The next CP high-to-low transition sets the counter on $Q_0 = Q_1 = Q_2 = L$, $Q_3 = H$,that is the count position 8.

Counter disabling by low level on CPE. operation N°. 1, is not strictly required : it is recommended in order to avoid spike generation on the first stage due to CP transition during reset operations.
From the above it can be seen that zero reset during BCD count sequence, when P inputs are already high, can be accomplished by the simplified operation sequence:

1. CPE H to L,
2. Reset H to L,
4. Reset L to H,
6. CPE L to H.

TRUTH TABLES

BCD COUNT SEQUENCE (see note)

OUTPUTS				COUNT
Q_0	Q_1	Q_2	Q_3	
L	L	L	L	0
H	L	L	L	1
L	H	L	L	2
H	H	L	L	3
L	L	H	L	4
H	L	H	L	5
L	H	H	L	6
H	H	H	L	7
L	L	L	H	8
H	L	L	H	9
L	L	L	L	0

Note: CPE, R, P_0, P_1, P_2 and P_3 inputs are all H; transition from a count position to the following one is attained through a high-to-low CP input transition.

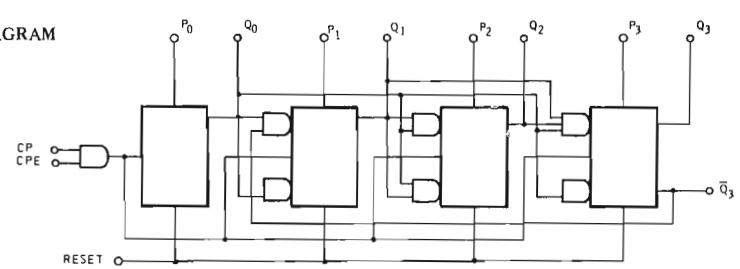
PRESET COUNT

INPUTS				OUTPUTS				COUNT
P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	
H	H	H	H	L	L	L	L	0
L	H	H	H	H	L	L	L	1
H	L	H	H	L	H	L	L	2
L	L	H	H	H	H	L	L	3
H	H	L	H	L	L	H	L	4
L	H	L	H	H	L	H	L	5
H	L	L	H	L	H	H	L	6
L	L	L	H	H	H	H	L	7
H	H	H	L	L	L	L	H	8
L	H	H	L	H	L	L	H	9

OUTPUTS : L = V_{OL}, H = V_{OH}

INPUTS : L = V_{IL}, H = V_{IH}

LOGIC DIAGRAM



LOADING RULES (1 U.L. = 1 HLL gate input unit load)

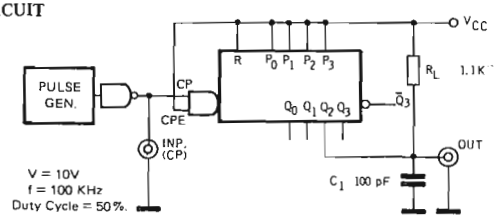
INPUTS :	CP, CPE	LOADING FACTOR	= 1 U.L.
	P0, P1, P2, P3		= 1.4 U.L.
	R		= 5.4 U.L.
OUTPUTS :	Q0, Q1, Q2, Q3, $\bar{Q}3$	DRIVING FACTOR	= 25 U.L.

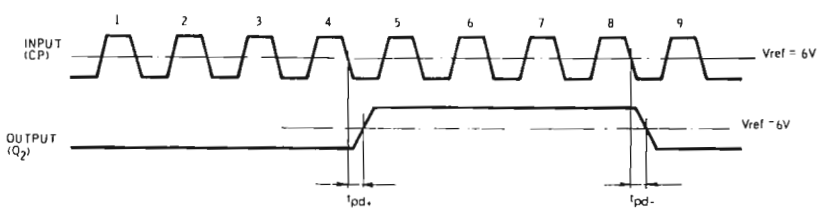
SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	UNIT	CONDITIONS
t_{pd+}	Turn-off Delay		350	600	nsec	$V_{CC} = 15$ V
t_{pd-}	Turn-on Delay		220	400	nsec	$C_L = 100$ pF
						$R_L = 1.1$ KΩ
f	Max. Input Clock Frequency	0.5	1		MHz	See test circuit

NOTES : The rise and fall times of the clock pulse must be lower than 5 µsec/V.
The clock pulse width at high level must be higher than 300 nS.

t_{pd} TEST CIRCUIT





STANDARD TEMPERATURE RANGE
0°C to 75°C

- STABLE HIGH-VOLTAGE OUTPUT CHARACTERISTICS AT 55V
- DIRECT DISPLAY DRIVE CAPABILITY
- WIDE RANGE OF SUPPLY VOLTAGE 10.8 V to 20V
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- 16-PIN CERAMIC DIP

BCD to Decimal Decoder/Driver

The H 158 is an HLL compatible BCD to Decimal Decoder/Driver. It accepts 8421 binary coded decimal inputs and provides ten mutually exclusive outputs which are able to directly drive gas-filled, cold-cathode indicator tubes. In accordance with the High Level Logic family characteristics, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerances and unusually low fan-in. These features make the H 158 particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

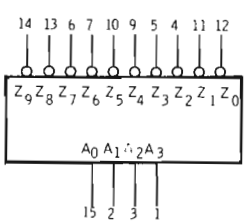
Supply Voltage (V_{CC}) Continuous	22 V
Input Voltage	-0.5 V to 20 V
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

Temperature Range	0°C to 75°C
Supply Voltage	10.8 V to 20 V

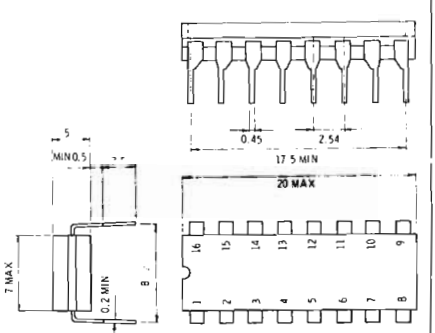
ORDERING NUMBER
H 158 DI

LOGIC DIAGRAM
AND PIN CONNECTION



GND = PIN 8
V_{CC} = PIN 16

PHYSICAL DIMENSIONS
16-pin ceramic DIP



Note : all dimensions in mm.

JANUARY 1971

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8V to 20V)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS
V_{OH}	Output High Voltage	55		55		55		V	V_{CC}=10.8 to 20V I_{OH}=100 µA V_{IN} at input thresholds
I_{CEX}	Output Leakage Current		20		20		20	µA	V_{CC}=10.8 to 20V V_{OUT}=20V V_{IN} at ground or V_{CC}
V_{OL}	Output Low Voltage		2		2		2	V	V_{CC}=10.8 to 20V I_{OL}=7mA V_{IN} at input thresholds
V_{IL}	Input Low Voltage		6		6		6	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	8		8		8		V	Guaranteed input high threshold for all inputs
I_F	Input Low Current		-0.6		-0.6		-0.6	mA	V_{CC}=20V
			-0.48		-0.48		-0.48	mA	V_{CC}=15V V_F=1.5V
			-0.36		-0.36		-0.36	mA	V_{CC}=10.8V
I_R	Input Reverse Current		5		5		5	µA	V_{CC} and V_R = 10.8 to 20 V
I_{PD}	Power Dissipation Current		30		30		30	mA	V_{CC}=20V Inputs Grounded

LOADING RULES (1 U.L. = 1 HLL GATE INPUT UNIT LOAD)

INPUTS : A_0 A_1 A_2 A_3 LOADING FACTOR = 1 U.L.

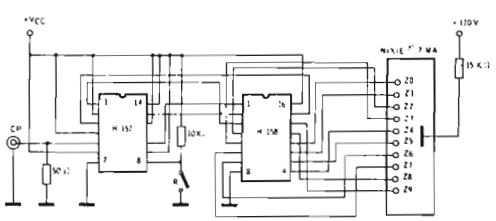
FUNCTIONAL DESCRIPTION

The BCD to Decimal Decoder/Driver accepts BCD inputs from HLL or MOS circuits and produces the correct output selection to directly drive gas-filled, cold-cathode indicator tubes.
The outputs are selected as shown in the Truth Table. The H 158 is capable of driving all known available cold cathode indicator tubes having 7mA or less cathode current.

A_0	A_1	A_2	A_3	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7	Z_8	Z_9
L	L	L	L	L									
H	L	L	L		L								
L	H	L	L			L							
H	H	L	L				L						
L	L	H	L					L					
H	L	H	L						L				
L	H	H	L							L			
H	H	H	L								L		
L	L	L	H									L	
H	L	L	H										L

Note : Positions not shown are High.

COUNTING TEST CIRCUIT



HLL INTEGRATED CIRCUIT

H 159

PRELIMINARY DATA

QUAD LATCH

The **H 159** (standard temperature range) is a monolithic integrated circuit, available in 16-lead dual in-line ceramic package, useful in monitoring or storage applications.
A common clock input (ϕ), when in the high state, allows information present at the data input (D) to be transferred to the output of the latch. When ϕ is low, the information present at Q or $\overline{Q}$, will remain at the previous level.
A common Reset (R) input allows resetting of all Q outputs to a logic "0" state, independent of ϕ or D.

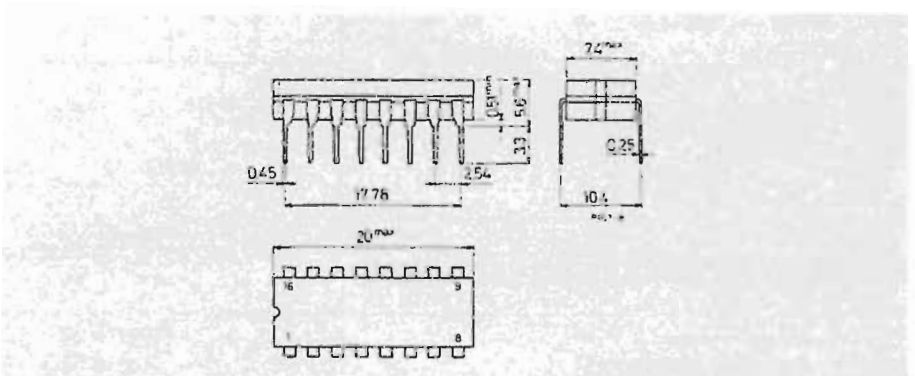
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	22	V
V_i	Input voltage	-0.5 to 20	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 75	°C

ORDERING NUMBER: H 159 D1

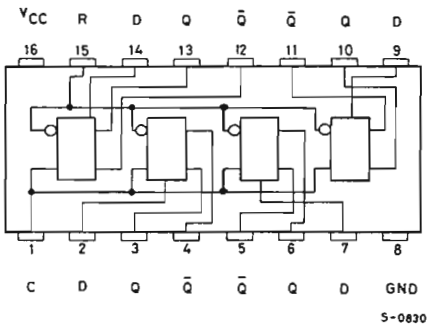
MECHANICAL DATA

Dimensions in mm

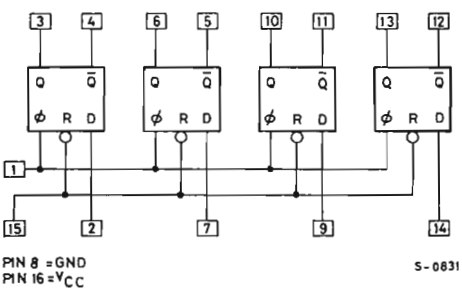


H 159

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



TRUTH TABLE

ϕ	D	R	Qn+1
0	X	1	Qn
X	X	0	0
1	0	1	0
1	1	1	1

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	10.8 to 20	V
T_{op}	Operating temperature	0 to 75	°C

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	I_{OH} = -200 μA V_i = see truth table V_{CC} = 10.8V V_{CC} = 15V V_{CC} = 20V	 9.3 13.5 18.5	 9.8 14 19	 	 V V V
V_{OL}	Output low voltage	I_{OL} = 12 mA V_I = see truth table V_{CC} = 10.8V to 20V	 	 1	 1.5	 V
V_{IH}	Input high voltage	V_{CC} = 10.8V to 20V	8			V
V_{IL}	Input low voltage	V_{CC} = 10.8V to 20V			6	V
I_{IL}	Input low current	V_{IL} = 1.5V V_{CC} = 10.8V to 20V			-0.36	mA
I_{IR}	Input reverse current	V_{CC} = 20V V_{IR} = 20V			5	μA
I_{SC}	Short-circuit output current	V_{CC} = 20V Input and outputs grounded	-9	-15	-25	mA
I_{PD}	Power dissipation current	V_{CC} = 20V			34	mA

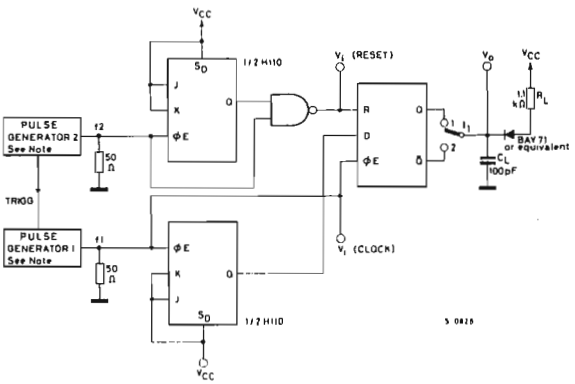
DYNAMIC ELECTRICAL CHARACTERISTICS: (T_{amb} = 25°C, V_{CC} = 15V, C_L = 100 pF, R_L 1.1 kΩ)

Parameter		Test conditions*	Min.	Typ.	Max.	Unit
t_{pd1}	Propagation delay time to logical 1 level from ϕ to Q	$I_1 = 1$			770	ns
t_{pd0}	Propagation delay time to logical 0 level from ϕ to Q	$I_1 = 1$			440	ns
t_{pd1}	Propagation delay time to logical 1 level from ϕ to $\overline{Q}$	$I_1 = 2$			300	ns
t_{pd0}	Propagation delay time to logical 0 level from ϕ to $\overline{Q}$	$I_1 = 2$			540	ns
t_{pd0}	Propagation delay time to logical 0 level from R to Q	$I_1 = 1$			100	ns
t_{pd1}	Propagation delay time to logical 1 level from R to $\overline{Q}$	$I_1 = 2$			100	ns

*See switching times test circuit and waveforms

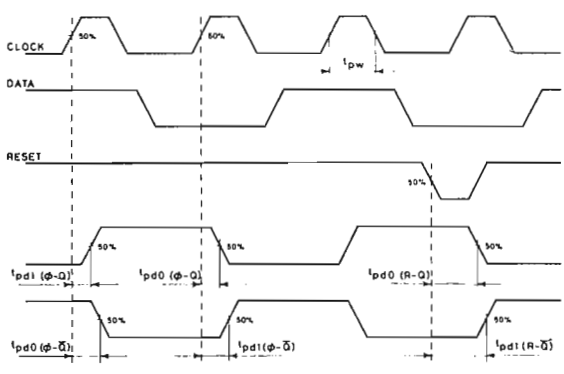
SWITCHING TIMES

Test circuit



NOTE: The pulse generators have the following characteristics: $t_r = t_f \geqslant 10$ ns @ 10V, $t_{pw} = 5\ \mu s$, PRR = 50 kHz (Pulse Generator 1), PRR = 25 kHz (Pulse Generator 2)

Waveforms



HLL INTEGRATED CIRCUIT

H 160

PRELIMINARY DATA

4-BIT SHIFT REGISTER

- JK MASTER SLAVE FLIP-FLOPS
- ASYNCHRONOUS MASTER RESET
- INDIVIDUAL SET INPUT

The **H 160** (standard temperature range) is a monolithic integrated circuit, available in 16-lead dual in-line ceramic package,consisting of four JK Master Slave flip-flops, connected in serial fashion.
The outputs of the flip-flops change state on the negative transition of the clock pulse. A set input (S) is provided for eack flip-flops hat acts when a low level is applied regardless of the state of the clock similarly an asynchronous master reset (MR) input clears all the flip-flop when a low level is applied.
The clock enable (ϕ E) control provides a means of inhibiting the clock input.
Q outputs are available from all four stages, and $\overline{Q}$ from the last register stage.

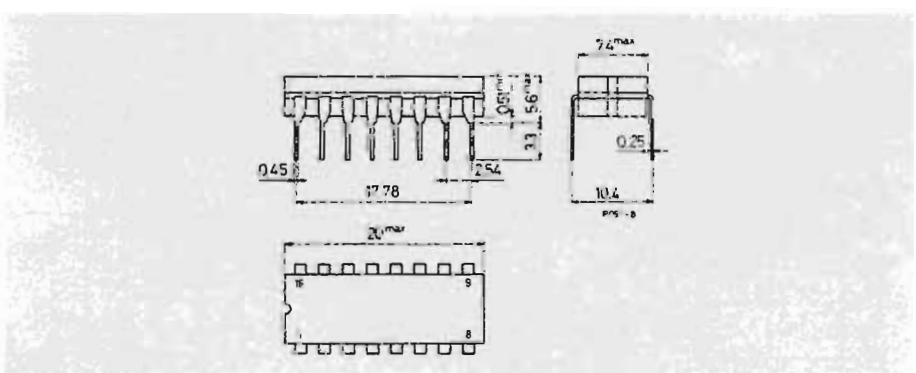
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	22	V
V_i	Input voltage	-0.5 to 20	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 75	°C

ORDERING NUMBER: H 160 D1

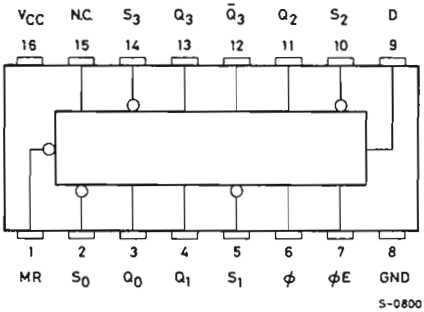
MECHANICAL DATA

Dimensions in mm

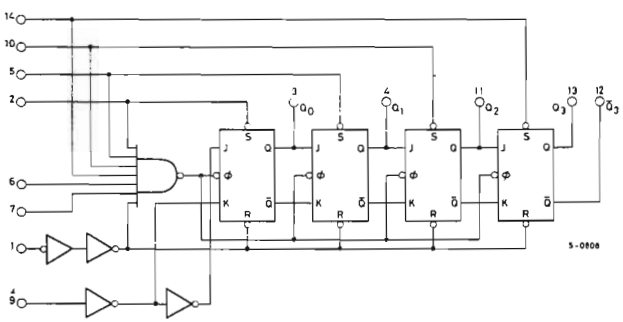


H 160

CONNECTION DIAGRAMS



BLOCK DIAGRAM



TRUTH TABLES

MR	S_1	Q_1
X	0	1
0	1	0
1	1	X

COUNT	D	Q_0	Q_1	Q_2	Q_3
0	1	0	0	0	0
1	1	1	0	0	0
2	1	1	1	0	0
3	1	1	1	1	0
4	1	1	1	1	1
0	0	1	1	1	1
1	0	0	1	1	1
2	0	0	0	1	1
3	0	0	0	0	1
4	0	0	0	0	0

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	10.8 to 20 V
T_{op}	Operating temperature	0 to 75 °C

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	I_{OH} = -200 µA V_i = see truth tables V_{CC} = 10.8V V_{CC} = 15V V_{CC} = 20V	 9.3 13.5 18.5	 9.8 14 19	 	 V V V
V_{OL}	Output low voltage	I_{OL} = 12 mA V_i = see truth tables V_{CC} = 10.8V to 20V	 	 1	 1.5	 V
V_{IH}	Input high voltage	V_{CC} = 10.8V to 20V	8			V
V_{IL}	Input low voltage	V_{CC} = 10.8V to 20V			6	V
I_{IL}	Input low current (ϕ, ϕE, D, $\overline{MR}$)	V_{CC} = 20V V_{IL} = 1.5V			0.4	mA
I_{IL}	Input low current (S)	V_{CC} = 20V V_{IL} = 1.5V			0.8	mA
I_{IR}	Input reverse current (ϕ, ϕE, D, $\overline{MR}$)	V_{CC} = 20V V_{IR} = 20V			5	µA
I_{IR}	Input reverse current (S)	V_{CC} = 20V V_{IR} = 20V			10	µA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{SC}	Short-circuit output current	$V_{CC} = 20V$ $V_i(S_i) = GND$	-9		-25	mA
I_{PD}	Power dissipation current	$V_{CC} = 20V$ Inputs GND			38	mA

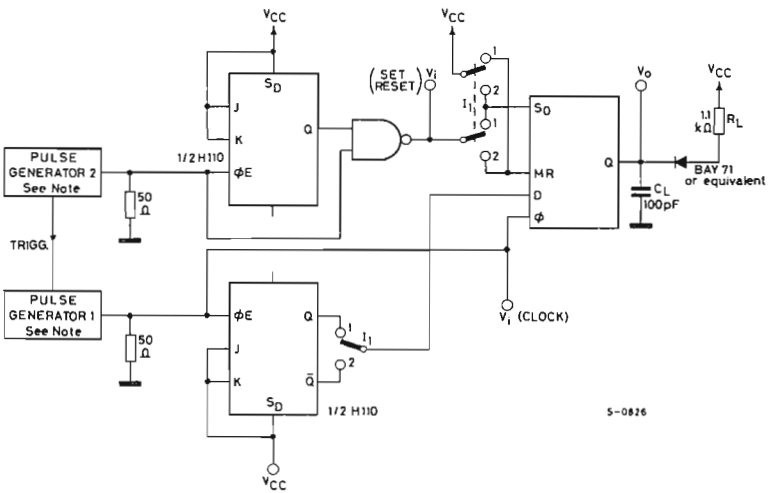
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25°C$, $V_{CC} = 15V$, $C_L = 100\,pF$, $R_L = 1.1\,k\Omega$)

Parameter		Test conditions*	Min.	Typ.	Max.	Unit
t_{pd1}	Propagation delay time to logical 1 level from ϕ to Q	$I_1 = 1$		350	700	ns
t_{pd0}	Propagation delay time to logical 0 level from ϕ to Q	$I_2 = 2$		350	700	ns
t_{pd1}	Propagation delay time to logical 1 level from S_o to Q	$I_1 = 1$ $I_2 = 1$		50		ns
t_{pd0}	Propagation delay time to logical 0 level from MR to Q	$I_1 = 2$ $I_2 = 2$		400		ns
t_{pw}	Minimum input pulse width from ϕ to MR				300	ns
f_{max}	Maximum clock frequency				1.5	MHz

*See switching times test circuit and waveforms

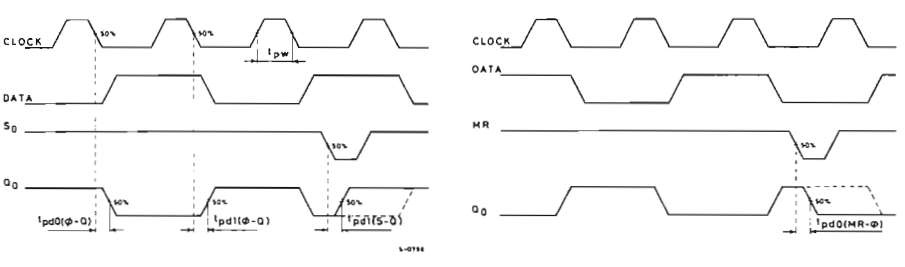
SWITCHING TIMES

Test circuit



NOTE: The pulse generators have the following characteristics: $t_r = t_f \geqslant 10$ ns @ 10V, $t_{pw} = 5\ \mu s$, PRR = 50 kHz (Pulse Generator 1), PRR = 25 kHz (Pulse Generator 2)

Waveforms



HLL INTEGRATED CIRCUITS

H 165
H 166

PRELIMINARY DATA

QUAD SCHMITT TRIGGER

- DELAY PINS ALLOW the USE of EXTERNAL SLOW-DOWN CAPACITOR
- IDEAL FOR USE as a LINE RECEIVER

The H 165 and H 166 (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line ceramic package. The H 165 (active pull-up output) and the H 166 (open collector output) are HLL integrated circuits. The device (H 165-H 166) is presented with a choice of two truth tables determined by whether an internal pull-up resistor (pin P) is left open or is connected to V_{CC}. If pin P is left open, the device will not recognize open circuits. By this we mean that the input will continue to see the logic state that was at the input before the connection was broken. It is this characteristic that eliminates errors due to contact baunce on relay or switch contacts. If pin P is tied to V_{CC}, the device acts like a standard HLL circuits and considers an open input connection to be a logic one. An inhibit pin is provided that forces all outputs high whenever it is high.

ABSOLUTE MAXIMUM RATINGS

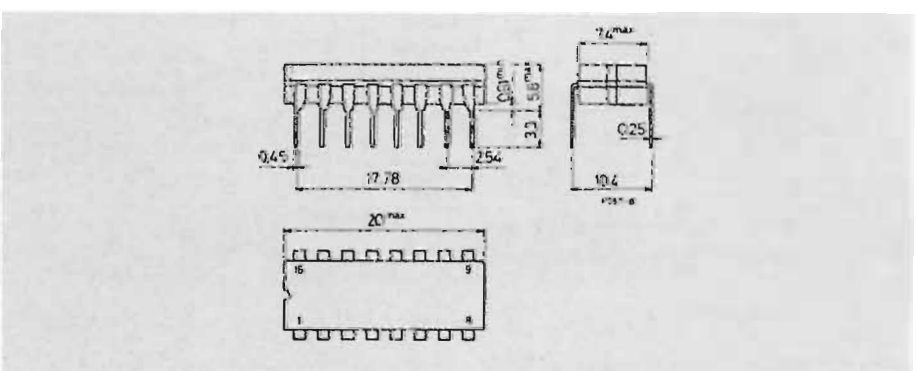
V_{CC}	Supply voltage	22	V
V_i	Input voltage	-0.5 to 20	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 75	°C

ORDERING NUMBERS:

H 165 D1 for dual in-line ceramic package (active pull-up output)
H 166 D1 for dual in-line ceramic package (open collector output)

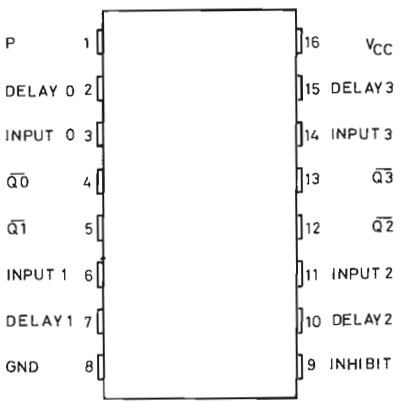
MECHANICAL DATA

Dimensions in mm



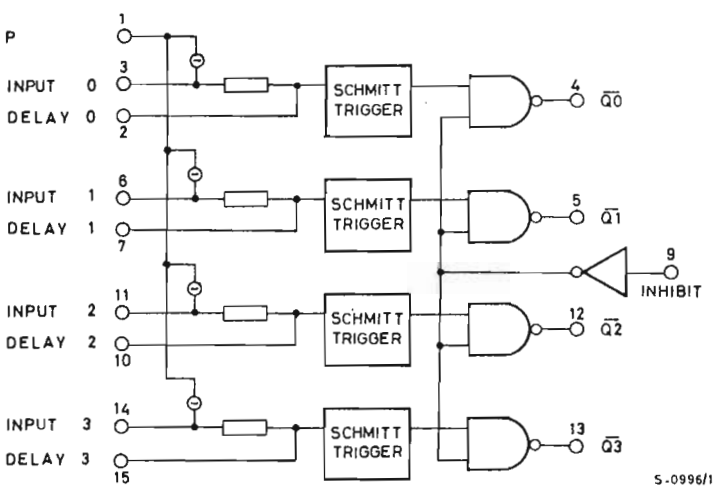
3/75

CONNECTION DIAGRAM



S-1068/1

BLOCK DIAGRAM



S-0996/1

* See truth tables

TRUTH TABLES

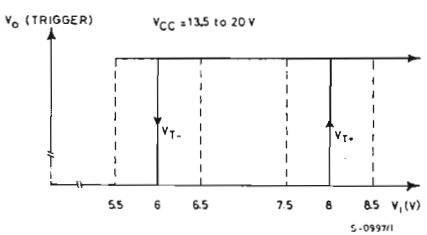
Pin 1 connected to V_{CC}

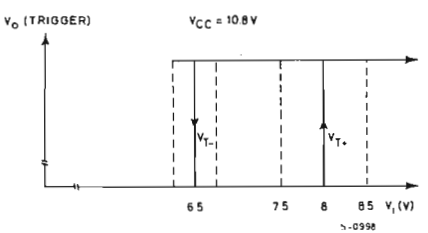
INPUTS				OUTPUTS	
INHIBIT		A			
t^n	t^{n+1}	t^n	t^{n+1}	t^n	t^{n+1}
0	0	0	open	1	0
0	0	1	open	0	0
1	1	X	X	1	1

Pin 1 open

INPUTS				OUTPUTS	
INHIBIT		A			
t^n	t^{n+1}	t^n	t^{n+1}	t^n	t^{n+1}
0	0	0	open	1	1
0	0	1	open	0	0
1	1	X	X	1	1

TRIGGER TRANSFER CHARACTERISTICS





RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	10.8 to 20	V
T_{op}	Operating temperature range	0 to 75	°C

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage (for **H 165** only)	I_{OH} = -200 μA $V_{i\ (INH.)}$ = V_{CC}				
		V_{CC} = 10.8V	9.3	9.8		V
		V_{CC} = 15 V	13.5	14		V
		V_{CC} = 20 V	18.5	19		V
V_{OL}	Output low voltage (for **H 165** only)	I_{OL} = 12 mA $V_{i\ (INH.)}$ = GND $V_{i\ (TRIG.)}$ = V_{CC} V_{CC} = 10.8 to 20V		1	1.5	V
V_{OL}	Output low voltage (for **H 166** only)	I_{OL} = 12 mA $V_{i\ (INH.)}$ = GND $V_{i\ (TRIG.)}$ = V_{CC} V_{CC} = 10.8 to 20V			0.4	V
V_{IL}	Input low voltage at inhibit input				6	V
V_{IH}	Input high voltage at inhibit input		8			V
I_R	Input reverse current at inhibit input	V_R = 20V V_{CC} = 20V			5	μA
I_F	Input low current at inhibit input	V_F = 1.5V V_{CC} = 10.8 to 20V			-0.4	mA
I_{SC}	Short-circuit output current (for **H 165** only)	$V_{i\ (INH.)}$ = V_{CC} V_{CC} = 20V	-9		-25	mA

STATIC ELECTRICAL CHARACTERISTICS (continued)

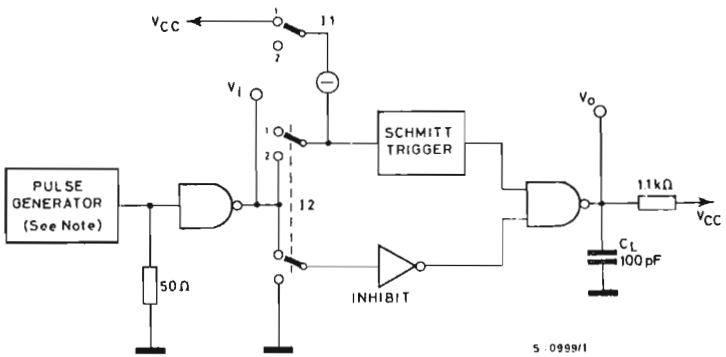
Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{PD}	Power dissipation current (for **H 165** only)	$V_{i\ (INH.)} = V_{CC}$ $V_{i\ (TRIG.)} = GND$ $V_{CC} = 20V$			38	mA
I_{PD}	Power dissipation current (for **H 166** only)	$V_{i\ (INH.)} = V_{CC}$ $V_{i\ (TRIG.)} = GND$ $V_{CC} = 20V$			33	mA
V_{T+}	Trigger positive transition threshold voltage at 3, 6, 11, 14 pins	$V_{CC} = 10.8$ to $20V$	7.5		8.5	V
V_{T-}	Trigger negative transition threshold voltage at 3, 6, 11, 14 pins	$V_{CC} = 10.8V$ $V_{CC} = 13.5$ to $20V$	 5.5	6.5	 6.5	V V
I_{T+}	Input current at positive going threshold (PIN 1 connected to V_{CC})	$V_{CC} = 20V$			5	μA
I_{T+}	Input current at positive going threshold (PIN 1 open)	$V_{CC} = 20V$			1	mA
I_{T-}	Input current at negative going threshold (PIN 1 connected to V_{CC})	$V_{CC} = 20V$			-3	mA
I_{T-}	Input current at negative going threshold (PIN 1 open)	$V_{CC} = 20V$			-1	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} = 15V, R_L = 1.1 kΩ, C_L = 100 pF, see test circuit)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{pd1}	Propagation delay time to logical 1 level from trigger input	Pull up input to V_{CC} I_1 (1) I_2 (2)			700	ns
t_{pd0}	Propagation delay time to logical 0 level from trigger input	Pull up input to V_{CC} I_1 (1) I_2 (2)			700	ns
t_{pd1}	Propagation delay time to logical 1 level from trigger input	Pull up input open I_1 (2) I_2 (2)			700	ns
t_{pd0}	Propagation delay time to logical 0 level from trigger input	Pull up input open I_1 (2) I_2 (2)			700	ns
t_{pd1}	Propagation delay time to logical 1 level from inhibit input	Pull up input to V_{CC} I_1 (1) I_2 (1)			500	ns
t_{pd0}	Propagation delay time to logical 0 level from inhibit input	Pull up input to V_{CC} I_1 (1) I_2 (1)			500	ns
t_{pd1}	Propagation delay time to logical 1 level from inhibit input	Pull up input open I_1 (2) I_2 (1)			500	ns
t_{pd0}	Propagation delay time to logical 0 level from inhibit input	Pull up input open I_1 (2) I_2 (1)			500	ns

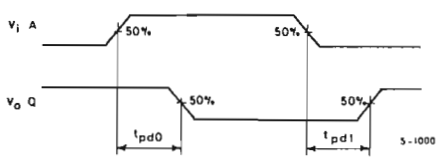
SWITCHING TIMES

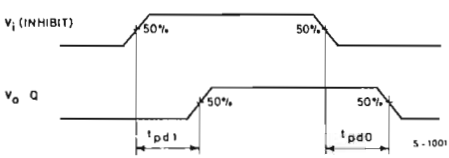
Test circuit



NOTE: The pulse generators have the following characteristics: $t_r = t_f \leqslant 10$ ns @ 10V, $t_{pw} = 5$ µs, PRR = 100 kHz

Waveforms





H 167
H 168

PRELIMINARY DATA

QUAD 2 - INPUT EXCLUSIVE OR GATE

The H 167 and H 168 (standard temperature range) are monolithic integrated circuits, available in 14-lead dual in-line ceramic package.

ABSOLUTE MAXIMUM RATINGS

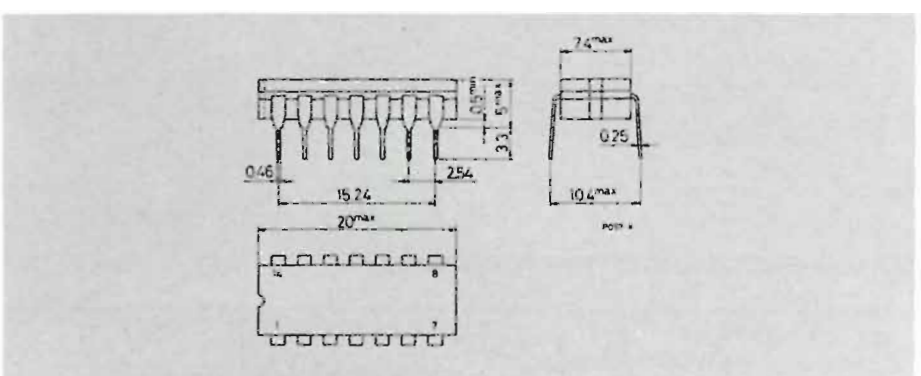
V_{CC}	Supply voltage	22	V
V_i	Input voltage	-0.5 to 20	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 75	°C

ORDERING NUMBERS:

H 167 D1 for dual in-line ceramic package (active pull-up output)
H 168 D1 for dual in-line ceramic package (open collector output)

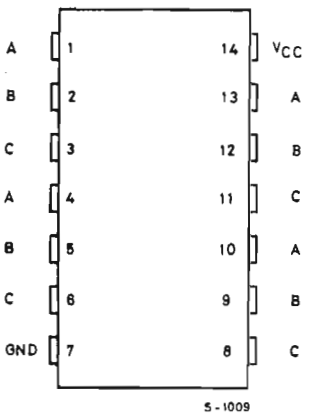
MECHANICAL DATA

Dimensions in mm

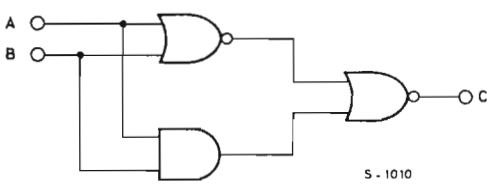


H 167
H 168

CONNECTION DIAGRAM



BLOCK DIAGRAM



TRUTH TABLE

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	10.8 to 20	V
T_{op}	Operating temperature range	0 to 75	°C

STATIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25 °C)

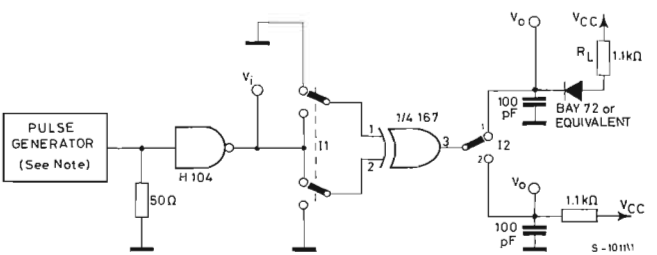
Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage (for **H 167** only)	I_{OH} = -200 μA V_i = V_{IL} V_{CC}= 10.8V V_{CC}= 15 V V_{CC}= 20 V	 9.3 13.5 18.5	 9.8 14 19	 	 V V V
V_{OL}	Output low voltage (for **H 167** only)	I_{OL} = 12 mA V_i = V_{IH} V_{CC}= 10.8 to 20V	 	 1	 1.5	 V
V_{OL}	Output low voltage (for **H 168** only)	I_{OL} = 12 mA V_i = V_{IH} V_{CC}= 10.8 to 20V	 	 	 0.4	 V
V_{IL}	Input low voltage				6	V
V_{IH}			8			V
I_R	Input reverse current	V_R = 20V V_{CC}= 20V	 	 	 5	 μA
I_F	Input low current	V_F = 1.5V V_{CC}= 20V	 	 -0.1	 -0.4	 mA
I_{SC}	Short-circuit output current (for **H 167** only)	Input and output grounded V_{CC}= 20V	 -9	 	 -25	 mA
I_{PD}	Power dissipation current (for **H 167** only)	V_{CC}= 20V			38	mA
I_{PD}	Power dissipation current (for **H 168** only)	V_{CC}= 20V			33	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} = 15V, R_L = 1.1 KΩ, C_L = 100 pF)

Parameter		Test conditions	Min. Typ. Max.	Unit
t_{pd1}	Propagation delay time to logical 1 level	See test circuit	250	ns
t_{pd0}	Propagation delay time to logical 1 level	See test circuit	120	ns

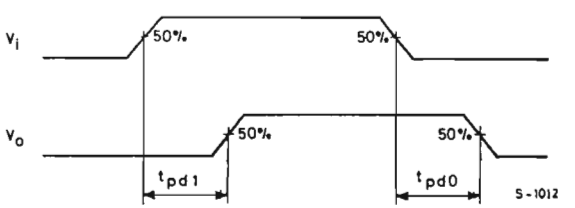
SWITCHING TIMES

Test circuit



NOTE: The pulse generator have the following characteristics: $t_r = t_f \leqslant 10$ ns @ 10V, $t_{pw} = 5$ µs, PRR = 100 kHz

Waveform



HLL INTEGRATED CIRCUITS

H 200 series

PRELIMINARY DATA

HIGH LEVEL LOGIC FAMILY

- WIDE RANGE of SUPPLY VOLTAGE 10.8 to 16V.
- HIGH DC NOISE IMMUNITY 5V (TYP.) at V_{CC} = 15V
- HIGH FANOUT 25 (WORST CASE)
- COMPATIBLE WITH COS/MOS ICs

High Level Logic is a family of high threshold integrated circuits. It offers the advantages of 5V DC noise immunity, high signal levels, large supply voltage tolerances and unusually high fanout. These features make the family particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit. The H 200 series elements are available in standard temperature range (0 to 75 °C) it comes in 14 and 16 pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS

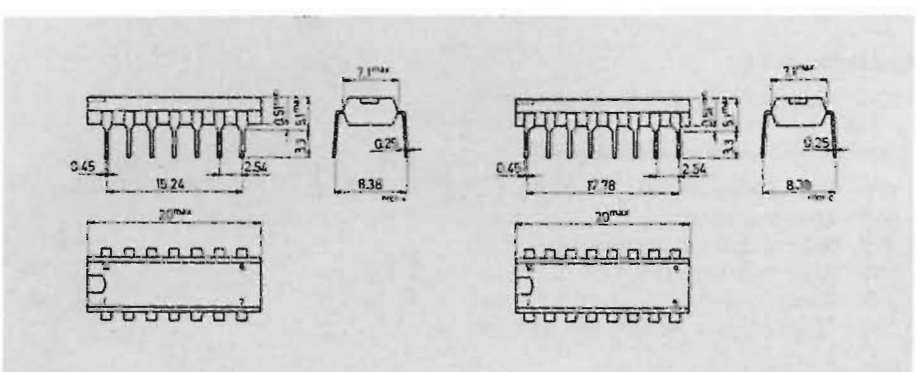
V_{CC}	Supply voltage	18	V
V_i	Input voltage	-0.5 to 16	V
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBER

H 2XX B1 for dual in-line plastic package

MECHANICAL DATA

Dimensions in mm



RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	10.8 to 16	V
T_{op}	Operating temperature range	0 to 75	°C

TYPE DESCRIPTIONS

Gates

H 202 Quad 2-input NAND gate (active pull-up)
H 203 Triple 3-input NAND gate (active pull-up)
H 204 Dual 4-input expandable NAND gate (active pull-up)
H 205 Dual 2-wide 2-input expandable AND-NOR gate (active pull-up)
H 209 Dual 4-input expandable power AND gate (open collector)
H 212 Hex inverter (open collector)
H 213 Dual 2-input NAND gate plus dual expandable inverter (open collector)
H 214 Quad TTL to HLL-COS/MOS converter
H 215 Strobed hex inverter (open collector)
H 218 Hex inverter (active pull-up)
H 219 Strobed hex inverter (active pull-up)
H 222 Quad 2-input NAND gate (passive pull-up)
H 224 Dual 4-input expandable NAND gate (passive pull-up)
H 267 Quad 2-input exclusive OR gate (active- pull-up)
H 268 Quad 2-input exclusive OR gate (open collector)

Memory elements

H 210 Dual J-K flip-flop with set input
H 211 Dual J-K flip-flop with set and clear inputs
H 259 Quad D-latch

Monostable element

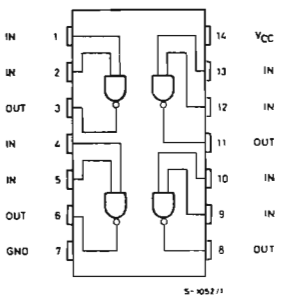
H 217 Monostable/astable multivibrator

Counters, register and special elements

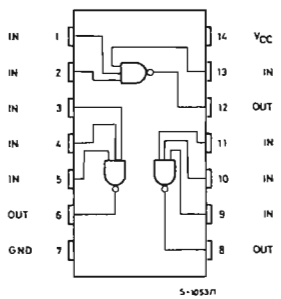
H 256 4-bit binary counter
H 257 Decade counter
H 258 BCD to decimal decoder/driver
H 260 4-bit shift register
H 265 Quad Schmitt trigger (active pull-up)
H 266 Quad Schmitt trigger (open collector)

CONNECTION DIAGRAMS

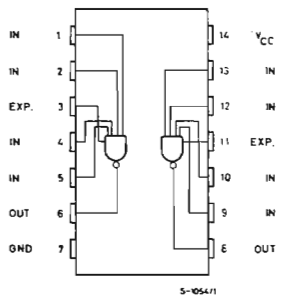
H 202/H 222



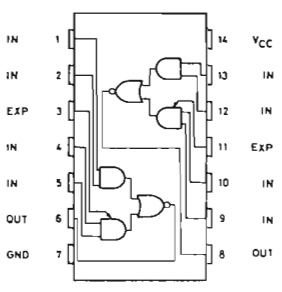
H 203



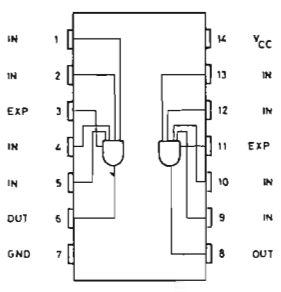
H 204/H 224



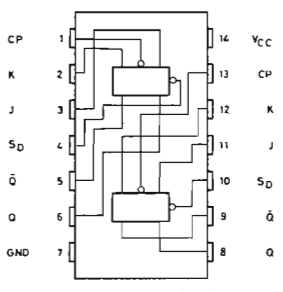
H 205



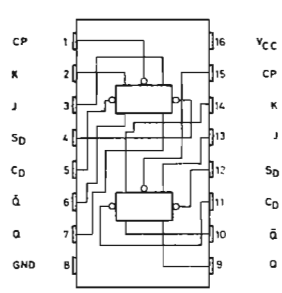
H 209



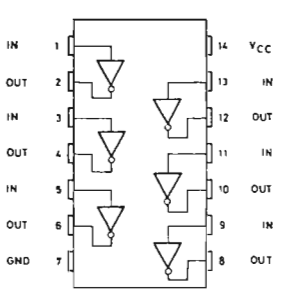
H 210



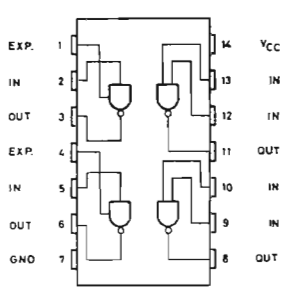
H 211



H 212/H 218

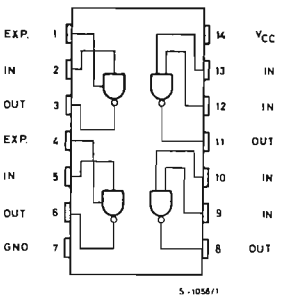


H 213

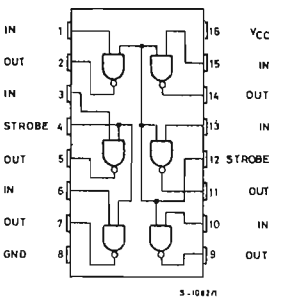


CONNECTION DIAGRAMS (continued)

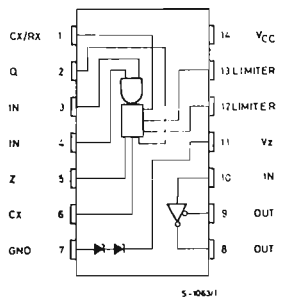
H 214



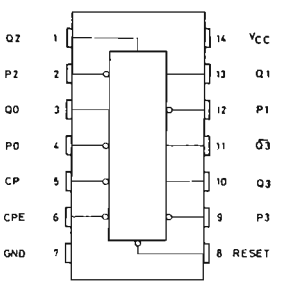
H 215/H 219



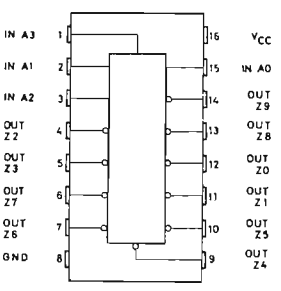
H 217



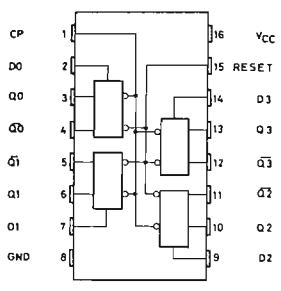
H 256/H 257



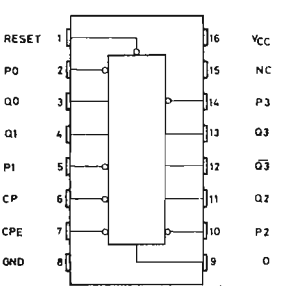
H 258



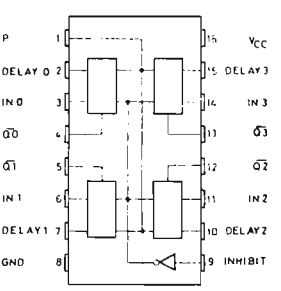
H 259



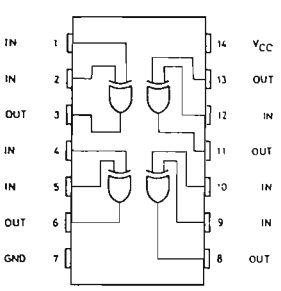
H 260



H 265/H 266



H 267/H 268



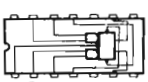
LPDTL INTEGRATED CIRCUITS

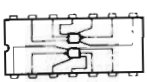
LPDTL INTEGRATED CIRCUITS

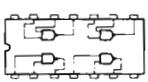
The following LPDTL devices are currently in production. Data sheets can be supplied on request.

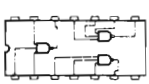
		t_{pd} (ns)	P_D (mW)	f (MHz)	Fan Out
GATES					
E 301	Dual 3-Input	60	2		10
E 302	Quad 2-Input	60	4		10
E 303	Triple 3-Input	60	3		10
E 304	Dual 4-Input with Extender	60	2		10
E 305	Dual 3-Input with Extender	60	2		10
E 306	3 and 4-Input with Extender	60	2		10
FLIP-FLOPS					
E 300	Clocked			2.5	10

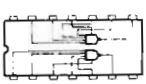
CONNECTION DIAGRAMS

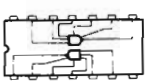

E300


E301


E302


E303


E304


E305


E306

Typical noise immunity: 1 V.
Extended temperature range (— 55°C to + 125°C): ceramic flat and DIP packages.
Standard temperature range (— 20°C to + 100°C): ceramic flat and DIP packages.

RTL INTEGRATED CIRCUITS

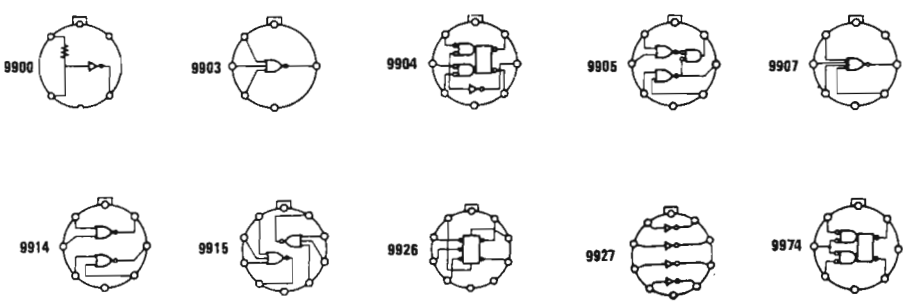
RTL INTEGRATED CIRCUITS

The following RTL devices are currently in production. Data sheets can be supplied on request.

		t_{pd} (ns)	P_D (mW)	f (MHz)	Fan Out
GATES					
9900	NOR buffer	10	20		80
9903*	NOR 3-Input	10	20		16
9907	NOR 4-Input	10	40		16
9914	NOR Dual 2-Input	15	40		16
9915	NOR Dual 3-Input	10	40		16
FLIP-FLOPS					
9926	JK		90	20	
9974	JK		90		
OTHER FUNCTIONS					
9904	Half adder	20	75		16
9905*	Half shift register	20	77		16
9927	Quad Inverter	10	30		16

* Standard temp. range only

CONNECTION DIAGRAMS



Extended temperature range (55°C to +125°C): TO-99/TO-100 packages.
Standard temperature range (0°C to +70°C): TO-99/TO-100 packages.

Printed in Italy by Pirovano - Segrate - Milano

ALPHA-NUMERICAL INDEX

DTL INTEGRATED CIRCUITS

TTL INTEGRATED CIRCUITS

HLL INTEGRATED CIRCUITS

LPDTL INTEGRATED CIRCUITS

RTL INTEGRATED CIRCUITS